High Data Rate 60 GHz CMOS Transceiver Design

Akira Matsuzawa

Tokyo Institute of Technology

Nov.12. 2015.

Contents

TOKYO TECH Pursuing Excellence

- Background and Motivation
- Development of High Data Rate 60 GHz CMOS Transceivers
- High Data Rate Circuits Design
- Basic Design Method for 60GHz CMOS RF Circuits
- High Speed and Low Power ADC
- Future Prospect of High Data Rate Wireless Systems
- Summary

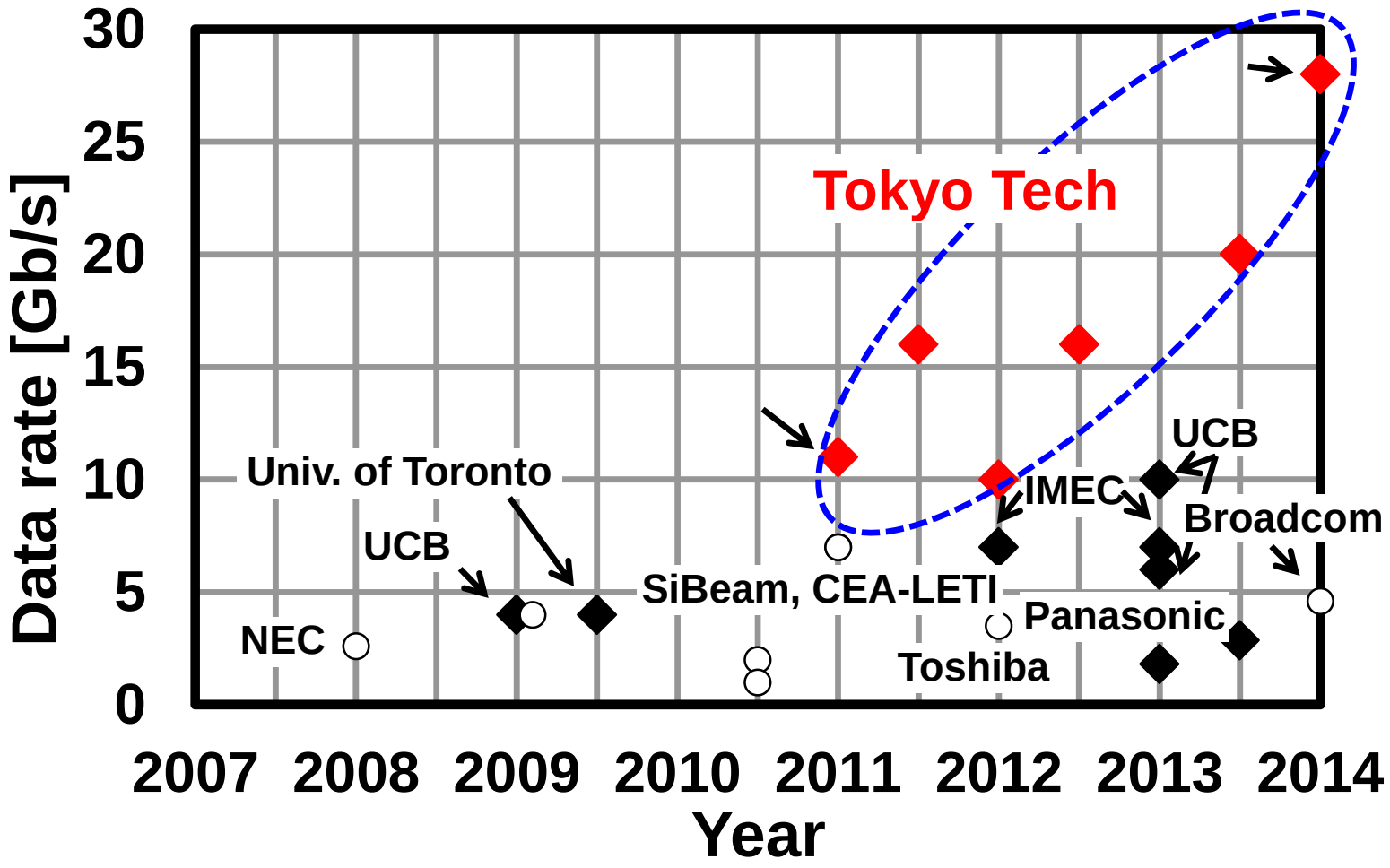
TOKYO TECH
Pursuing Excellence

Background and Motivation

Progress of data rate in 60 GHz band

TOKYO TECH Pursuing Excellence

Our lab. is developing high data rate wireless transceivers.
28 Gbps has been attained.



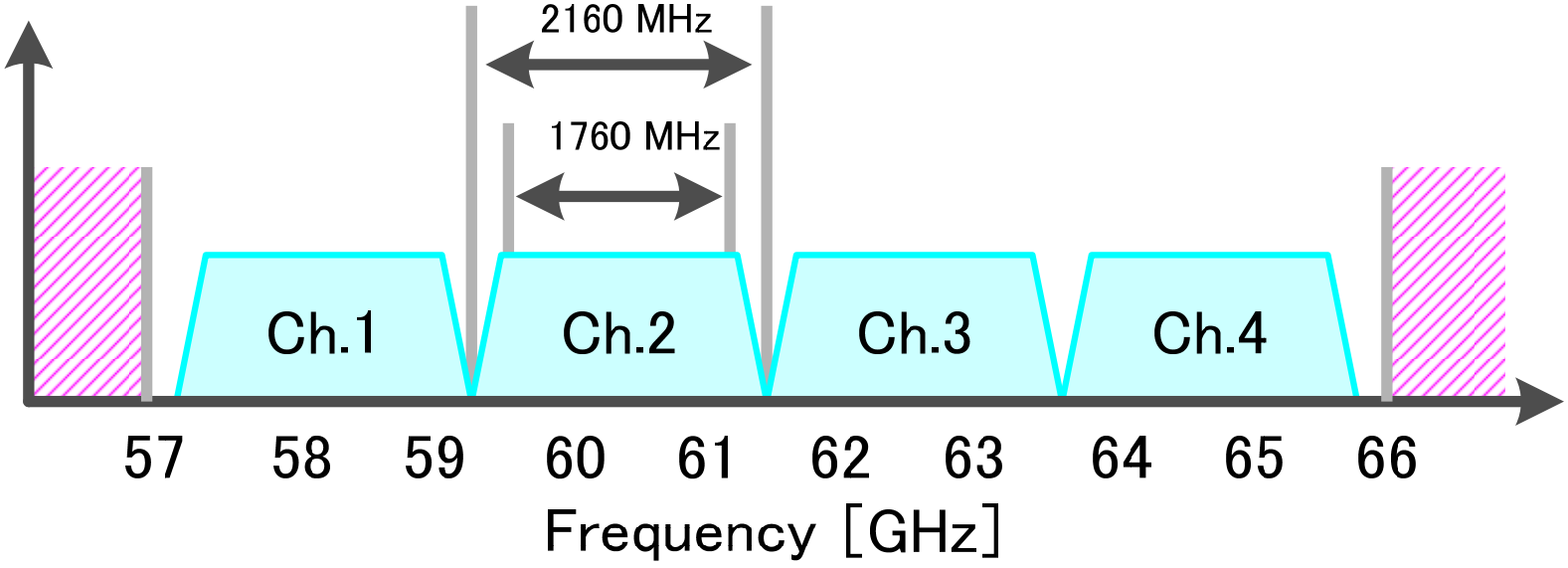
Matsuzawa & Okada Lab.

60GHz bandwidth allocation on IEEE 802.ad

TOKYO TECH Pursuing Excellence

Totally 9 GHz can be used.
The use of high # of bit can attain ultra-high data rate com.

	BPSK	QPSK	16QAM	64QAM
1ch	1.76	3.52	7.04	10.56
2ch	3.52	7.04	14.08	21.12
3ch	5.28	10.56	21.12	31.68
4ch	7.04	14.08	28.16	42.24

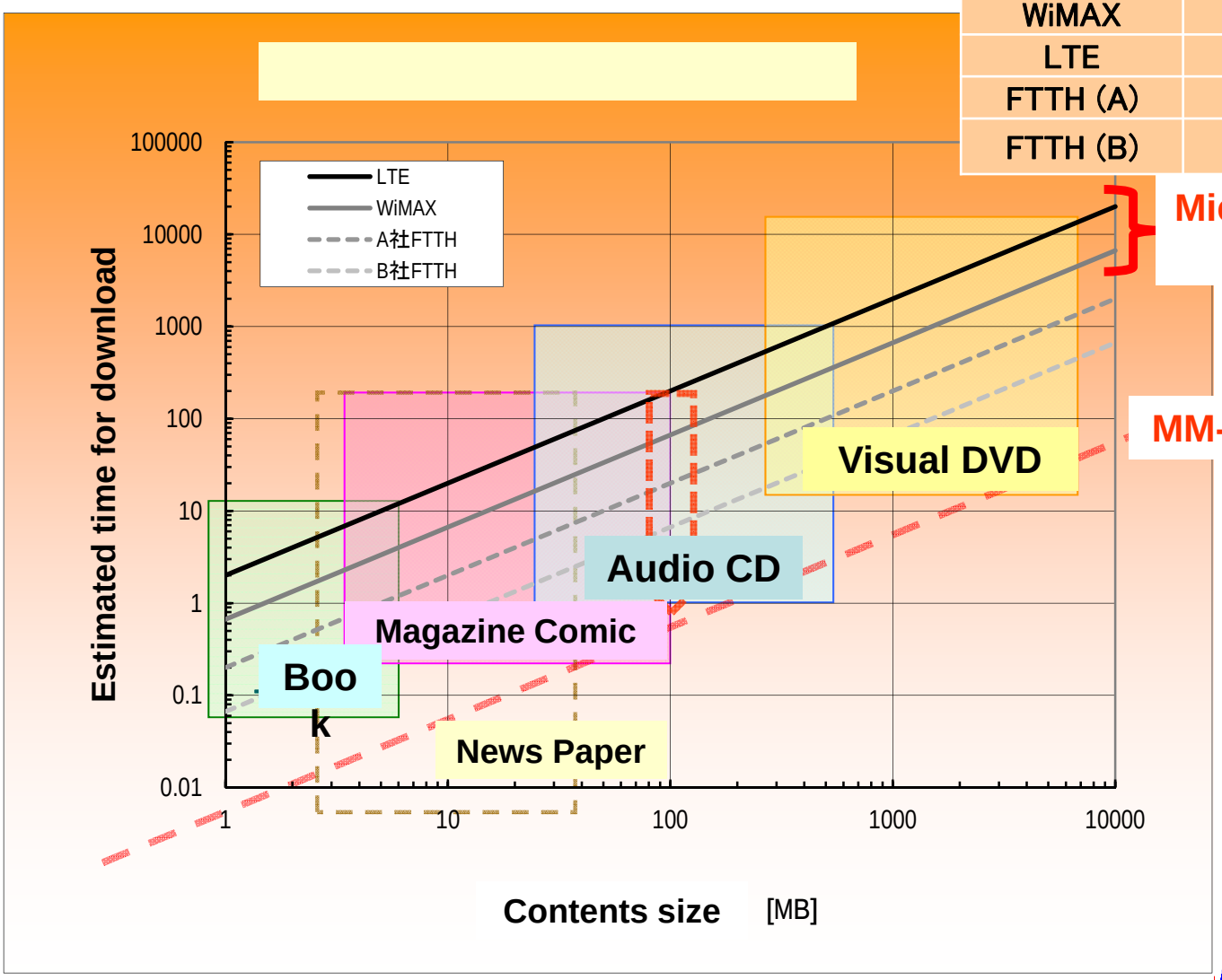


Matsuzawa & Okada Lab.

Time for big data contents download

60GHz MM wave can transfer the DVD data within several seconds

Measured average effective data rate as of Jan. 2011	
WiMAX	12 Mbps
LTE	4 Mbps
FTTH (A)	40 Mbps
FTTH (B)	120 Mbps



WiGig Usage Models

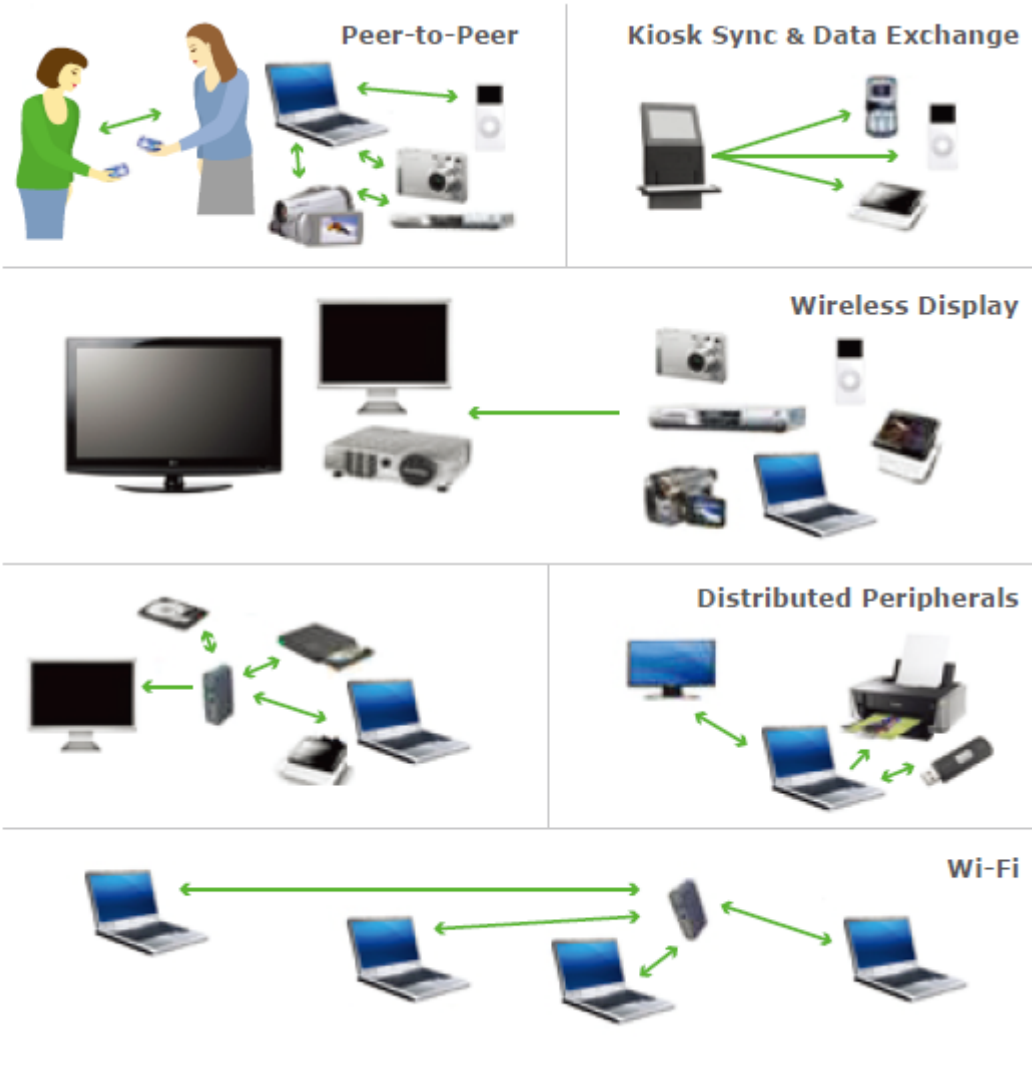
TOKYO TECH Pursuing Excellence

Instant Wireless Sync
- IP-based P2P applications
- Using I/O PAL

Wireless Display
- HD streams over HDMI or DP using A/V PAL
- CE, PE and HH usages

Cordless Computing
- Combination of Wireless display using A/V PAL, sync and I/O using I/O PAL

Internet Access
- Using native Wi-Fi, 802.11ad support



WiGig White Paper, "Defining the Future of Multi-Gigabit Wireless Communications" July 2010

TOKYO TECH
Pursuing Excellence

Development of High Data Rate

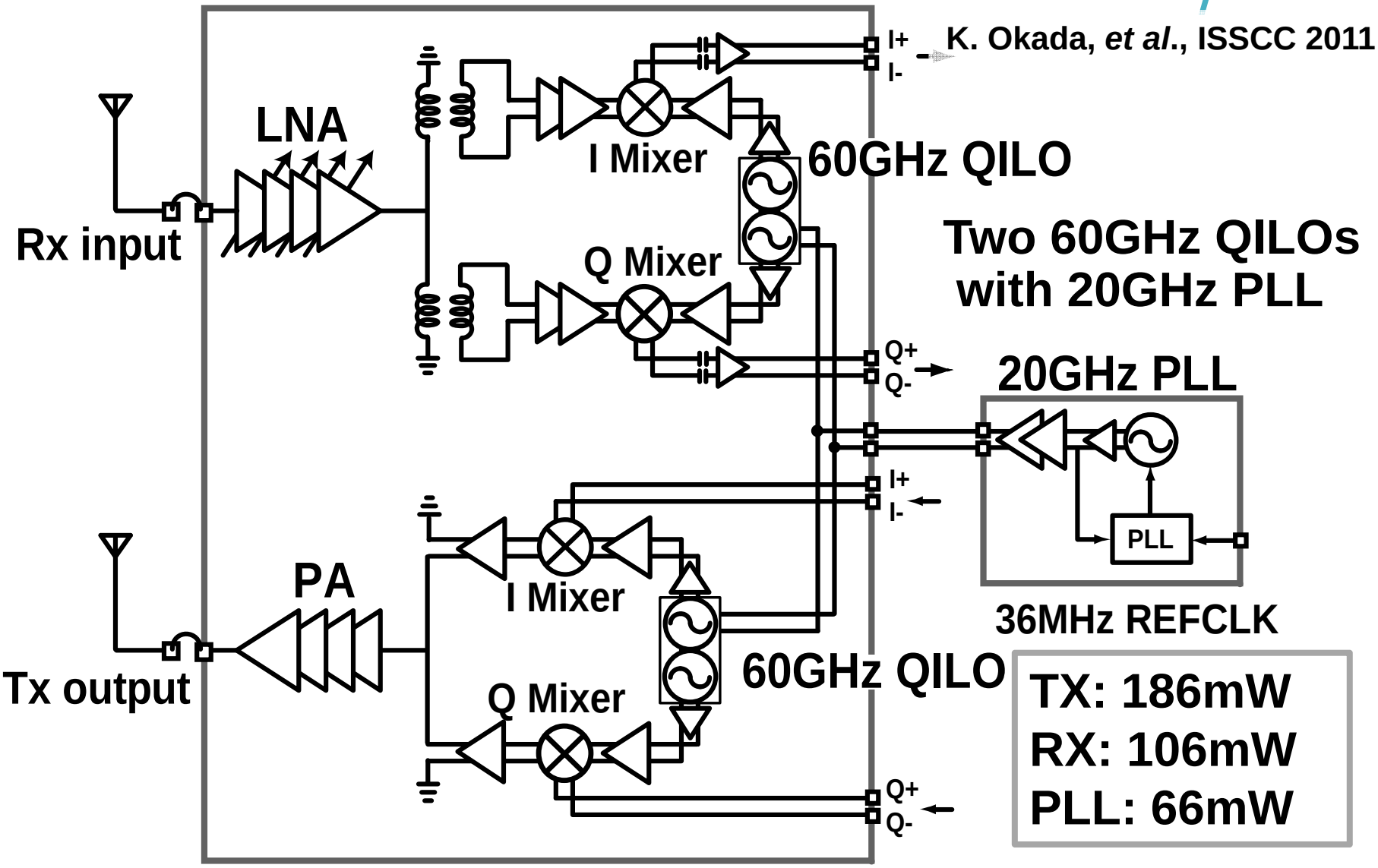
60 GHz CMOS Transceivers

Matsuzawa & Okada Lab.

The 1st 60GHz transceiver on ISSCC 2011

TOKYO TECH Pursuing Excellence

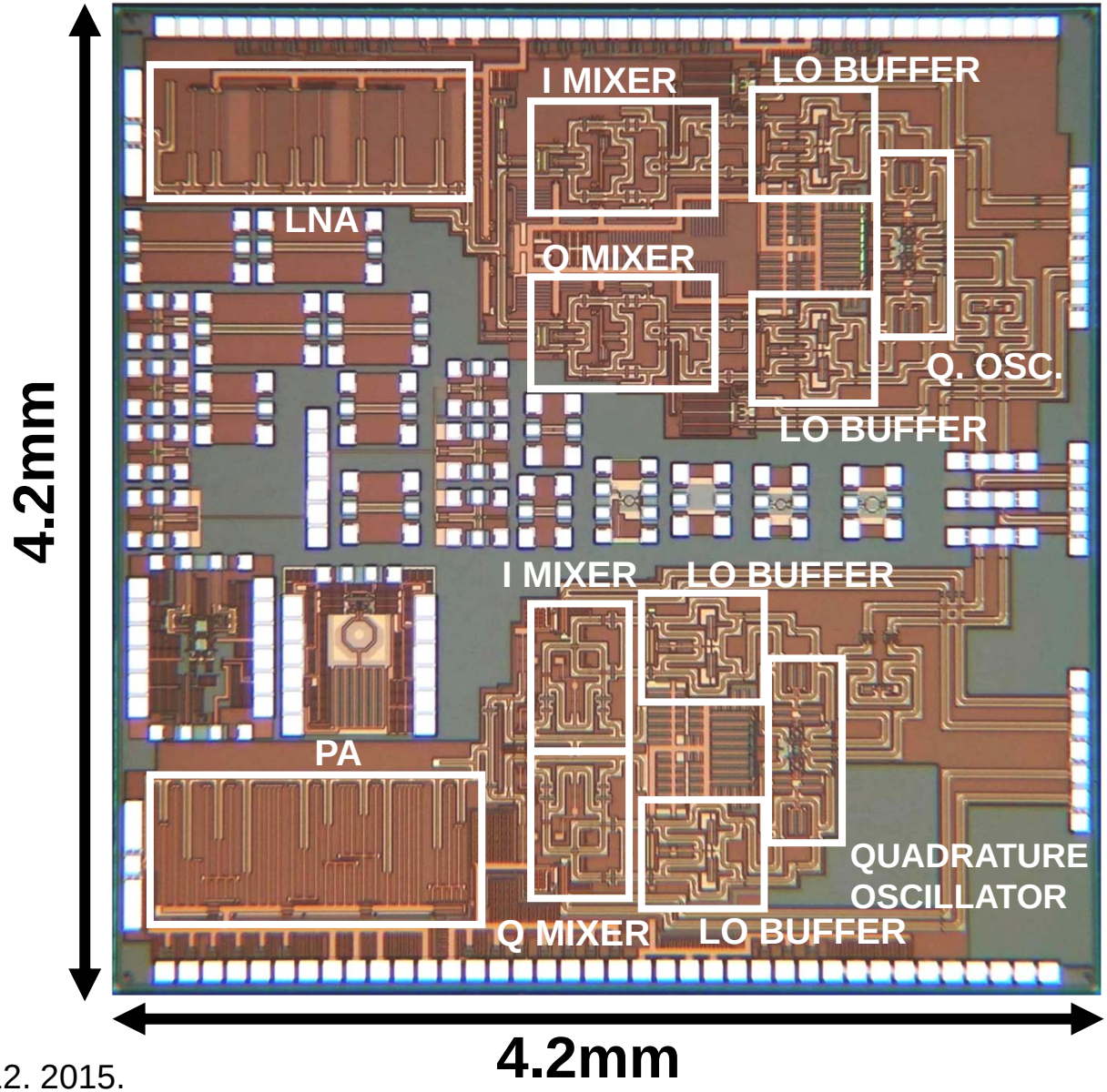
Direct conversion



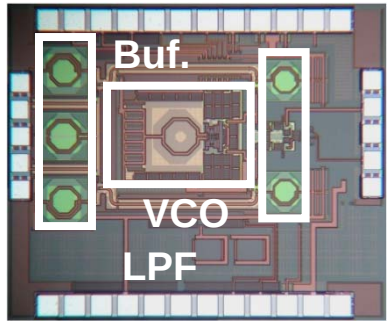
Matsuzawa & Okada Lab.

The 1st 60GHz transceiver on ISSCC 2011

TOKYO TECH Pursuing Excellence



11Gb/s (16QAM)
8Gb/s (QPSK)



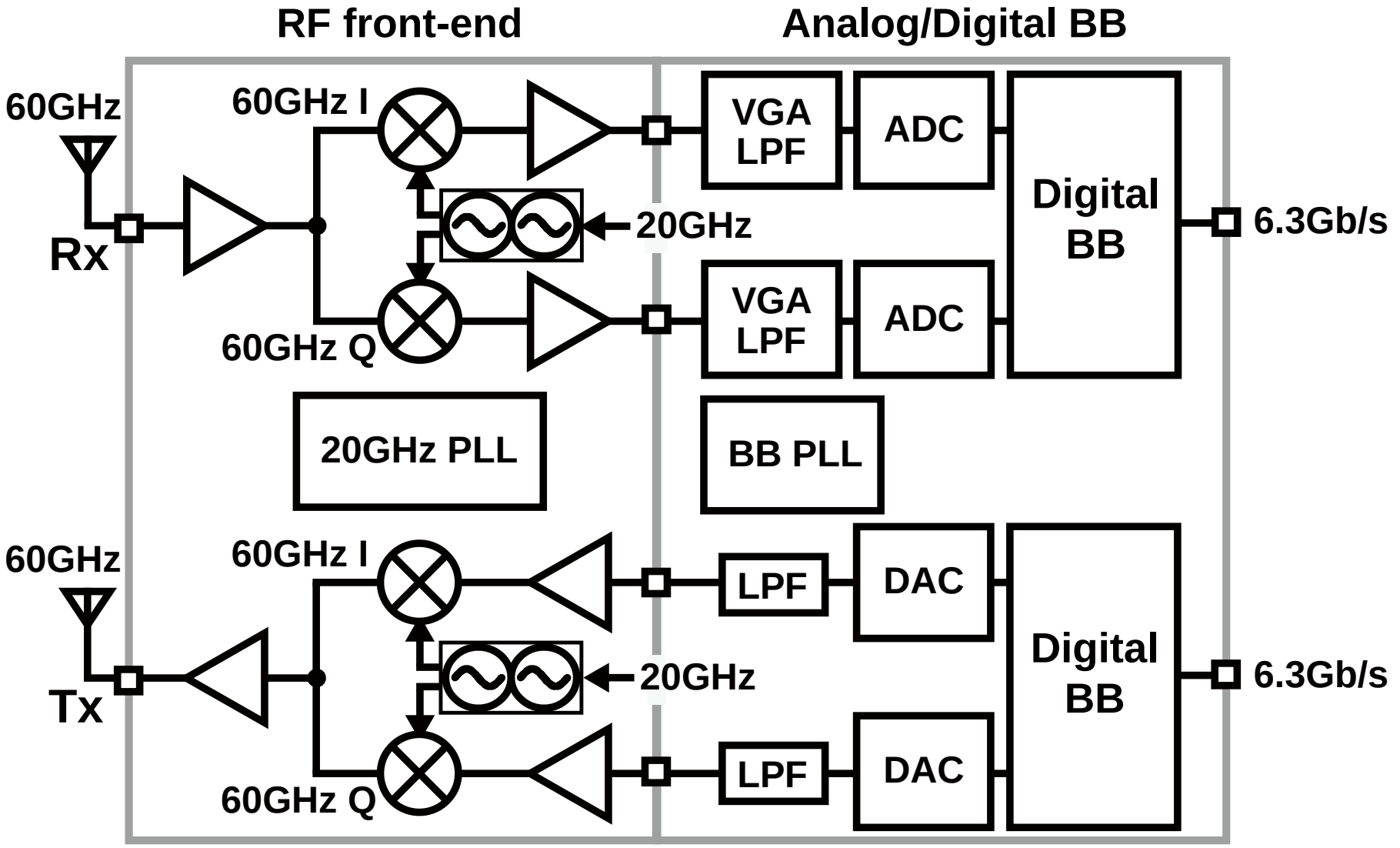
20GHz PLL
65nm CMOS
Rx:3.8mm²
Tx:3.5mm²
PLL:1.2mm²

Matsuzawa & Okada Lab.

The 2nd 60GHz Transceiver on ISSCC 2012

TOKYO TECH Pursuing Excellence

RF and baseband chips have been developed



K. Okada, *et al*., ISSCC 2012

Matsuzawa & Okada Lab.

The 2nd 60GHz Transceiver on ISSCC 2012

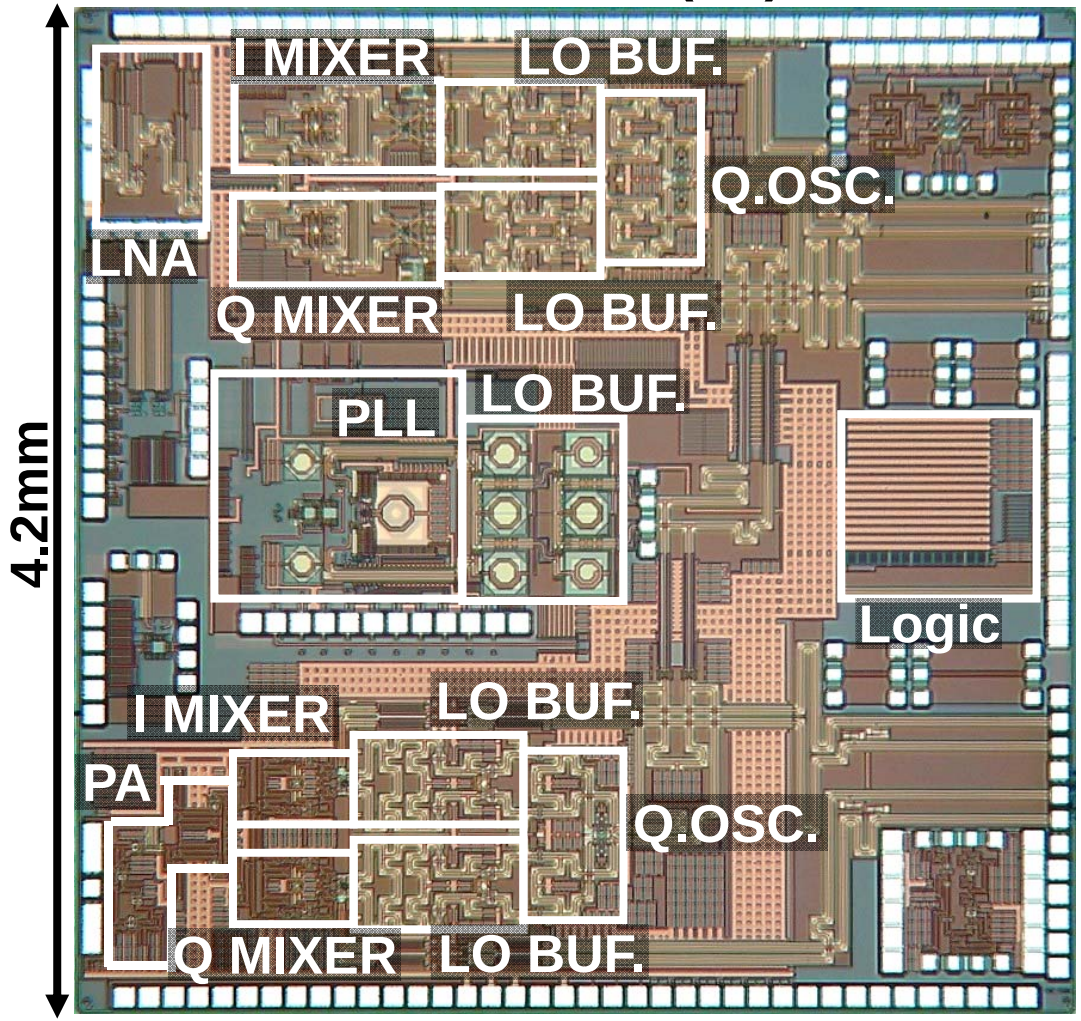
TOKYO TECH Pursuing Excellence

Full transceiver has been developed.

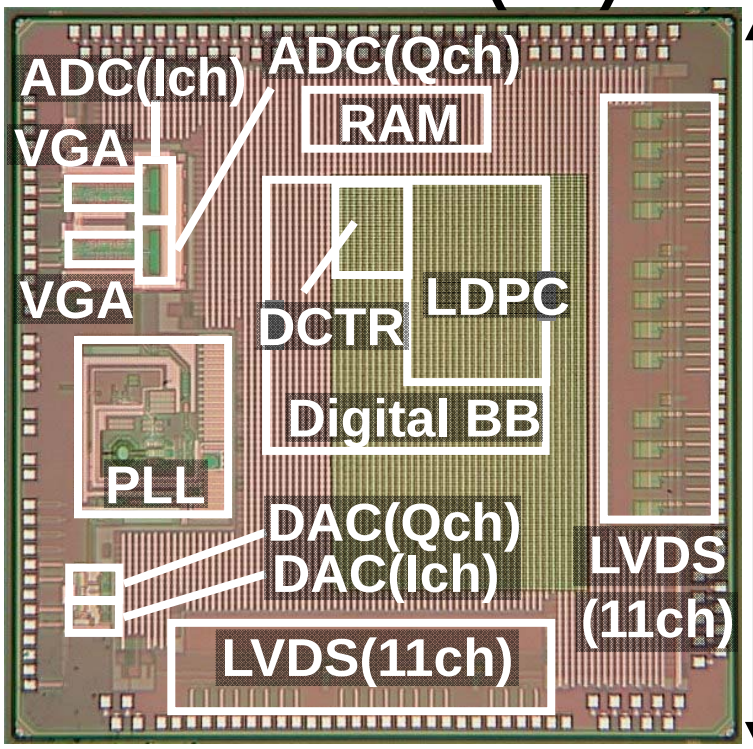
10Gb/s (16QAM)
TX: 319mW
RX: 223mW

K. Okada, *et al.*, ISSCC 2012

65nm CMOS (RF)



40nm CMOS (BB)



Tokyo Tech

SONY

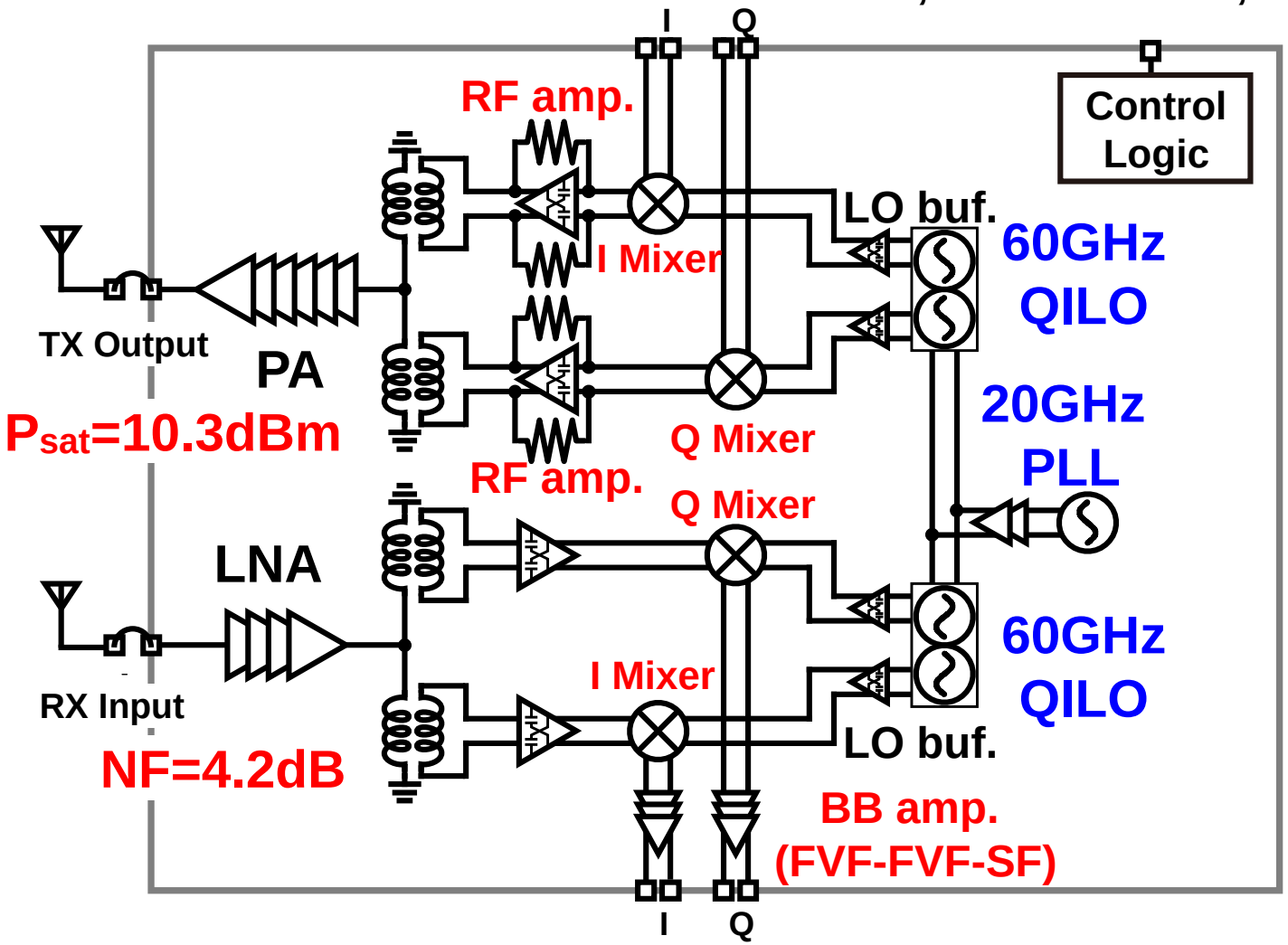
Matsuzawa & Okada Lab.

The 3rd 60 GHz Transceiver on ISSCC 2014

TOKYO TECH Pursuing Excellence

Direct conversion method is used for wider bandwidth and low power

*K. Okada, A. Matsuzawa., ISSCC 2014

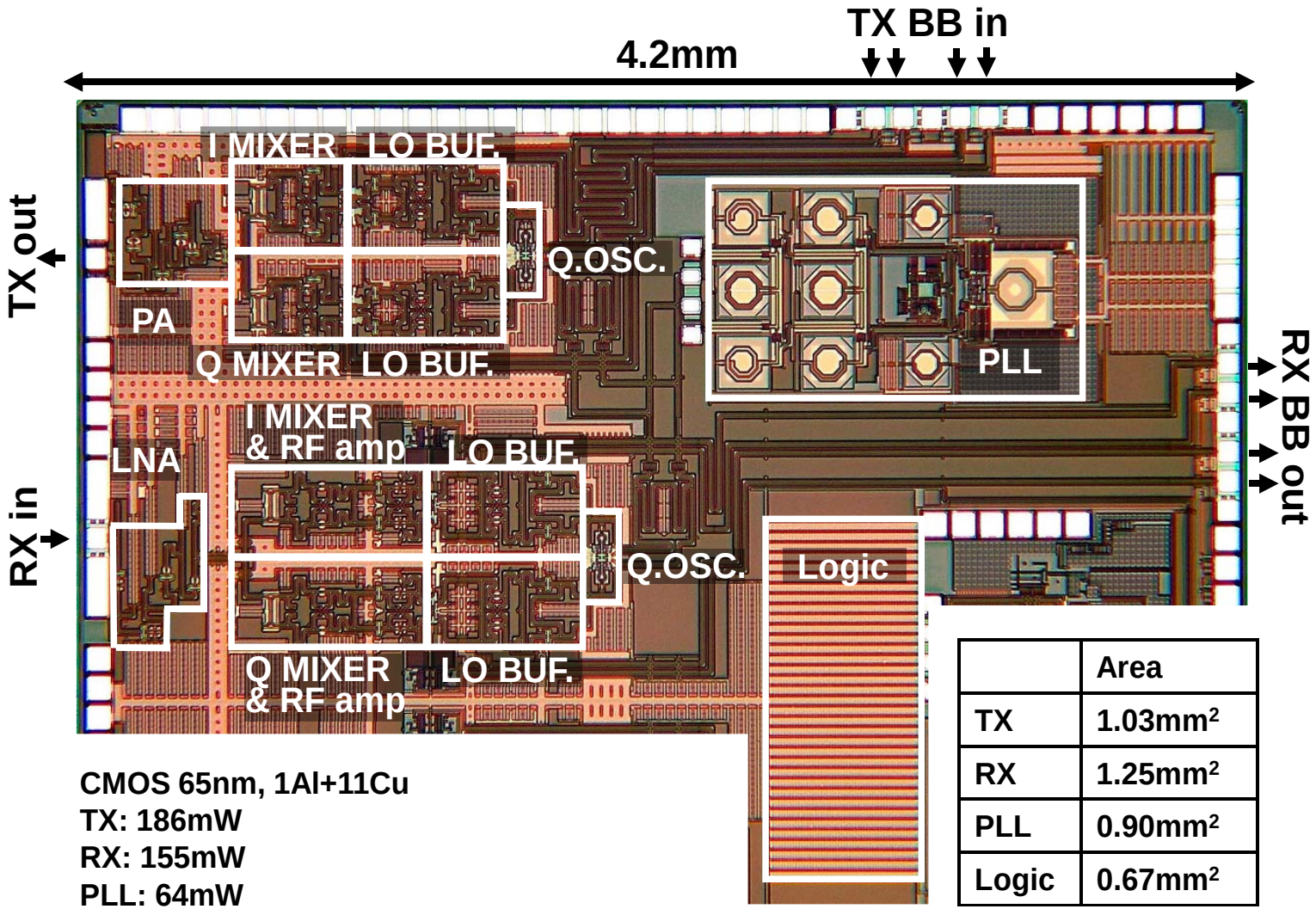


Matsuzawa & Okada Lab.

The 3rd 60 GHz Transceiver on ISSCC 2014

TOKYO TECH Pursuing Excellence

Chip was fabricated in 65 nm CMOS technology



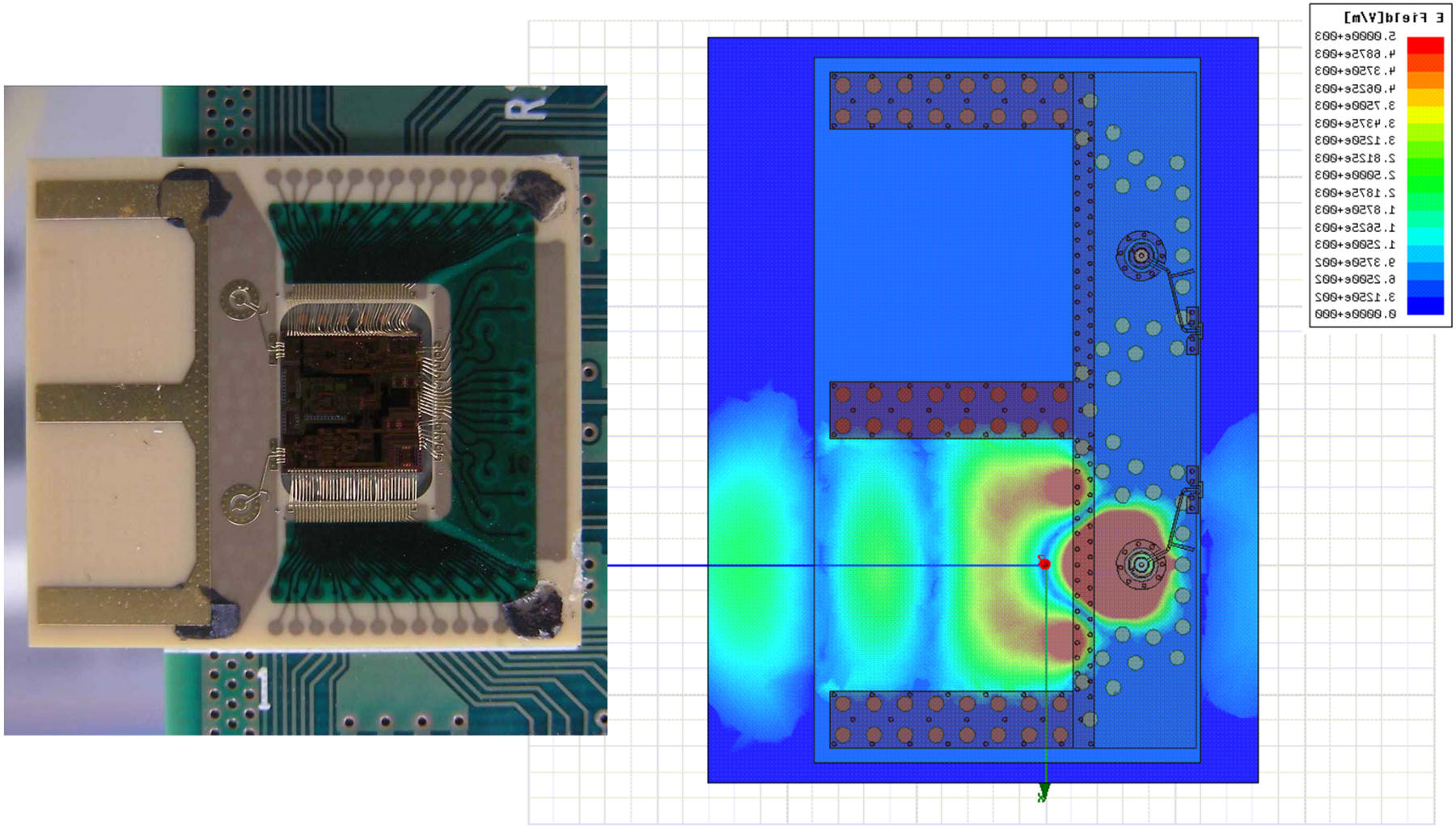
CMOS 65nm, 1Al+11Cu
TX: 186mW
RX: 155mW
PLL: 64mW

	Area
TX	1.03mm^2
RX	1.25mm^2
PLL	0.90mm^2
Logic	0.67mm^2

Chip with antenna in package

TOKYO TECH
Pursuing Excellence

The 60GHz RF chip are mounted on the antenna in package

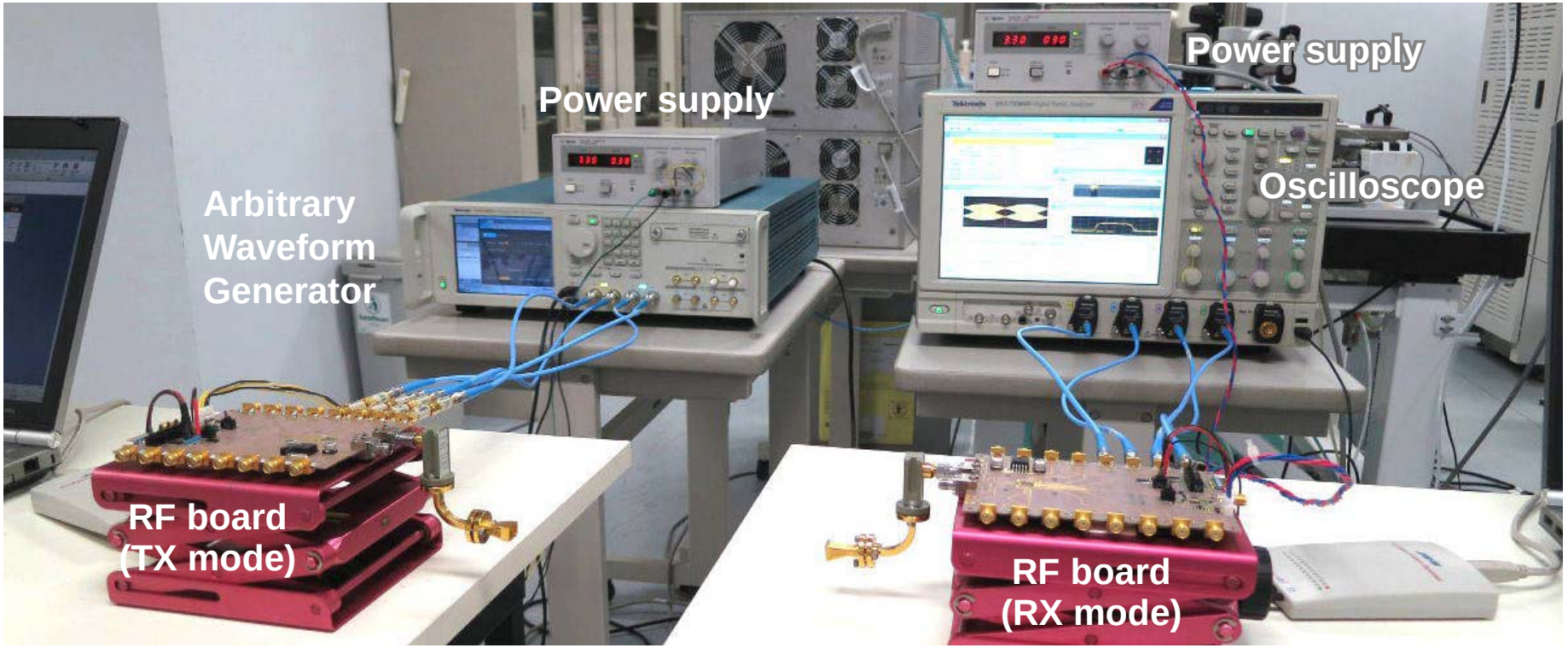


Matsuzawa & Okada Lab.

Chip measurement setup

TOKYO TECH Pursuing Excellence

Chip was measured with high speed measurement system

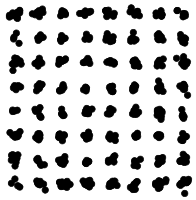
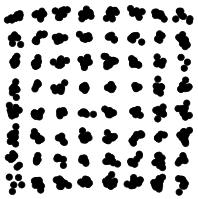
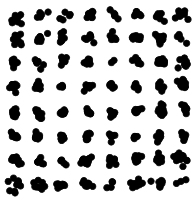
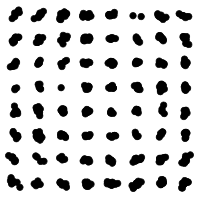
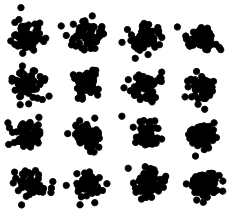
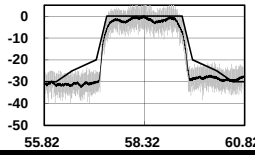
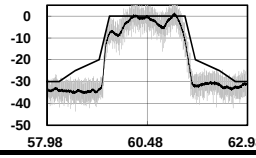
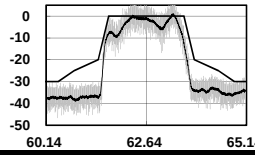
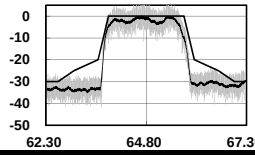
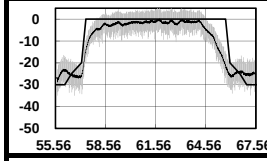


- **25-GS/s AWG**
- **100-GS/s oscilloscope (33GHz BW)**
- **14-dBi horn antennas**

Measured result

TOKYO TECH Pursuing Excellence

The world's first 64 QAM has been realized
The world's fastest 28 Gbps has been attained.

Channel	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 bond
Modula-tion	64QAM				16QAM
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s	28.16Gb/s
Conste-llation					
Spec-trum					
TX EVM	-27.1dB	-27.5dB	-28.0dB	-28.8dB	-20.0dB
TX-to-RX EVM	-24.6dB	-23.9dB	-24.4dB	-26.3dB	-17.2dB

Matsuzawa & Okada Lab.

Performance comparison

TOKYO TECH Pursuing Excellence

Highest data rate with low EVM and power dissipation

	Data rate / Modulation	TX-to-RX EVM	Integration	Power consumption
SiBeam [3]	7.14Gb/s(16QAM)	-19dB	65nm, 32x32-array heterodyne, TX, RX, LO	TX: 1,820mW RX: 1,250mW
Tokyo Tech [4, 5]	16Gb/s(16QAM) 20Gb/s(16QAM)[5]	-21dB	65nm, direct-conversion, TX, RX, LO, antenna, analog & digital BB	TX: 319mW RX: 223mW
IMEC [6]	7Gb/s(16QAM)	-18dB	40nm, direct-conversion, TX, RX, w/o PLL	TX: 167mW RX: 112mW
Toshiba [7]	2.62Gb/s(QPSK)	N/A	65nm, heterodyne, TX, RX, LO, antenna, analog & digital BB	TX: 160mW RX: 233mW
IMEC [8]	7Gb/s(16QAM)	-15dB	40nm, 4-array direct-conversion, TX, RX, LO, antenna	TX: 330mW RX: 284mW for 1 stream
Panasonic [9]	2.5Gb/s(QPSK)	-22dB	90nm, direct-conversion, TX, RX, LO, antenna, analog & digital BB	TX: 347mW RX: 274mW
Broadcom [10]	4.6Gb/s(16QAM)	-20dB	40nm, 16-array heterodyne, TX, RX, LO, antenna, analog/digital BB	TX: 960mW RX: 1190mW
This work	10.56Gb/s(64QAM) 28.16Gb/s(16QAM)	-26dB	65nm, direct-conversion, TX, RX, LO	TX: 251mW RX: 220mW

Matsuzawa & Okada Lab.

TOKYO TECH
Pursuing Excellence

High Data Rate Circuits Design

Matsuzawa & Okada Lab.

Data rate in communication

Wider bandwidth and higher SNR are required to attain higher data rate

Shannon's theory

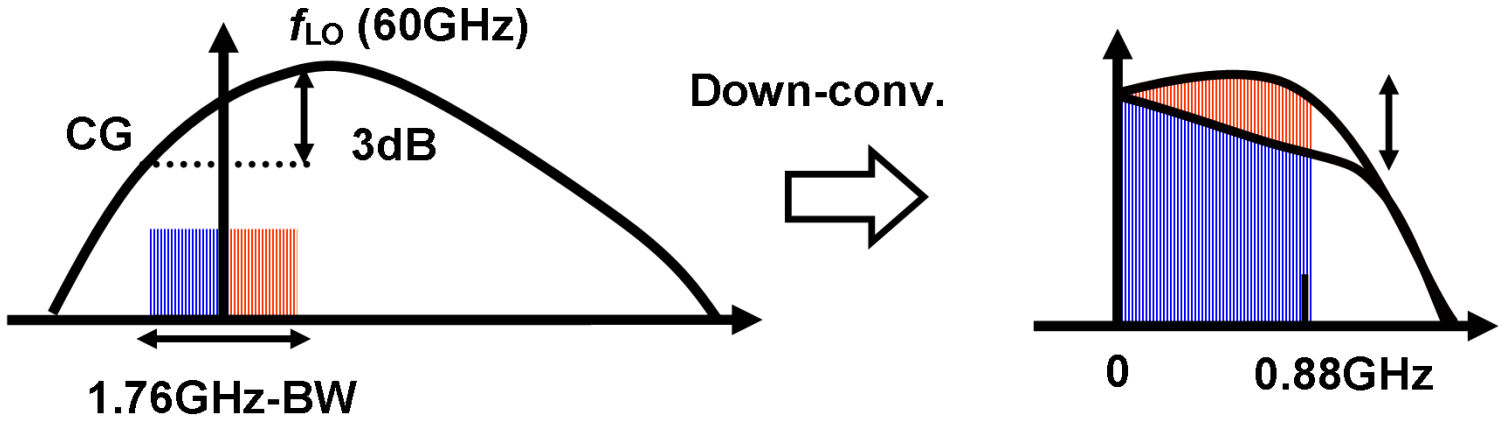
$$D_{rate} = BW \log_2\left(1 + \frac{S}{N}\right)$$

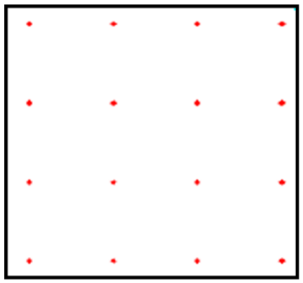
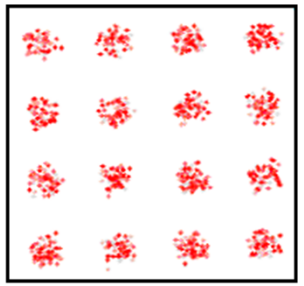
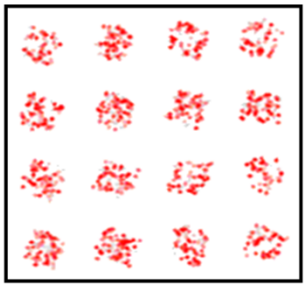
Wider bandwidth
- **Multi-cascaded amplifier**
- **Passive mixer circuit**

Higher SNR
- **Injection locked I/Q oscillator**
- **7 bit ADC**

Effect of the gain flatness

Poor gain flatness makes ISI (Inter Symbol Interference) due to different gain for plus frequency and minus frequency.



Gain Flatness	0dB	2dB	3dB
BER	~0	1.3e-5	3e-3
Constellation			

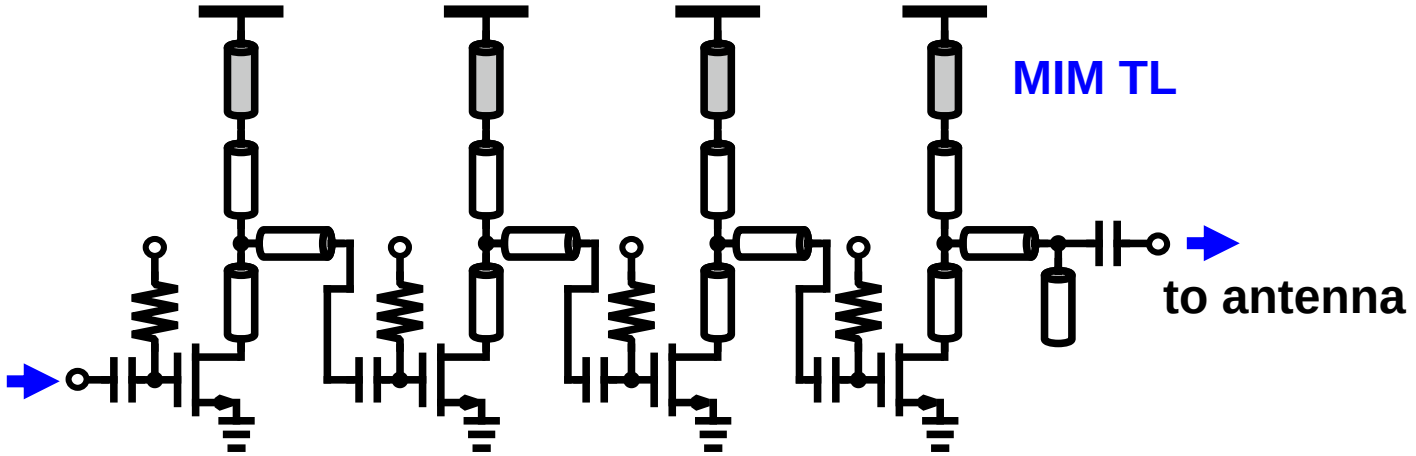
Multi-cascaded RF amplifiers

Multi-cascaded RF amplifier can increase the gain flatness due to the distributed resonant frequencies.

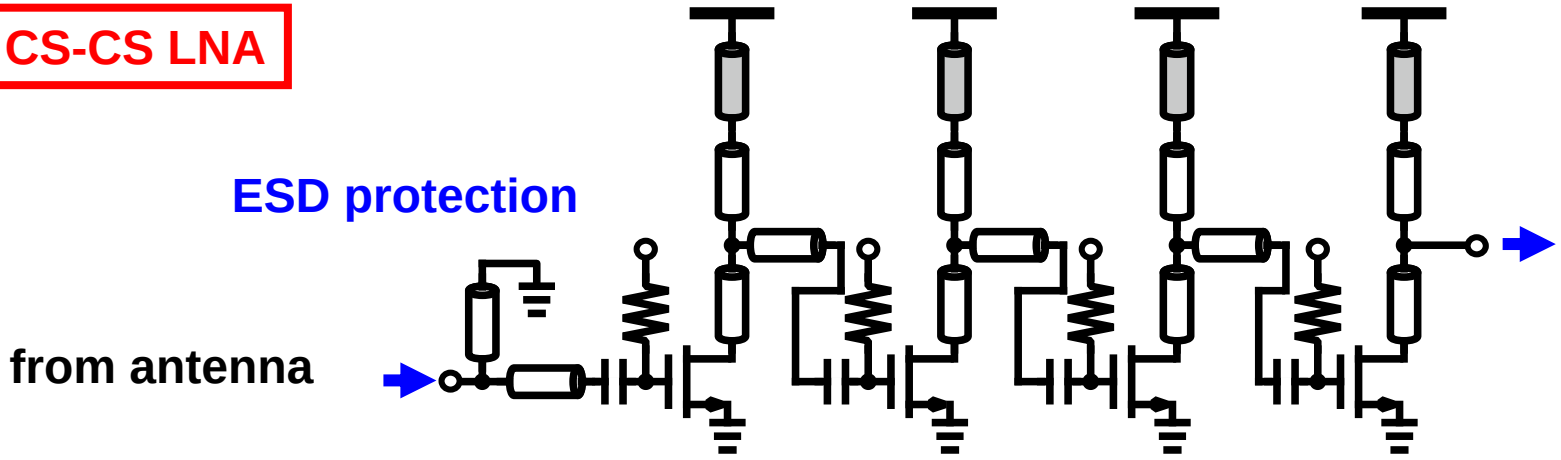
4-stage PA

MIM TL

TL



4-stage CS-CS LNA

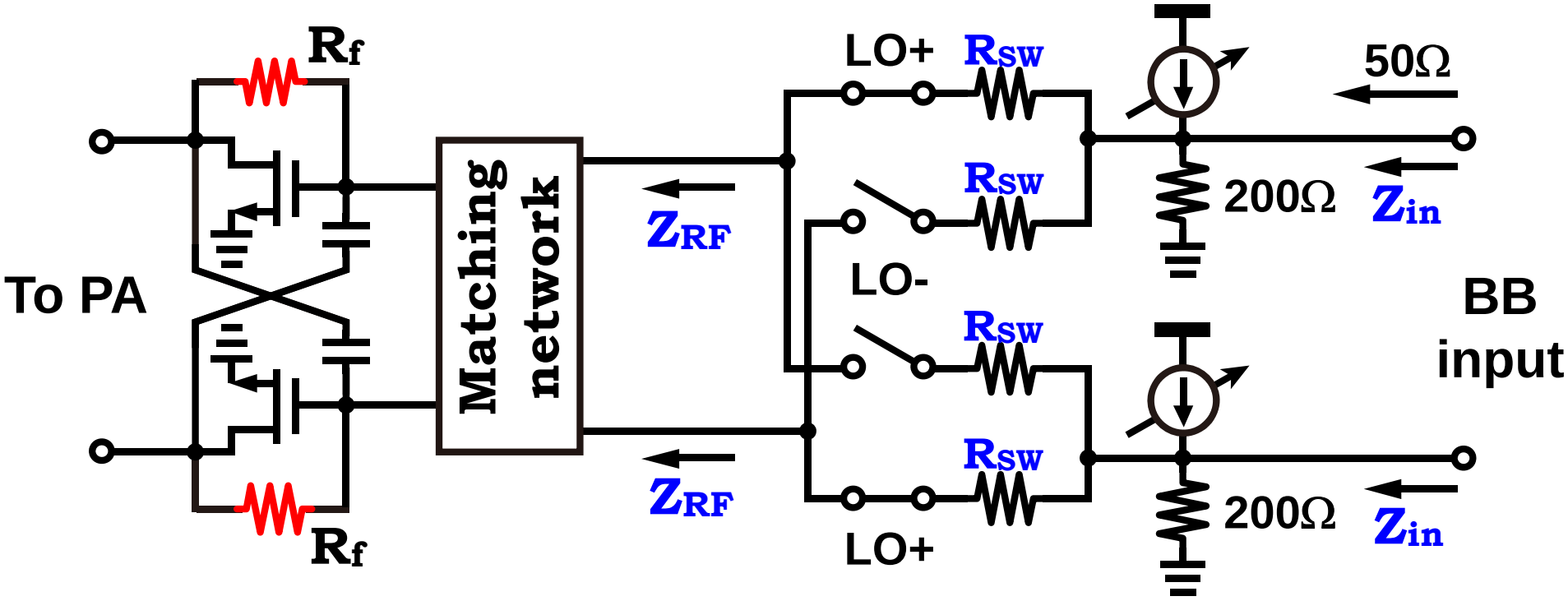


Mixer circuit in TX

TOKYO TECH Pursuing Excellence

Passive mixer with resistive feedback RF amplifier can realize Widely flat impedance, rather than LC impedance matching method.

$$Z_{in}(\omega) \approx 200\Omega \,//\, \left\{ R_{SW} + \frac{8}{\pi^2} \mathrm{Re}\left[Z_{RF}(\omega_{LO}) \right] \right\}$$

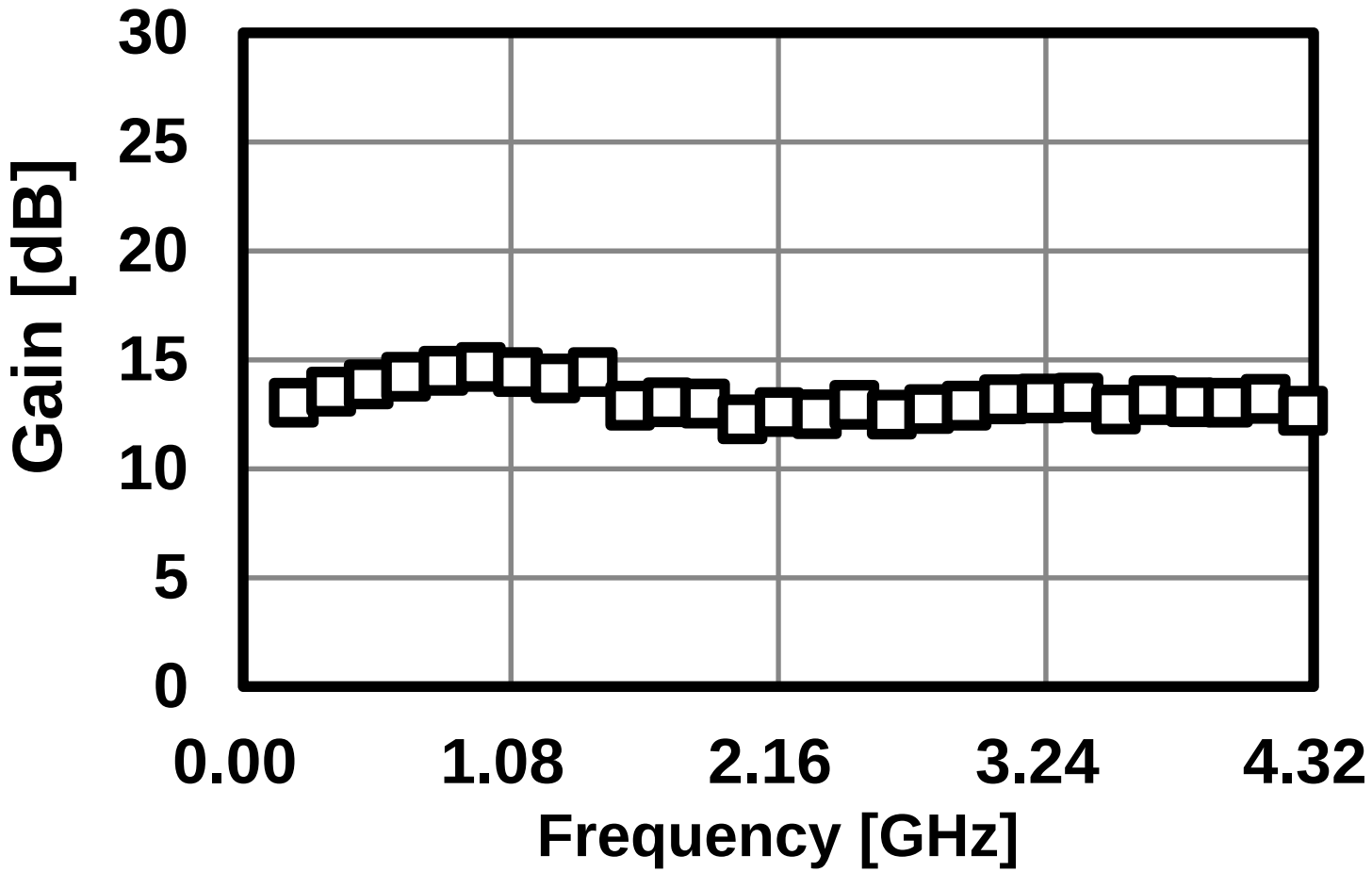


Matsuzawa & Okada Lab.

Measured gain of TX circuit

TOKYO TECH Pursuing Excellence

The gain flatness of 2 dB is attained for the band width of 4 GHz.



Matsuzawa & Okada Lab.

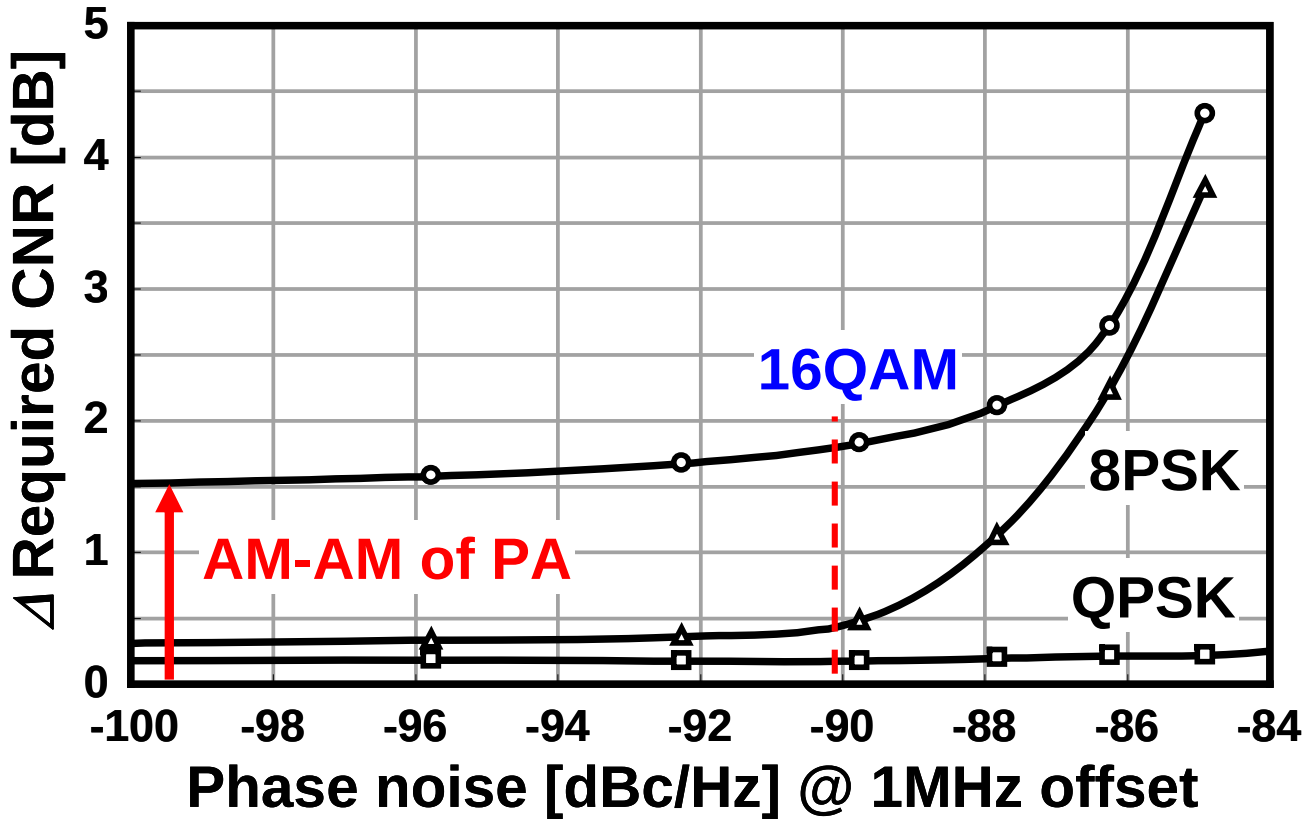
Required phase noise of IQ-VCO for 16QAM

TOKYO TECH Pursuing Excellence

A phase noise of LT. -90dBc/Hz@1MHz is required for 16QAM systems

A reported phase noise of 60GHz IQ VCO is -76dBc/Hz @1MHz at most

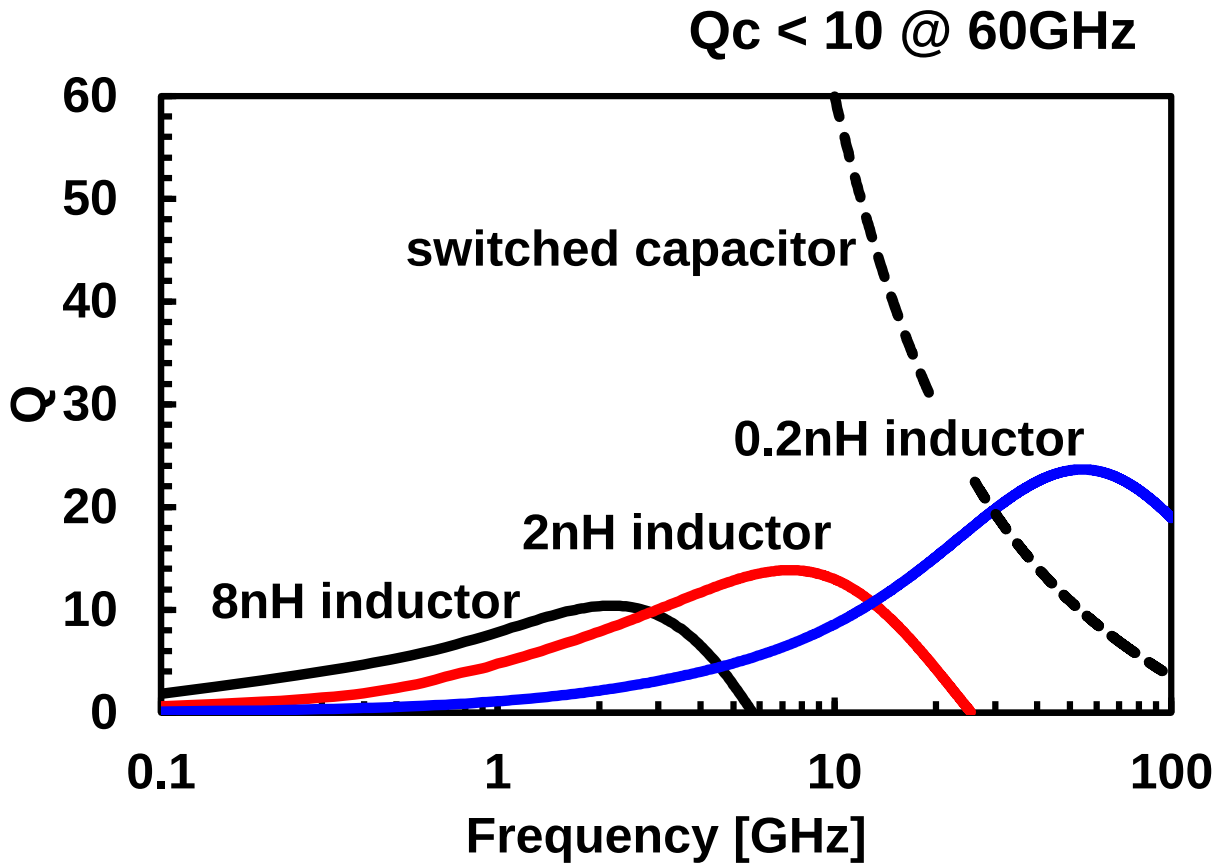
K. Scheir, et al., ISSCC, pp. 494-495,Feb. 2009.



Matsuzawa & Okada Lab.

Q of inductors and capacitor

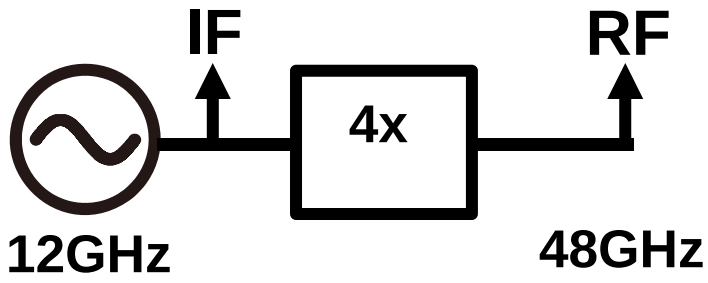
Q of capacitor is rapidly degraded with frequency.
Q of Less than 10 at 60 GHz at most.
→ Low phase noise 60 GHz VCO is hard to be realized.



Frequency Multiplier

TOKYO TECH Pursuing Excellence

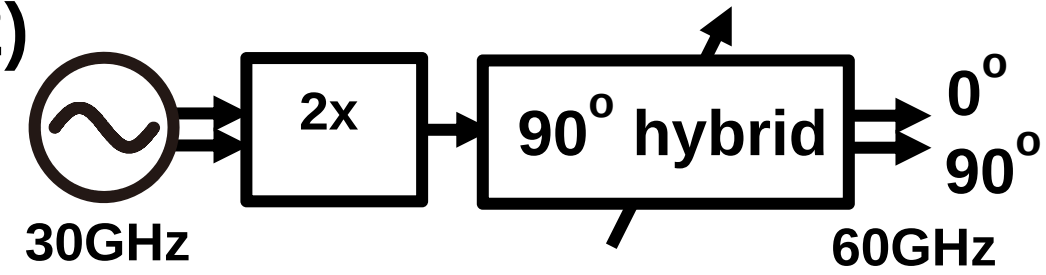
(1)



- for hetero-dyne TRX
- reasonable for PN and FTR

*S. Emami, *et al*., ISSCC 2011

(2)

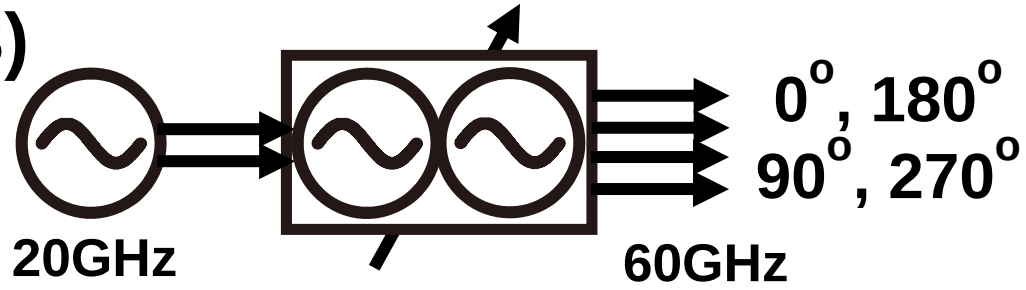


- 30GHz is too high for PN and FTR
- I/Q phase calibration is required.

(20GHz x 3, 15GHz x4 are OK.)

**C. Marcu, *et al*., ISSCC 2009

(3)



- 60GHz QILO***
- good for PN and FTR

***W. Chan, *et al*., ISSCC 2008

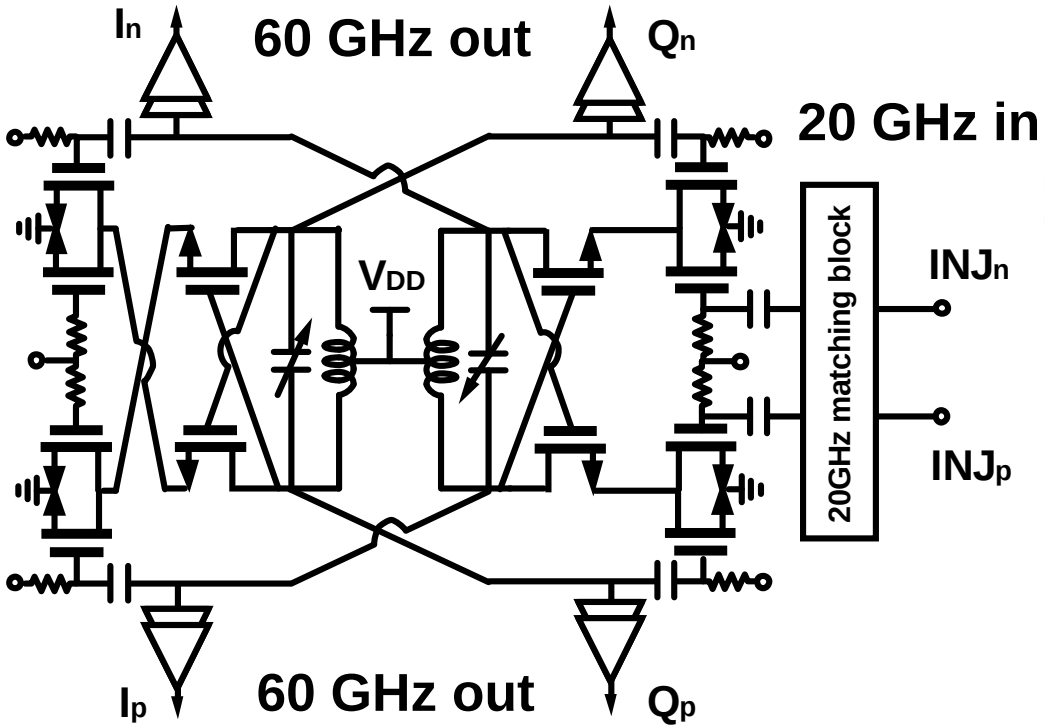
Matsuzawa & Okada Lab.

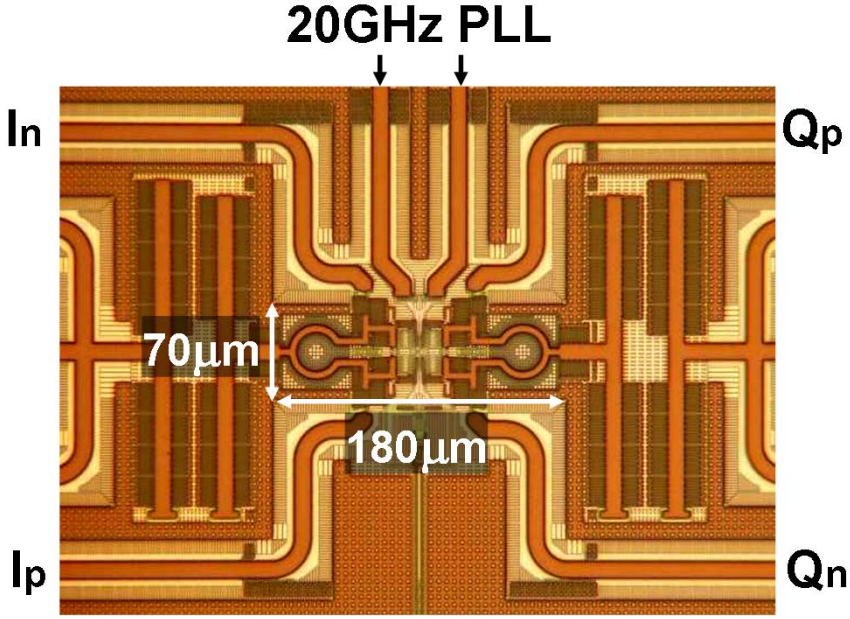
Injection locked 60GHz I/Q VCO

TOKYO TECH Pursuing Excellence

We have developed the injection locked 60 GHz I/Q VCO

The 60 GHz quadrature VCO is injected by 20 GHz PLL





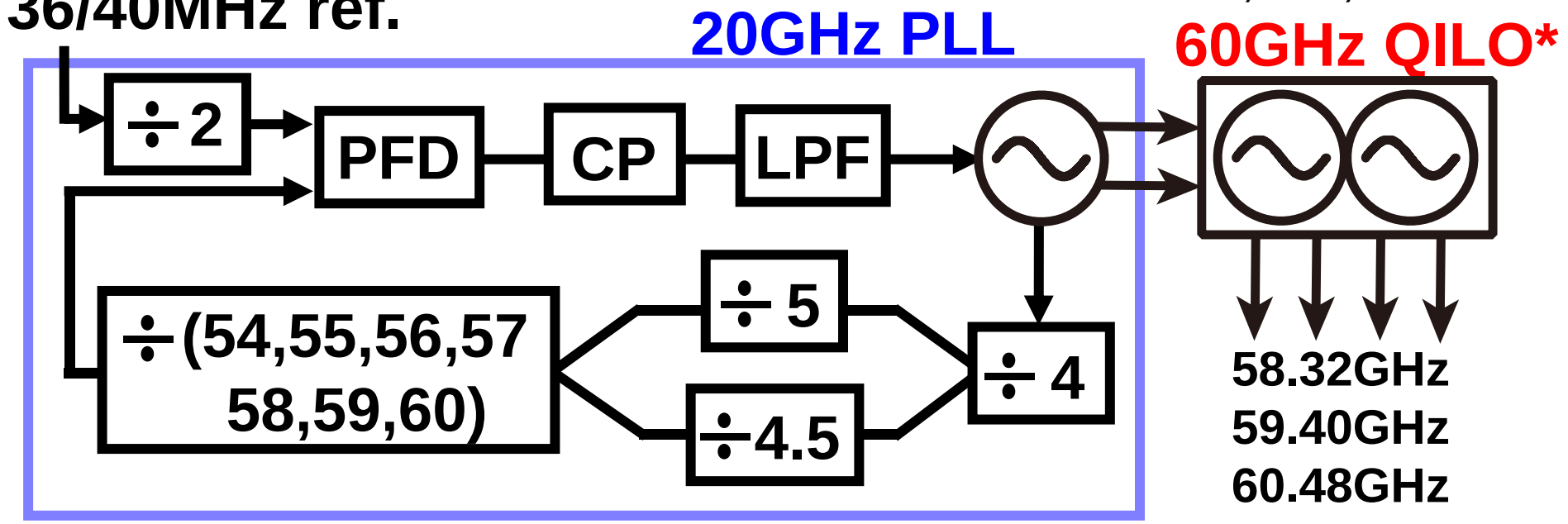
A. Musa, K. Okada, A. Matsuzawa., in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

Matsuzawa & Okada Lab.

60GHz Quadrature LO Design

TOKYO TECH Pursuing Excellence

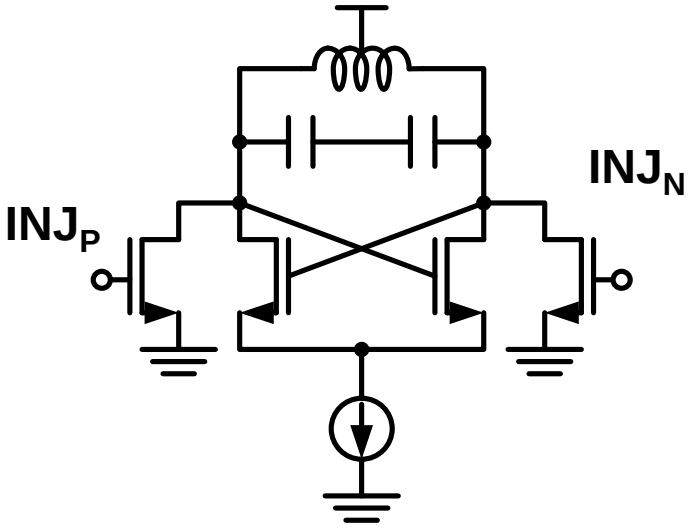
*K. Okada, *et al*., ISSCC 2011



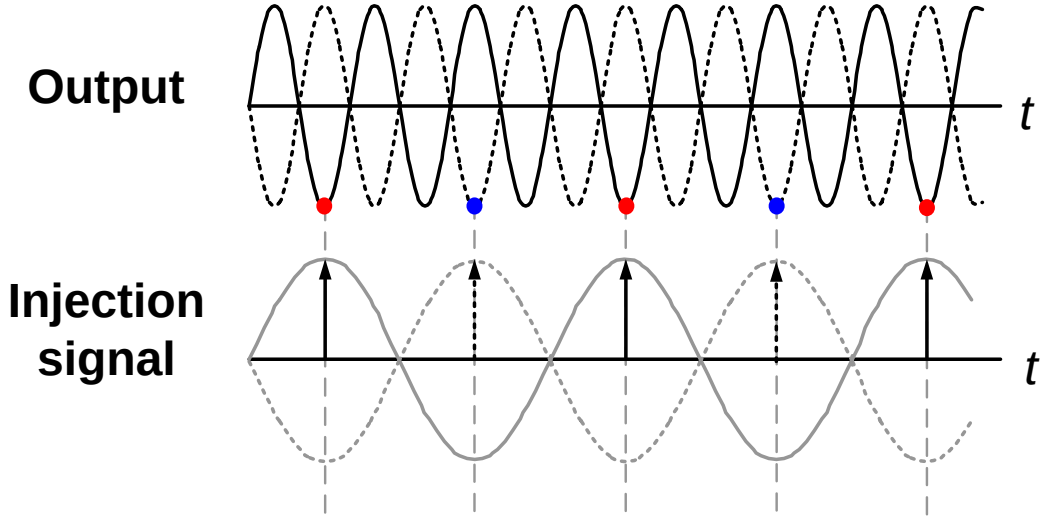
- 20GHz PLL: 64mW
- 60GHz QILO: 18mW(TX)&15mW(RX)
- QILO frequency range: 58-66GHz
- Phase noise improvement by injection locking*
- -96.5dBc/Hz @ 1MHz at 61.56GHz

Injection locking technique

Injection locking technique is a very important circuit technique for high frequency signal generation and frequency divider. Phase noise of the oscillator is mandated by the injection signal.



parallel injection



Phase noise $PN_{\mathrm{ILO}} = PN_{\mathrm{INJ}} + 20\log(N)$

N: Multiple number

9.5dB @ N=3

Locking frequency range $f_L \approx \frac{f_o}{2Q} \cdot \frac{I_{inj}}{I_{OSC}}$

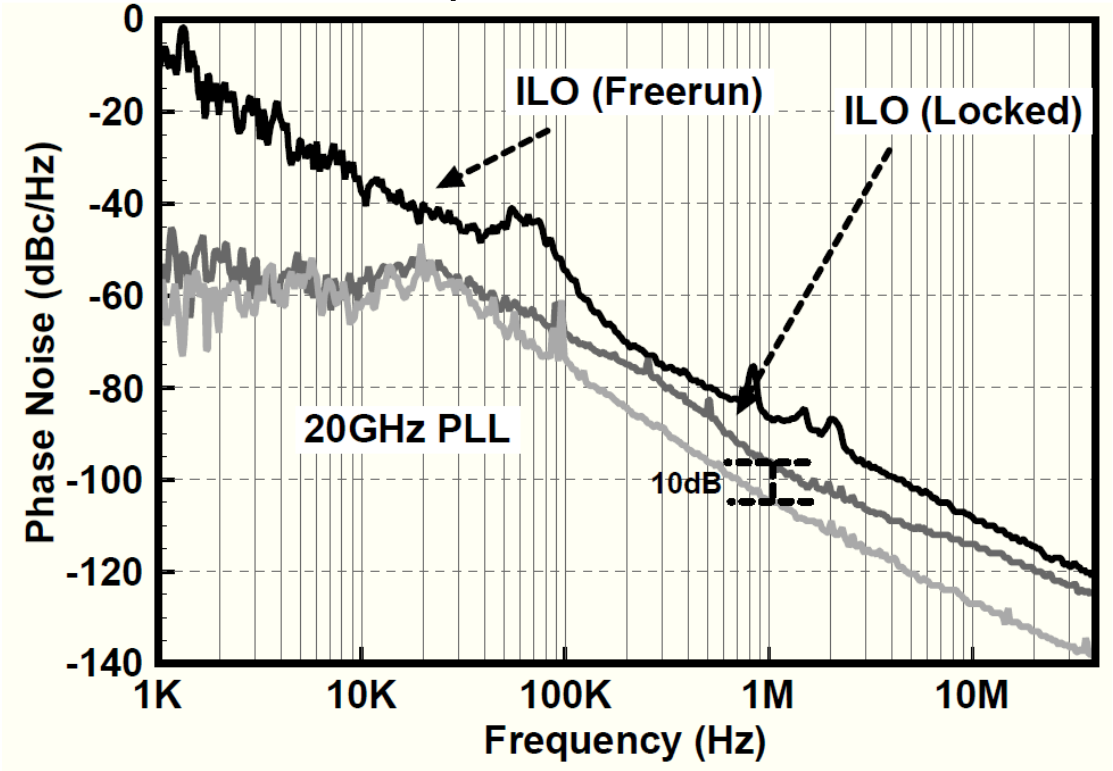
Low phase noise can be realized

TOKYO TECH Pursuing Excellence

Quadrature injection locked 60GHz oscillator with 20GHz PLL
Low phase noise of -96dBc/Hz @1MHz. Previous one is -76dBc/Hz@1MHz

Best phase noise is achieved.

58-63GHz, -96dBc/Hz-1MHz offset



A. Musa, K. Okada, A. Matsuzawa., in A-SSCC Dig. Tech. Papers, pp. 101–102, Nov. 2010.

Matsuzawa & Okada Lab.

TOKYO TECH
Pursuing Excellence

Basic Design Method for 60GHz

CMOS RF Circuits

Matsuzawa & Okada Lab.

Gain and Noise; f_{max} and f_T

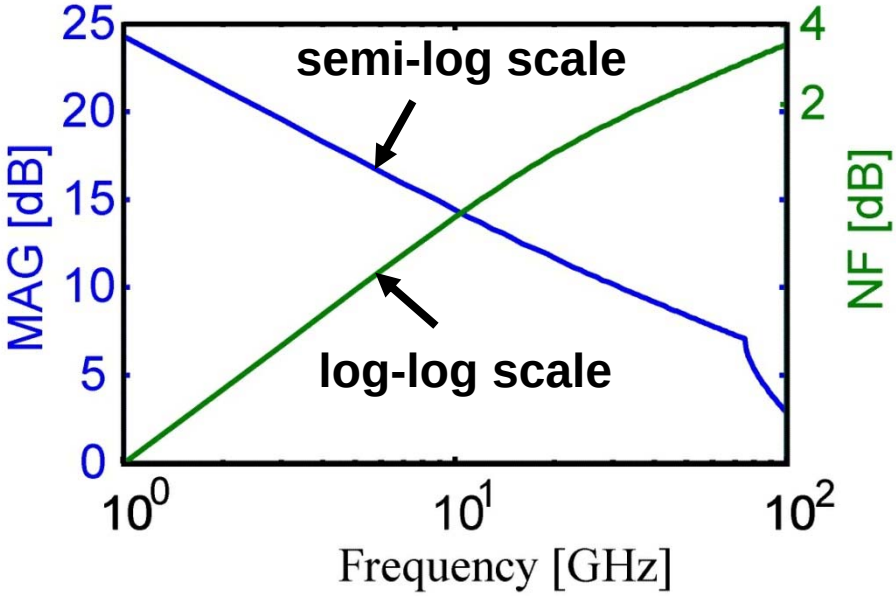
Gain and noise are mainly determined by f_{max} and f_T of Transistor

☹ **Lower gain**

- ☹ **MAG is inversely proportional to the logarithm of the operating frequency f_c.**

☹ **Higher noise**

- ☹ **NF_{min} is proportional to the operating frequency f_c.**



65nm NMOS

W_f=2.5μm, N_f=32, V_{gs}=0.8V and V_{ds}=0.8V.

$$G_{\max} \approx \frac{f_{\max}}{f_c}$$

$$NF_{\min} \approx 1 + \left(\frac{f_c}{f_T}\right)\sqrt{1.3 g_m \left(R_g + R_s\right)}$$

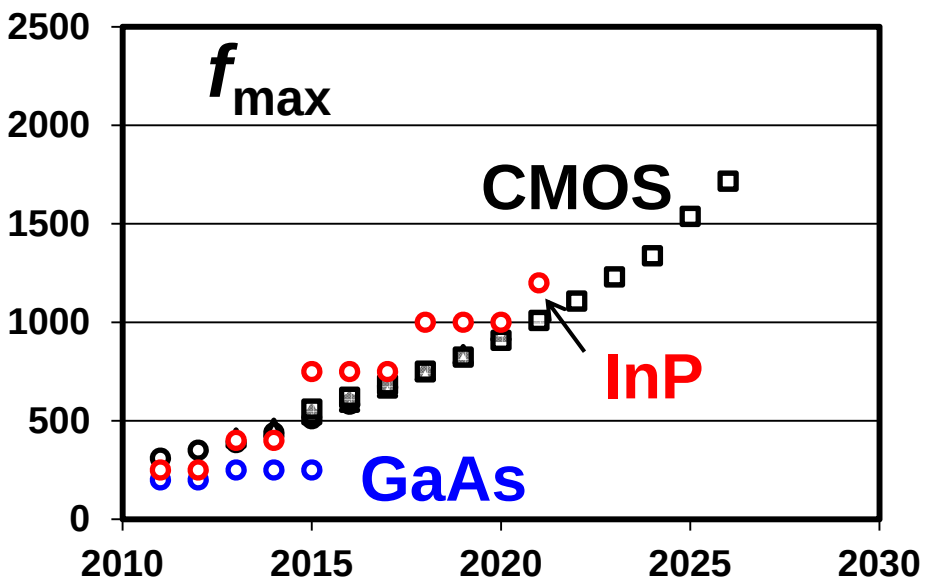
Basic RF performances

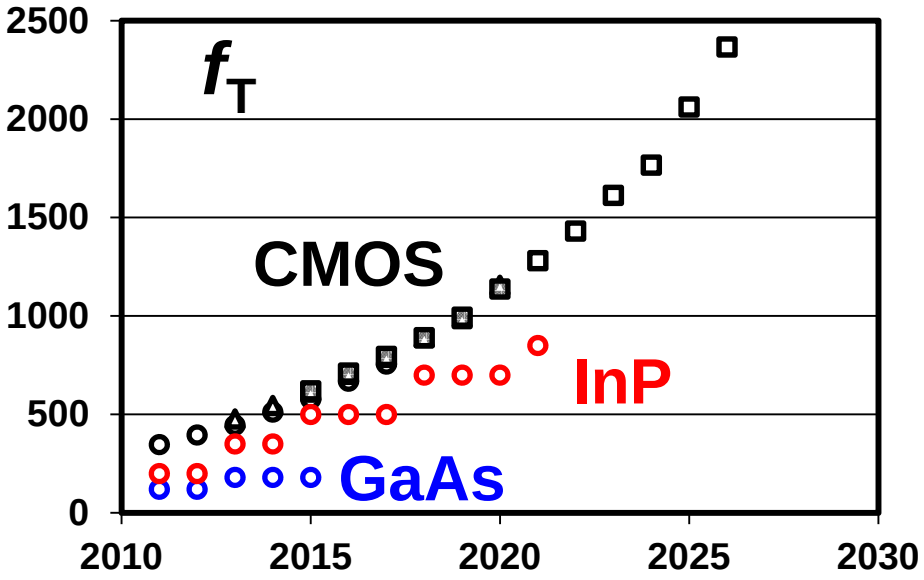
TOKYO TECH Pursuing Excellence

f_{max} and f_T of MOS transistor will increase continuously.
Gain and NF will be improved by using future CMOS technology.

$$G_{\max} \approx \frac{f_{\max}}{f_c}$$

$$NF_{\min} \approx 1 + \left(\frac{f_c}{f_T}\right)\sqrt{1.3 g_m \left(R_g + R_s\right)}$$





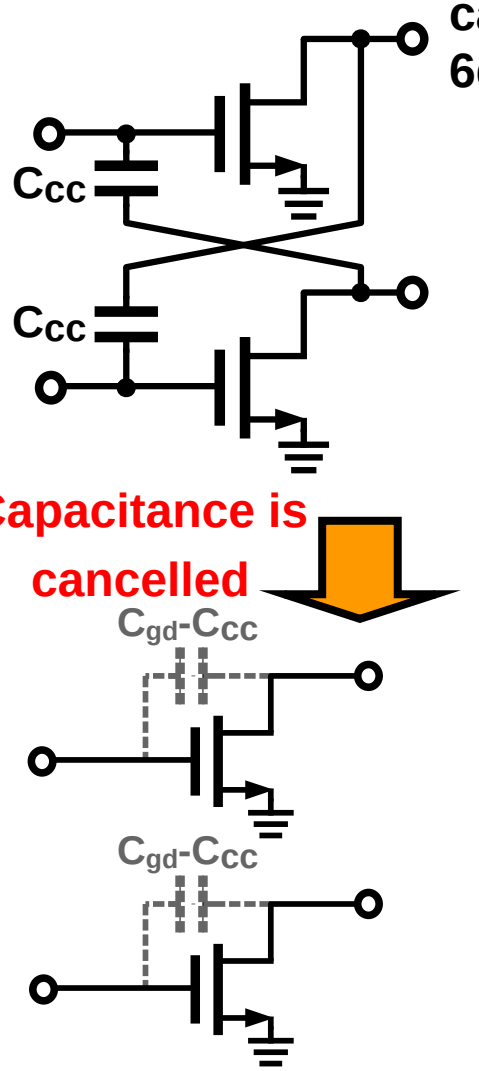
- ○ Bulk CMOS
- △ Ultra-Thin-Body Fully-Depleted (UTB FD) SOI
- □ Multi-Gate MOSFETs

ITRS RFAMS 2011.

Cross coupled feedback capacitors

TOKYO TECH Pursuing Excellence

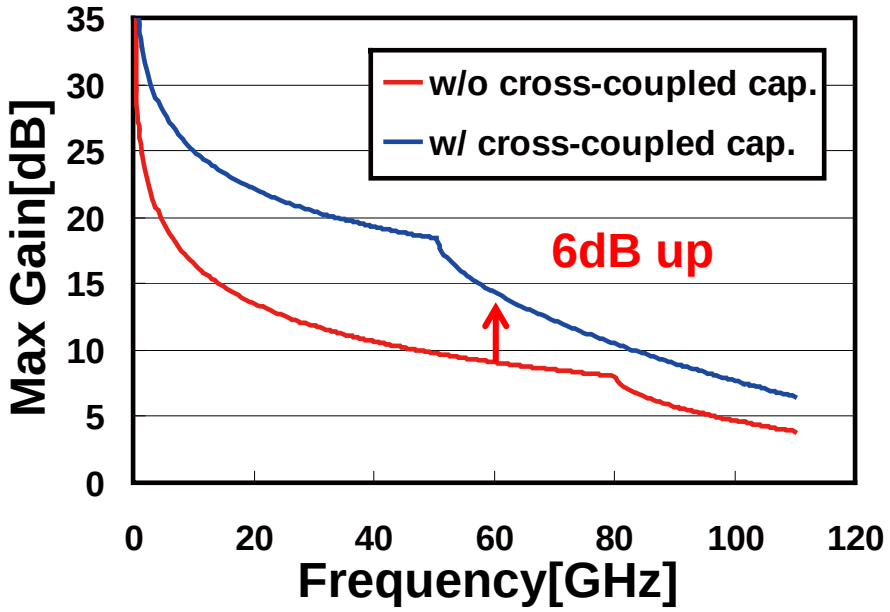
Differential circuit



Cross coupled feedback capacitors in a differential circuit can reduce the effective capacitance to increase the gain of 6dB at 60GHz.

$$f_{\max} = \frac{f_T}{2\sqrt{R_g g_m C_{gd}/(C_{gs}+C_{gd}) + (R_g + r_{ch} + R_s) g_{ds}}}$$

This term is reduced



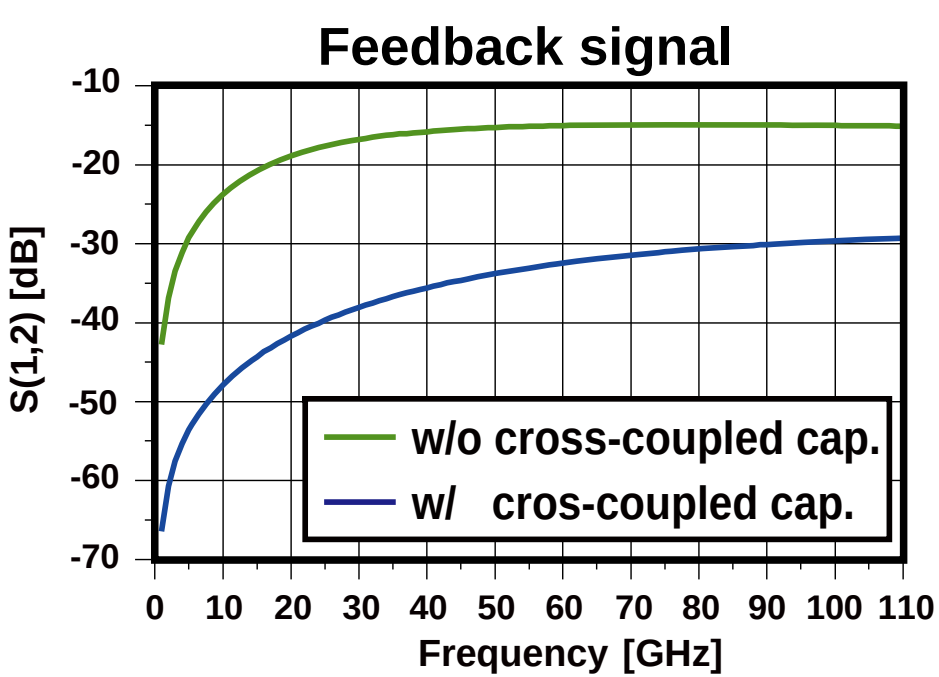
Y. Natsukari, et al., VLSI Circuits, Dig. Tech. Papers, pp. 252–253, June 2009.

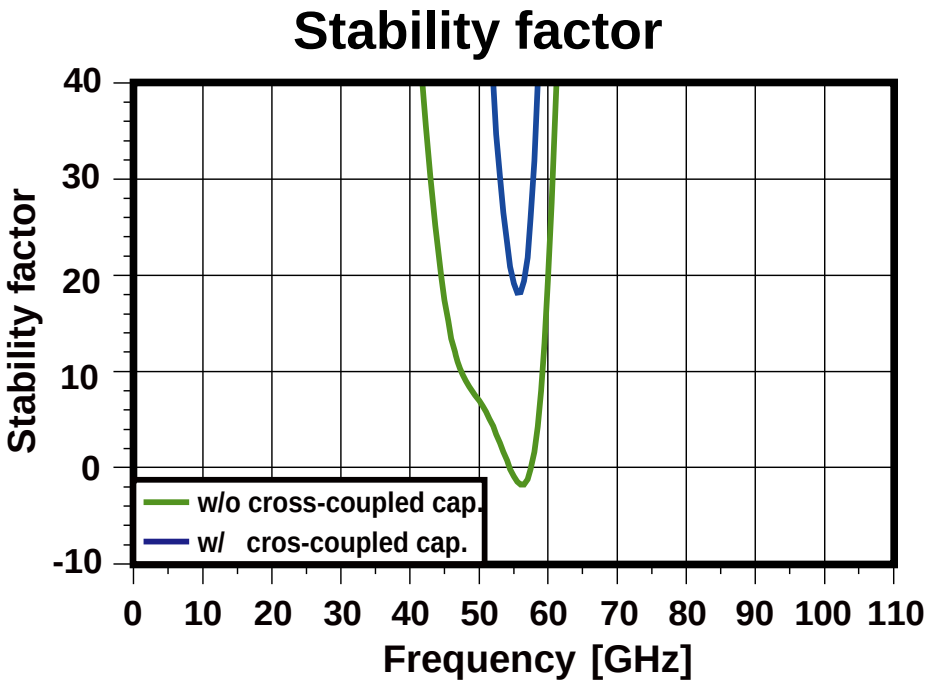
W. L. Chan, et al., ISSCC. Tech. Dig., pp. 380–381, Feb. 2009.

Feedback signal and stability

TOKYO TECH Pursuing Excellence

Feedback signal is suppressed by the cross coupled capacitors and this increase the stability of amplifier.

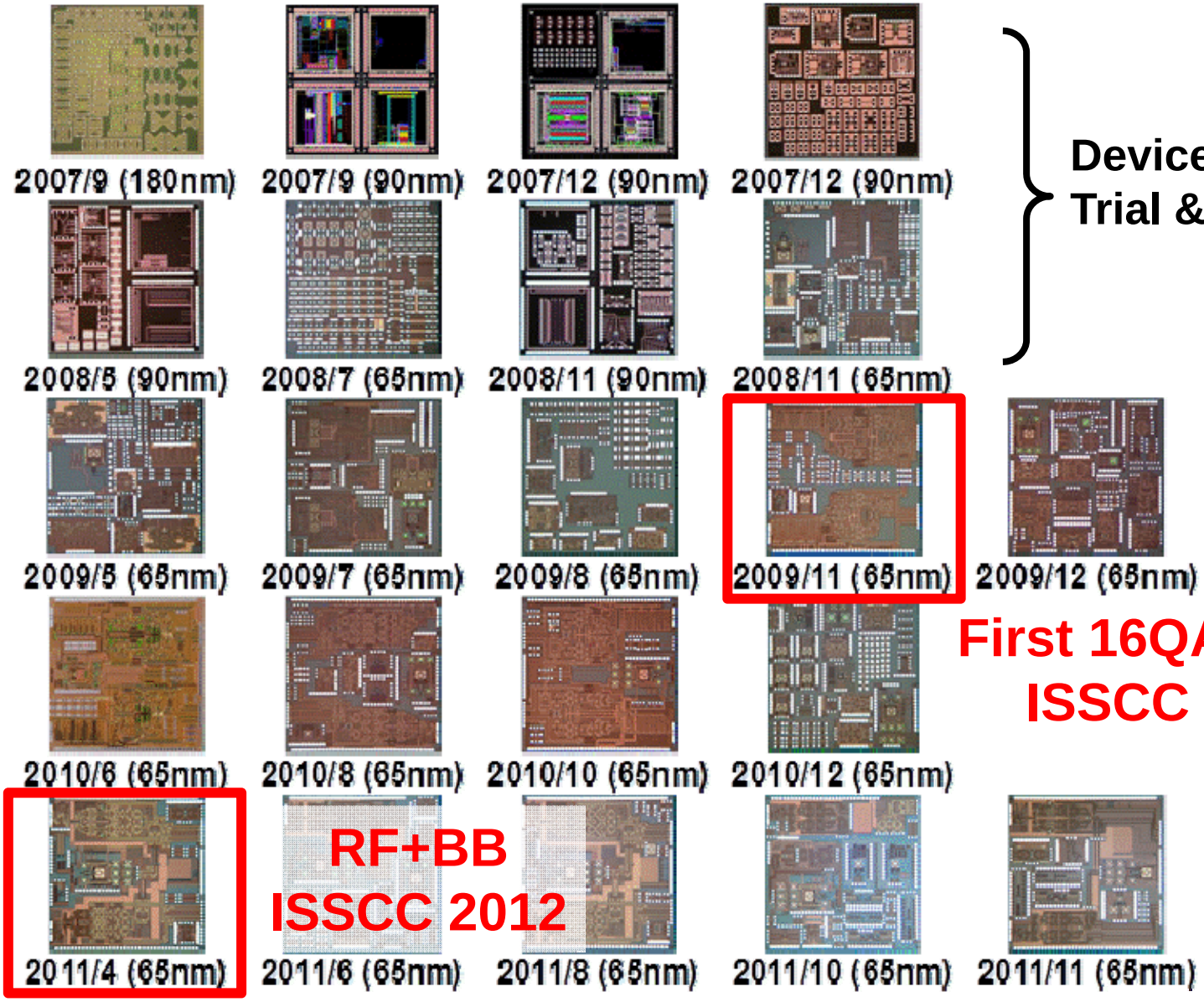




Matsuzawa & Okada Lab.

Development history of 60GHz circuits

TOKYO TECH Pursuing Excellence



Device modeling
Trial & Error

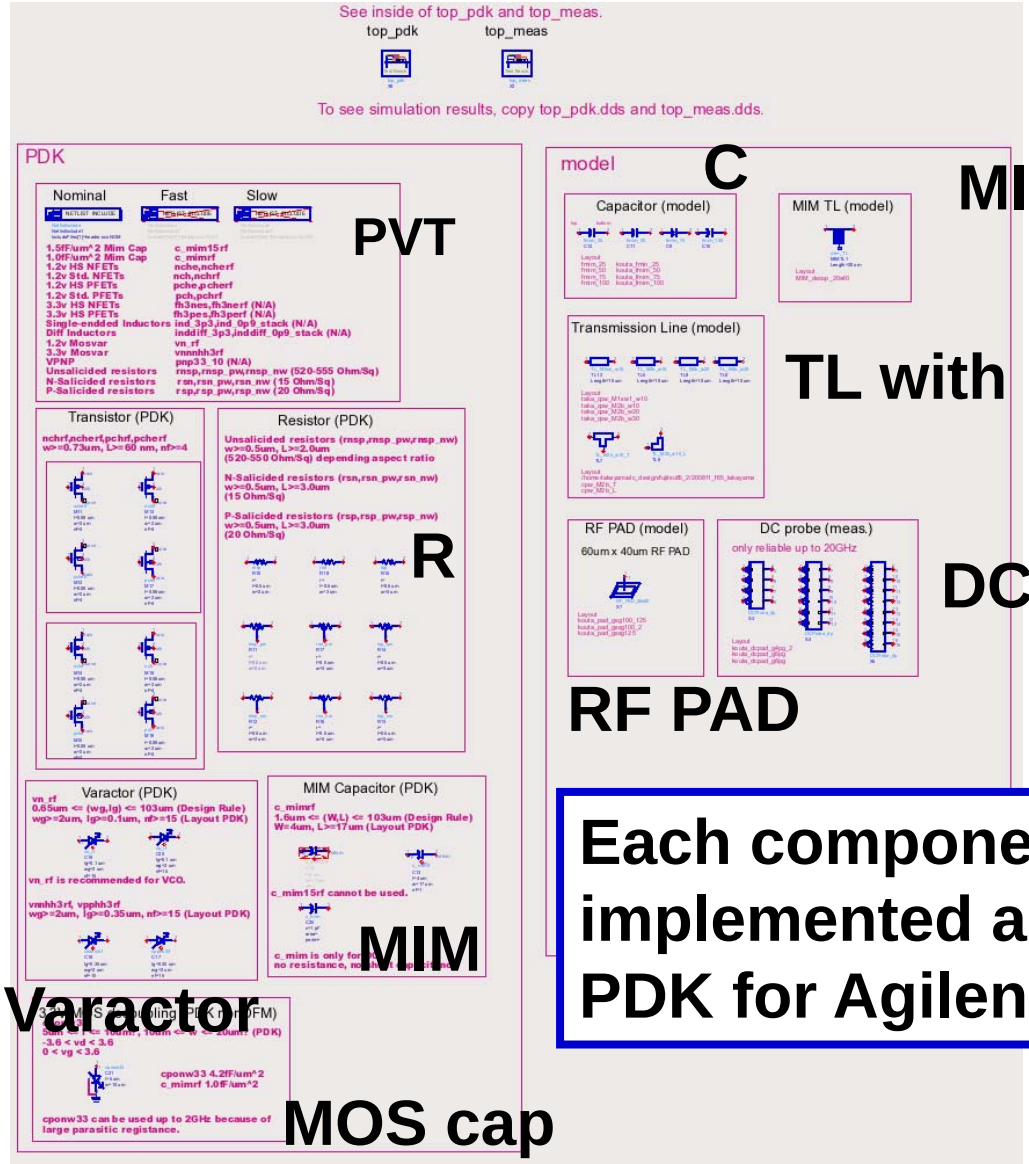
First 16QAM TRx
ISSCC 2011

RF+BB
ISSCC 2012

Matsuzawa & Okada Lab.

In-house PDK

TOKYO TECH Pursuing Excellence



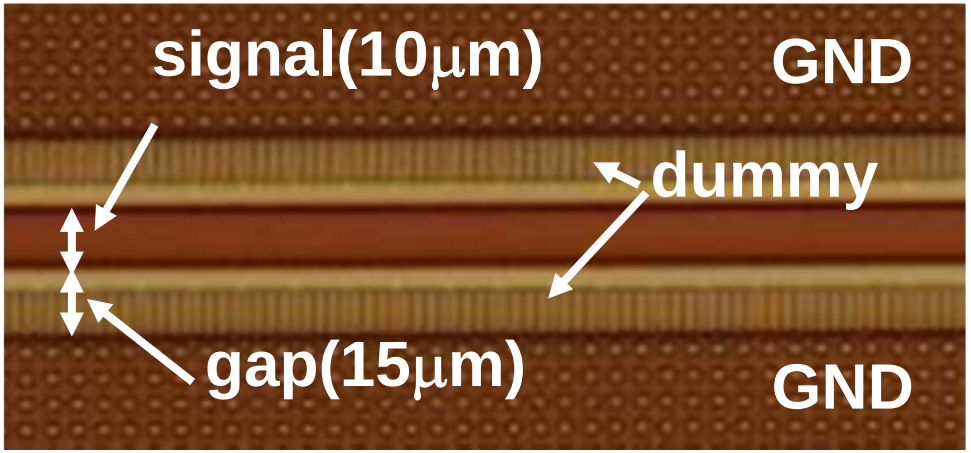
Each component is implemented as an in-house PDK for Agilent ADS.

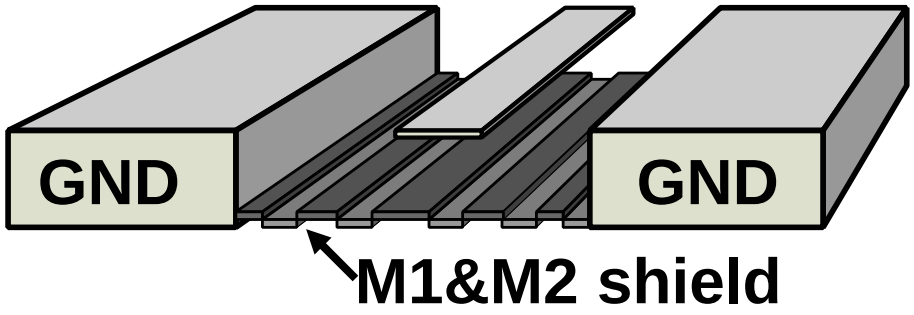
Key technology: low loss TR line

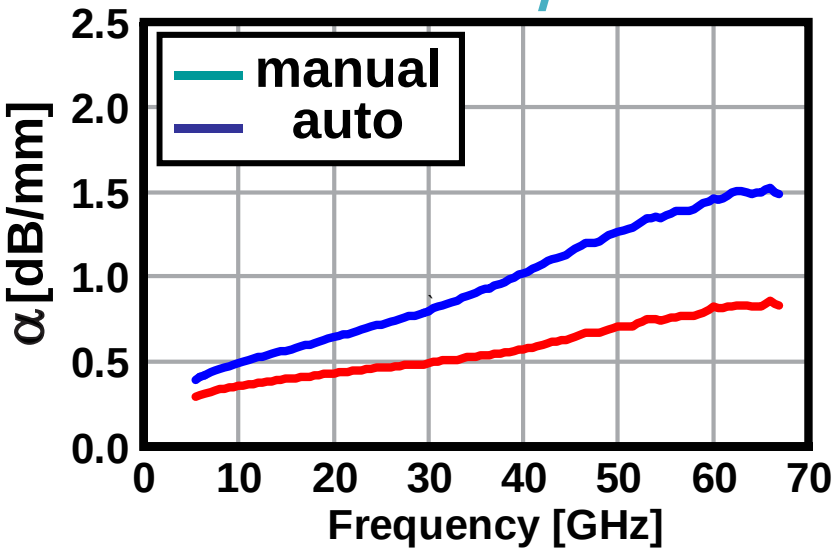
TOKYO TECH Global Excellence

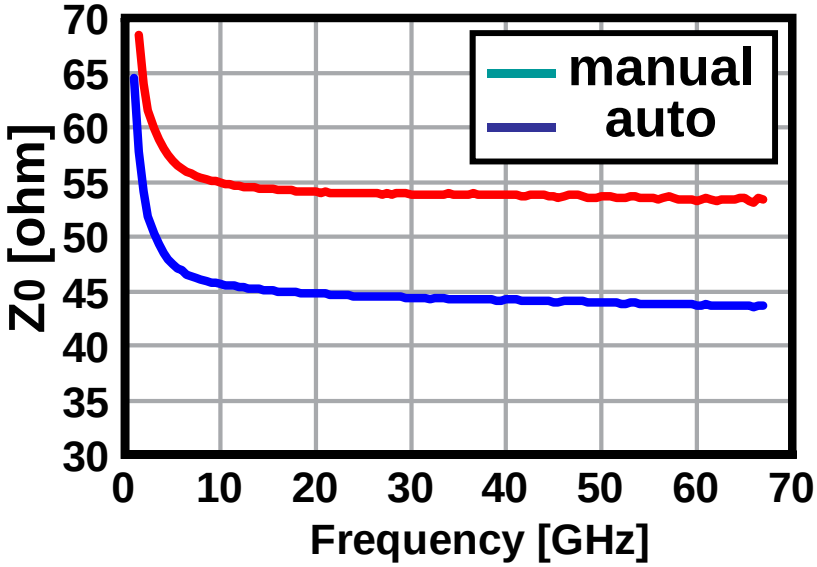
Optimized parameter and manually-placed dummy metal realize low loss transmission line.

- **0.8dB/mm**
- **Manually-placed dummy metal**







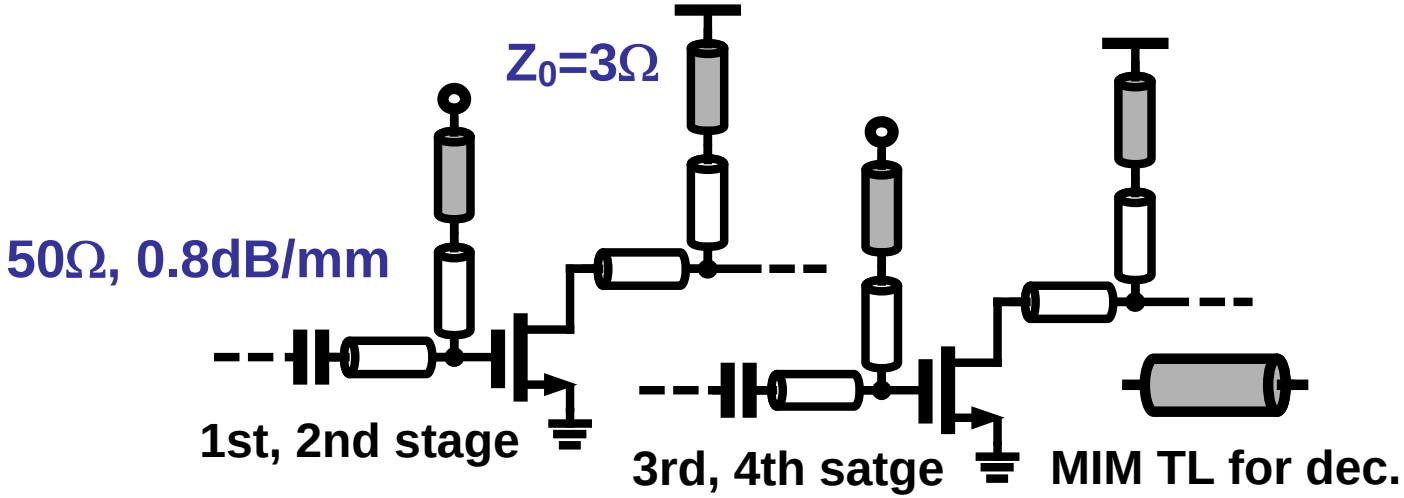


Matsuzawa & Okada Lab.

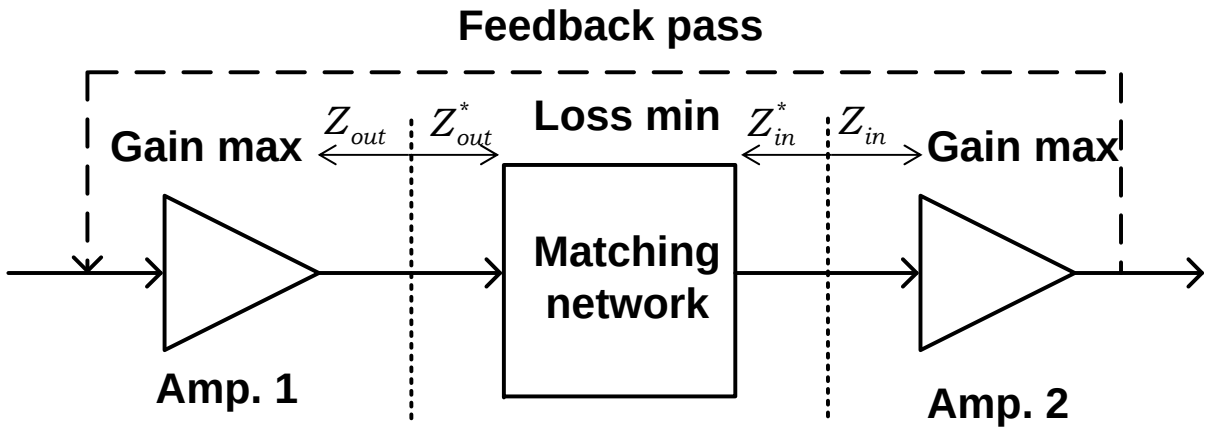
Basic amplifier design

TOKYO TECH Pursuing Excellence

Amplifier design;
accurate sizing, biasing, impedance matching and decoupling.



A several GHz oscillation will occur, if the feedback passes are made.

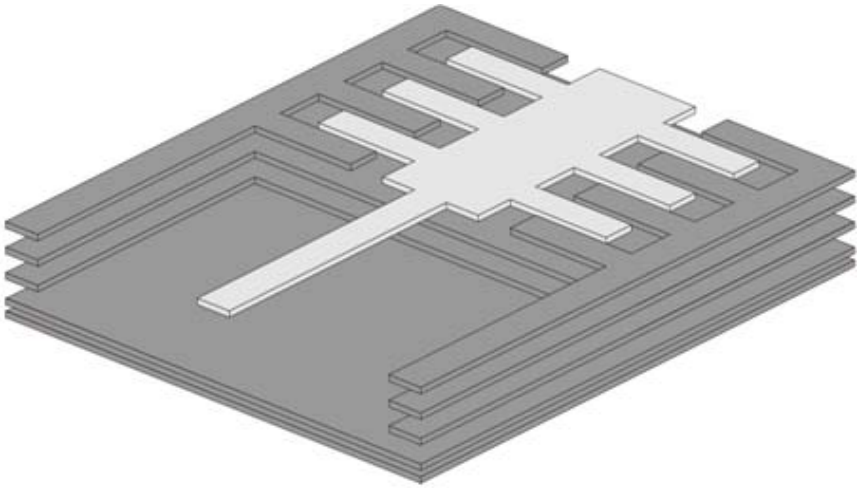


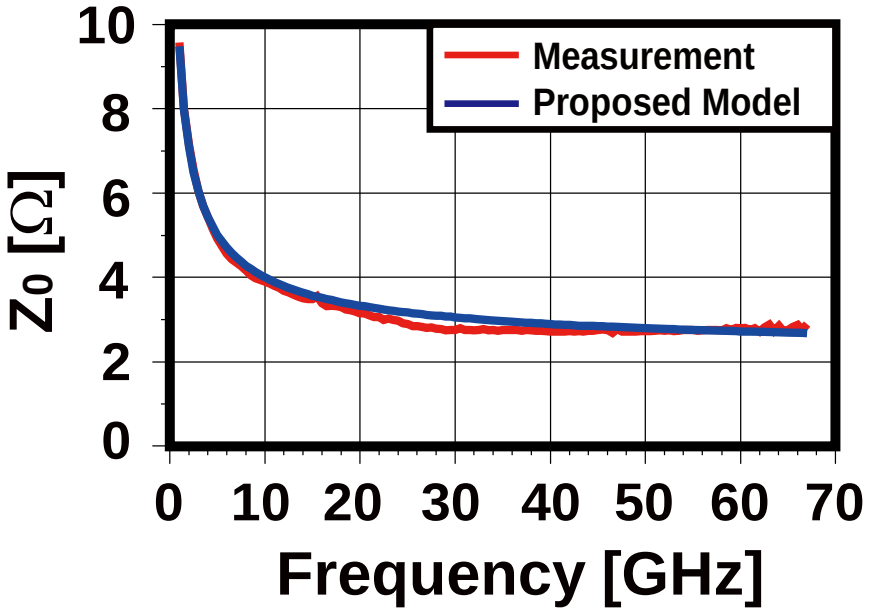
Matsuzawa & Okada Lab.

Decoupling capacitor

TOKYO TECH Pursuing Excellence

A decoupling capacitor has been developed using MIM capacitor with distributed structure to prevent a resonance,
Which occurs, if used a conventional capacitor structure.
A very low impedance of 3 ohm is realized.



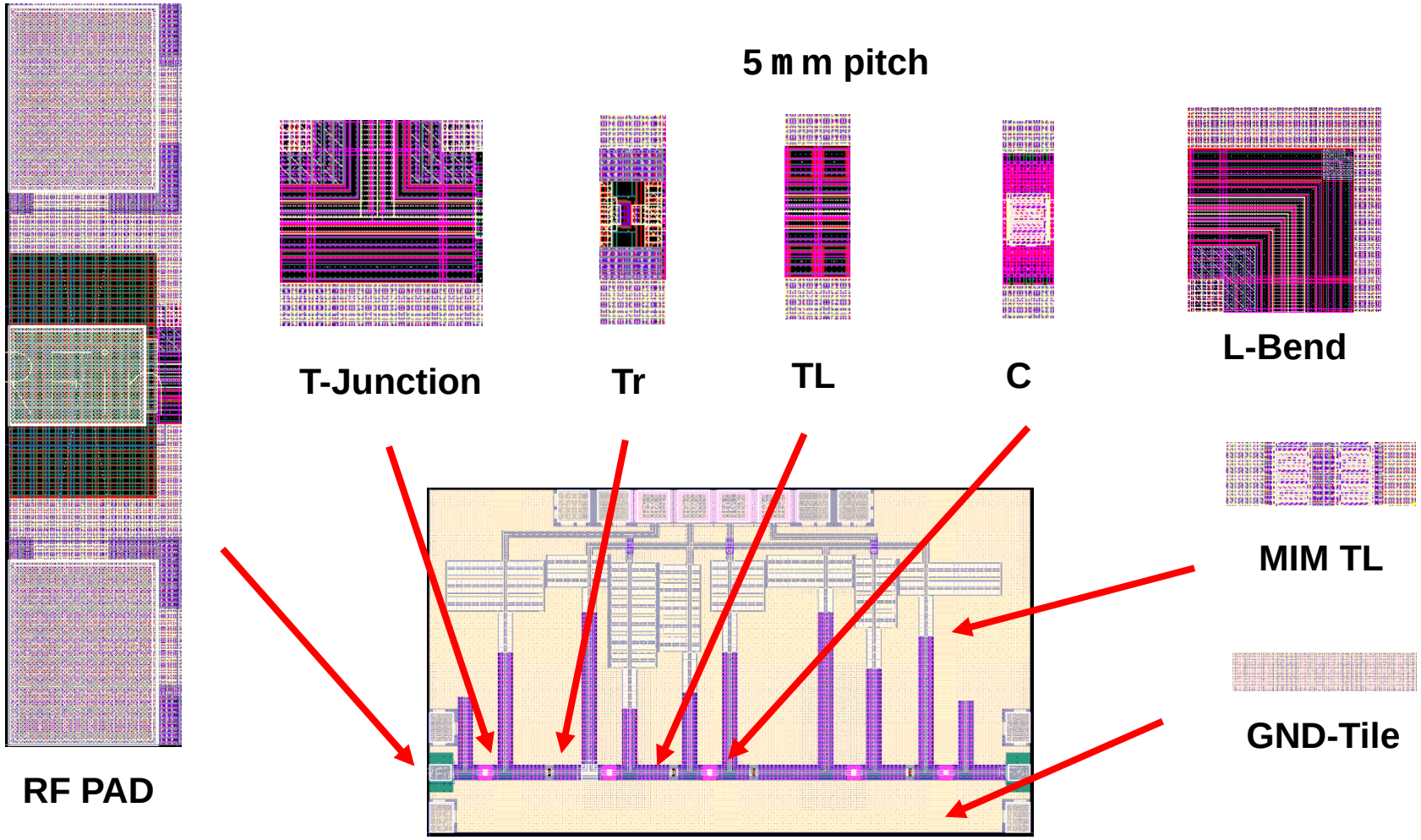


Matsuzawa & Okada Lab.

Tile-based layout method

TOKYO TECH Pursuing Excellence

Each component is previously measured and modeled.
The same layout is utilized to maintain modeling accuracy.

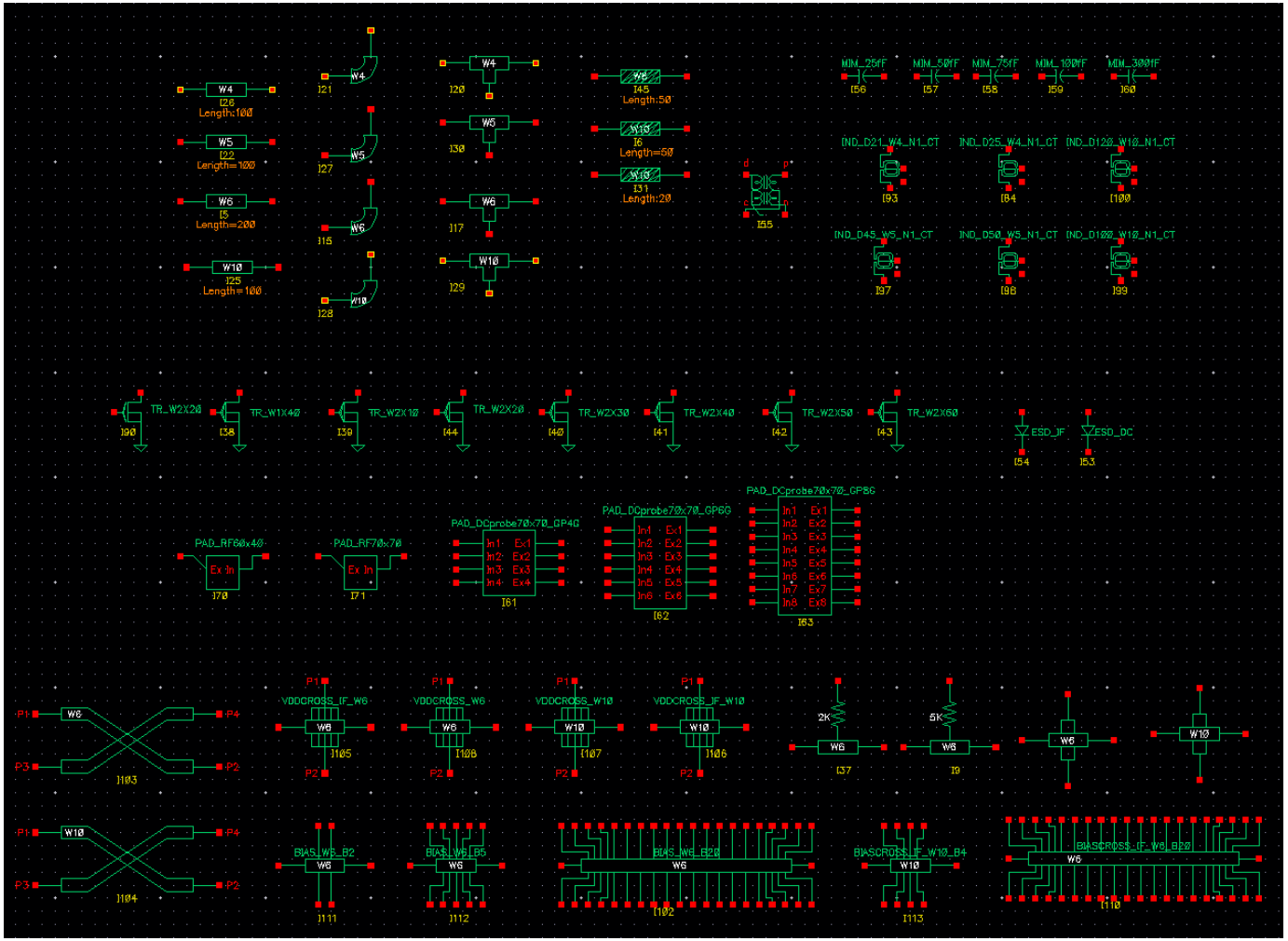


Matsuzawa & Okada Lab.

In-house PDK

TOKYO TECH Pursuing Excellence

We have developed in-house PDK for 60-GHz circuit design for Virtuoso

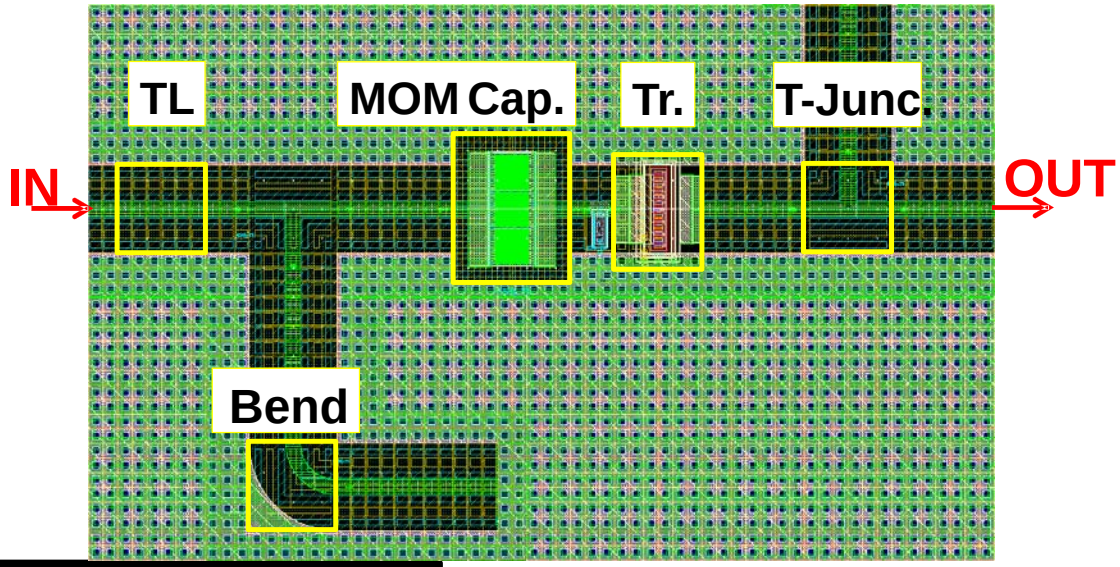


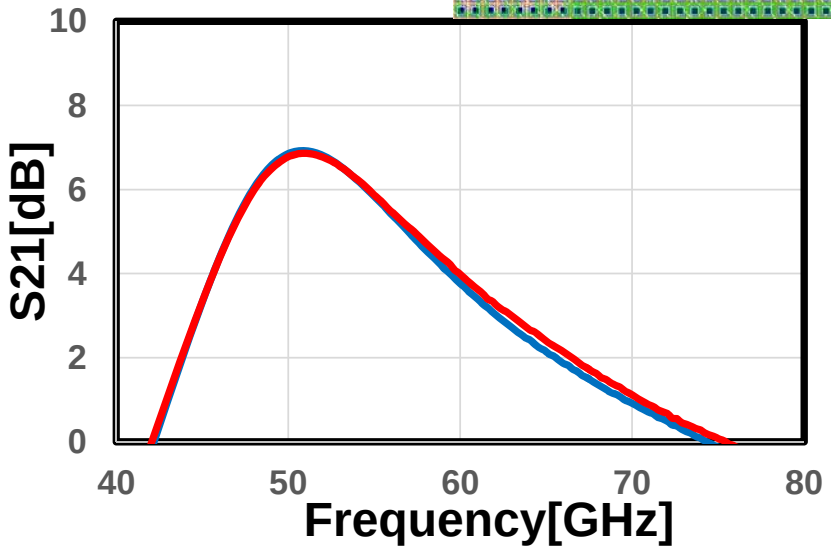
Matsuzawa & Okada Lab.

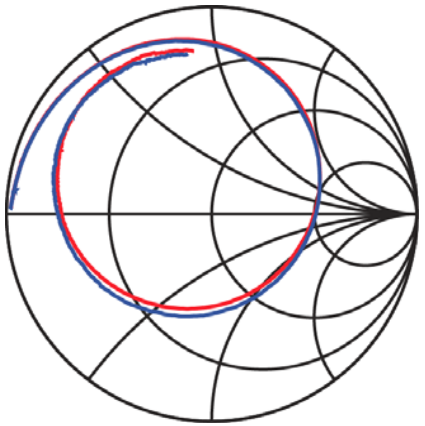
Design Example

TOKYO TECH Pursuing Excellence

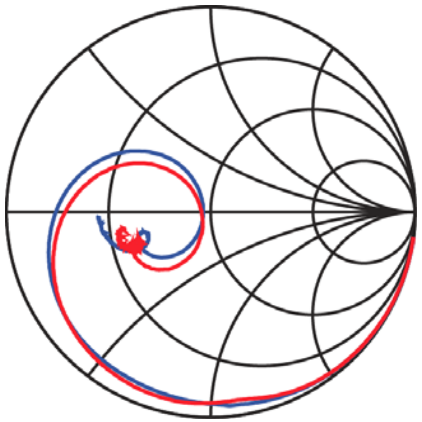
High design accuracy at around 60GHz has been attained







S11



S22

(RED:meas BLUE:sim)

Matsuzawa & Okada Lab.

TOKYO TECH
Pursuing Excellence

High Speed and Low Power ADC

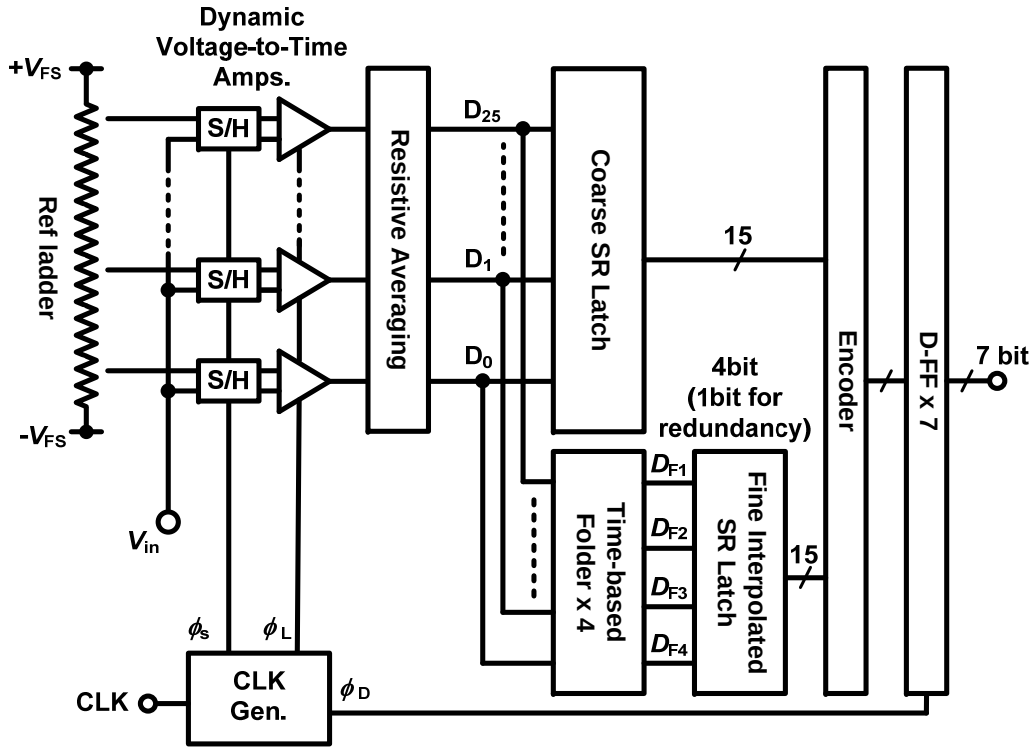
Matsuzawa & Okada Lab.

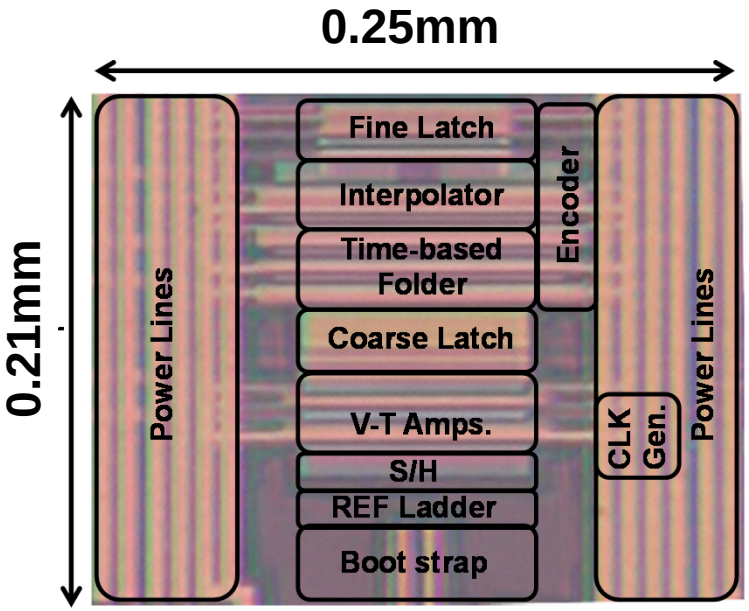
7bit 2.2GSps ADC for 60GHz ABB

TOKYO TECH Pursuing Excellence

- 7bit ADC for the 16QAM modulation
- Convert the voltage difference to the timing difference
- Folding and interpolation are realized by logic gates

M. Miyahara, A. Matsuzawa, ISSCC 2014





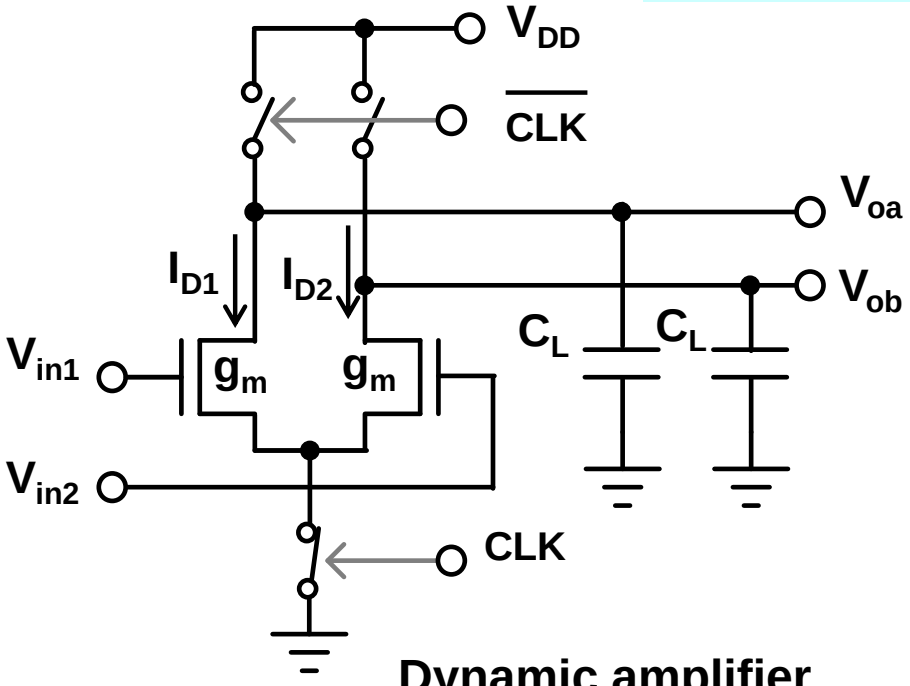
Matsuzawa & Okada Lab.

V to T conversion in dynamic amplifier

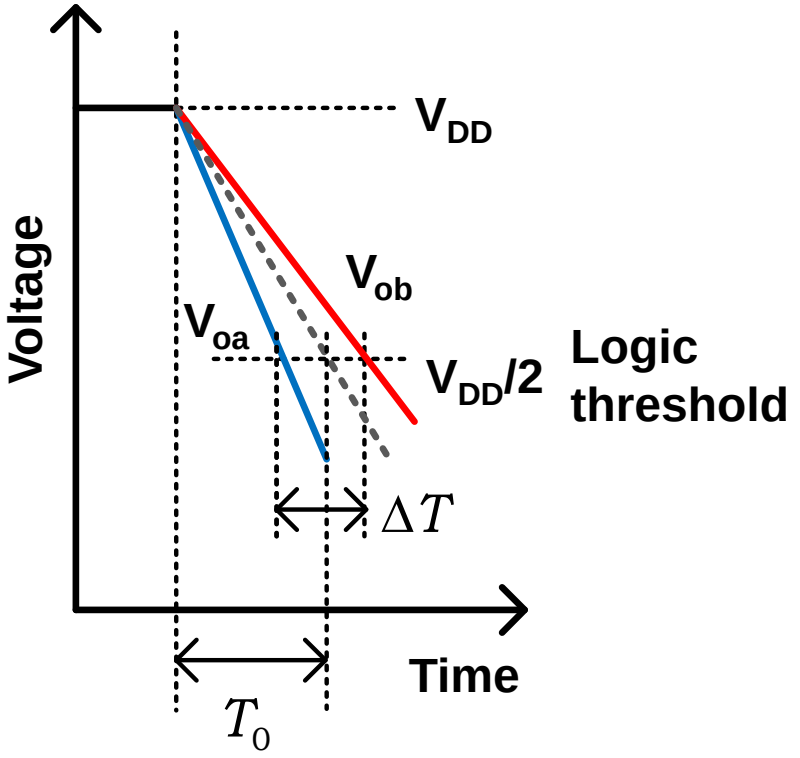
TOKYO TECH Pursuing Excellence

Voltage difference can be converted to time difference in a dynamic amplifier.

$$\Delta V_{in} = V_{in1} - V_{in2} \qquad \Delta T \approx \frac{\Delta V_{in}}{V_{eff}} T_0 \qquad V_{eff} = V_{GS} - V_T$$



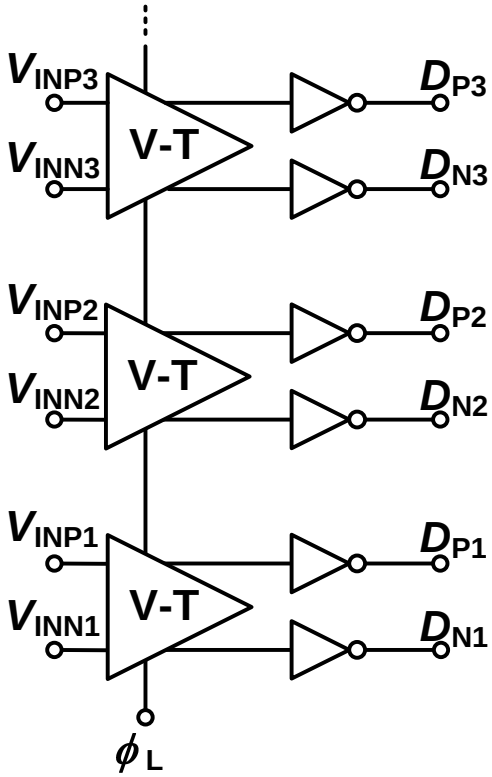
Dynamic amplifier



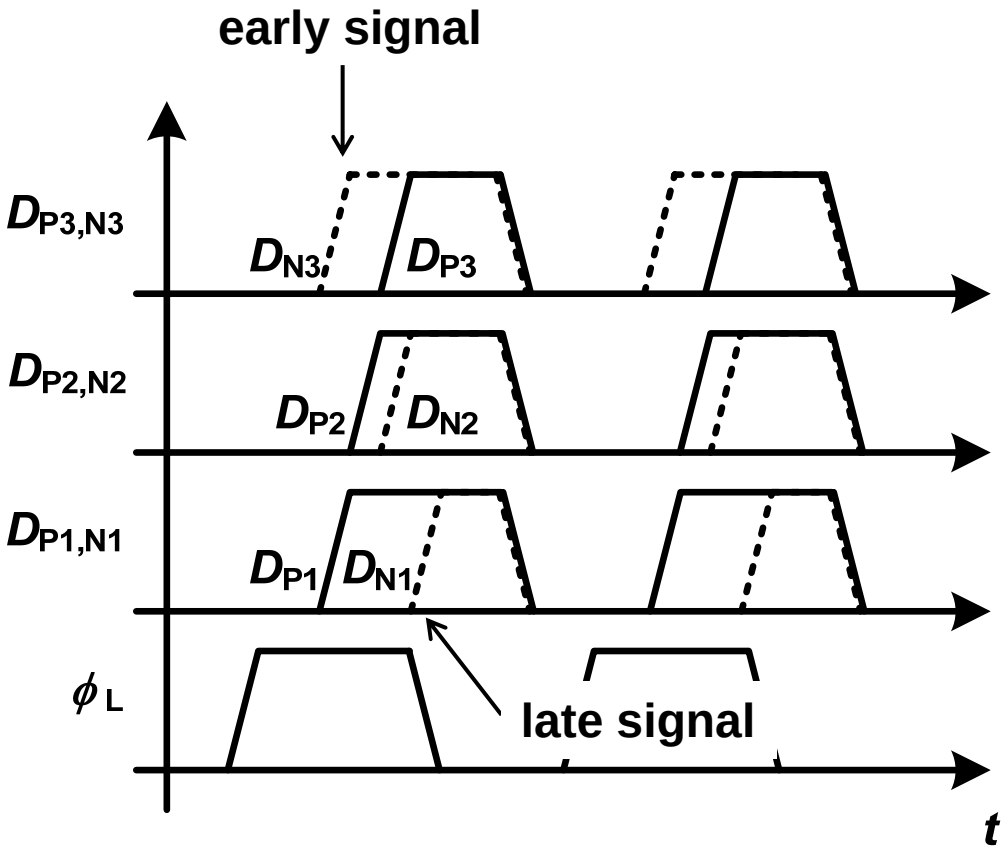
Matsuzawa & Okada Lab.

Conversion from the voltage to the timing

The signal generation of larger voltage difference is faster in the dynamic amplifier.



Dynamic Amps.

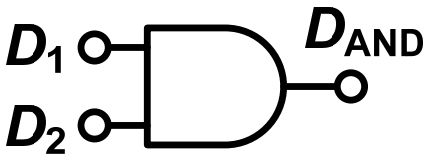


Signal folding in time-domain

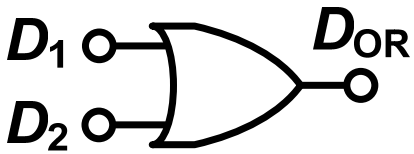
TOKYO TECH Pursuing Excellence

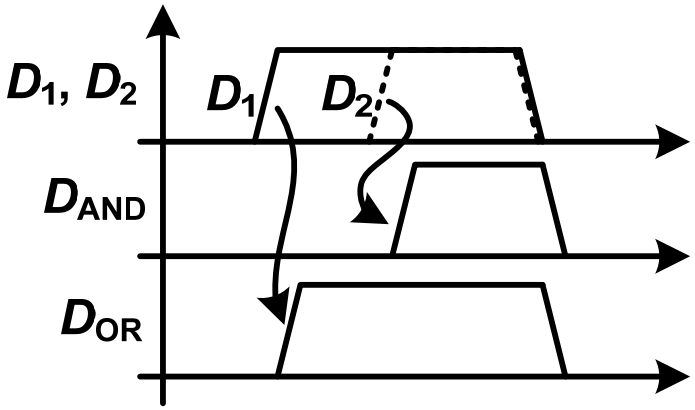
Signal folding in time-domain can be realized easily by simple logic gates.

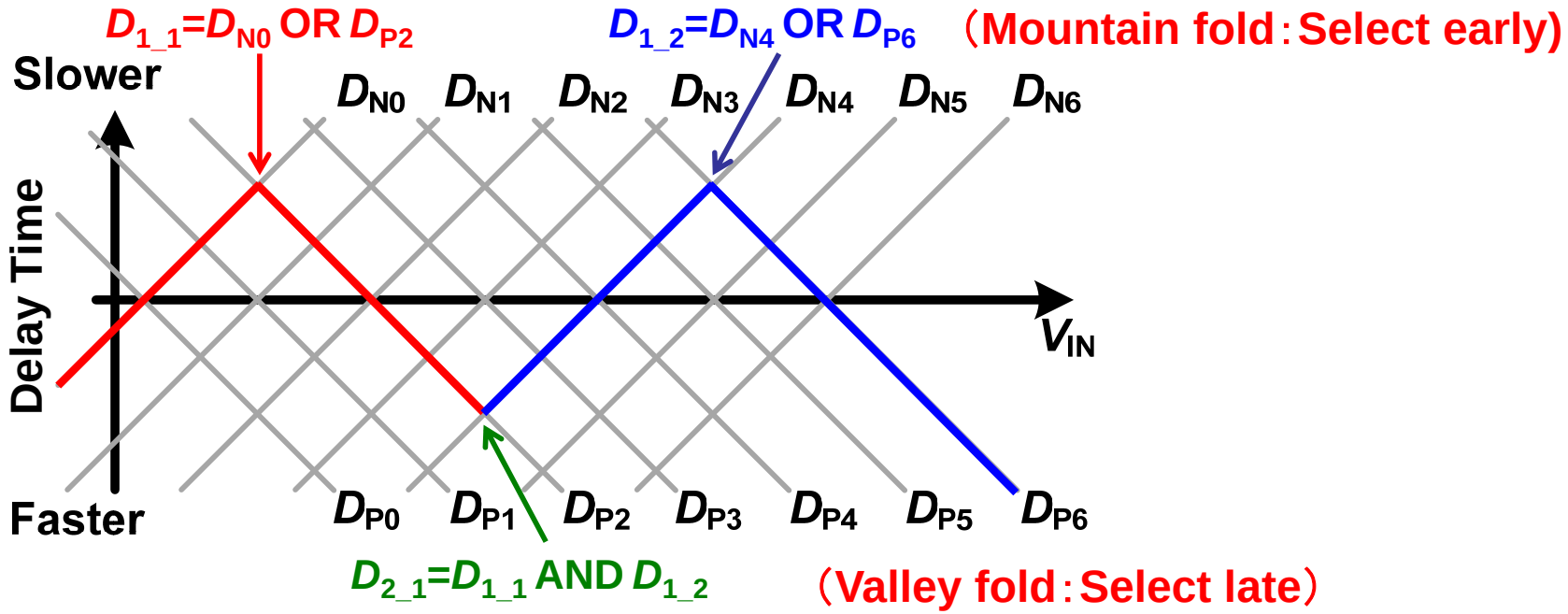
AND: Select late pulse



OR: Select early pulse







Matsuzawa & Okada Lab.

Performance comparison

TOKYO TECH Pursuing Excellence

Highest SNDR of 37.4 dB is attained in flash ADCs
No calibration circuits are required.
This ADC will contribute increase of data rate of 60 GHz transceivers.

P_d is large so far, however can be reduced by the optimization.

	ISSCC 2008 [3]	VLSI 2012 [8]	VLSI 2013 [9]	This work
Technology	90nm	40nm	32nm SOI	40nm LP
Resolution [bit]	5	6	6	7
Power Supply [V]	1	1.1	0.85	1.1
Sampling Frequency [GS/s]	1.75	3	5	2.2
Power Consumption [mW]	2.2	11	8.5	27.4
SNDR @Nyquist [dB]	27.6	33.1	30.9	37.4
FoMw [fJ/conv.-step]	64.5	99.3	59.4	210
FoMs [dB]	143.5	144.4	145.6	143.3
Core area [mm^2]	0.0165	0.021	0.02	0.052
Calibration	Off chip	Foreground	Off chip	No need

TOKYO TECH
Pursuing Excellence

Future Prospect of

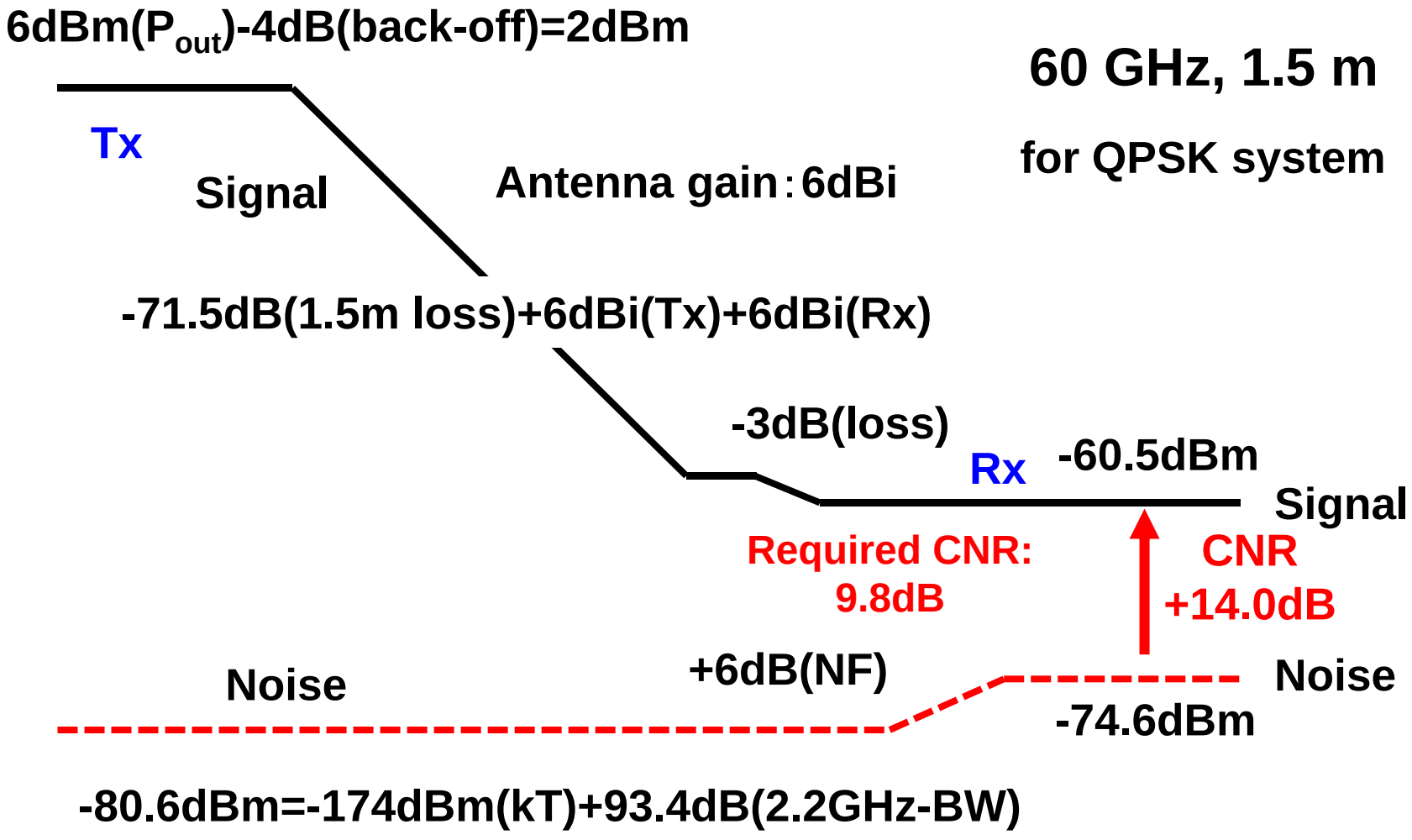
High Data Rate Wireless Systems

Nov.12. 2015.

Matsuzawa & Okada Lab.

Link budget example of wireless system

Transmitted RF power is lowered so much at the receiver



Calculations

Calculate the data rate as function of career frequency and Tx power

Shannon's theory

$$D_{rate} = BW \log_2\left(1 + \frac{S}{N}\right)$$

$$D_{rate} \approx BW \frac{\log_{10}(SNR)}{0.3} = BW \frac{SNR(dB)}{3}$$

Received signal

$$P_{RX}(dB) = P_{TX} - B_{OFF} + G_{AT} + G_{AR} - I_L - S_{LOSS}$$

Spatial loss

$$S_{LOSS} = -20\log\left(\frac{\lambda}{4\pi d}\right) = -20\log\left(\frac{c}{4\pi d f_c}\right) = 20\log\left(\frac{4\pi}{c} d f_c\right)$$

d: distance
f_c: career frequency

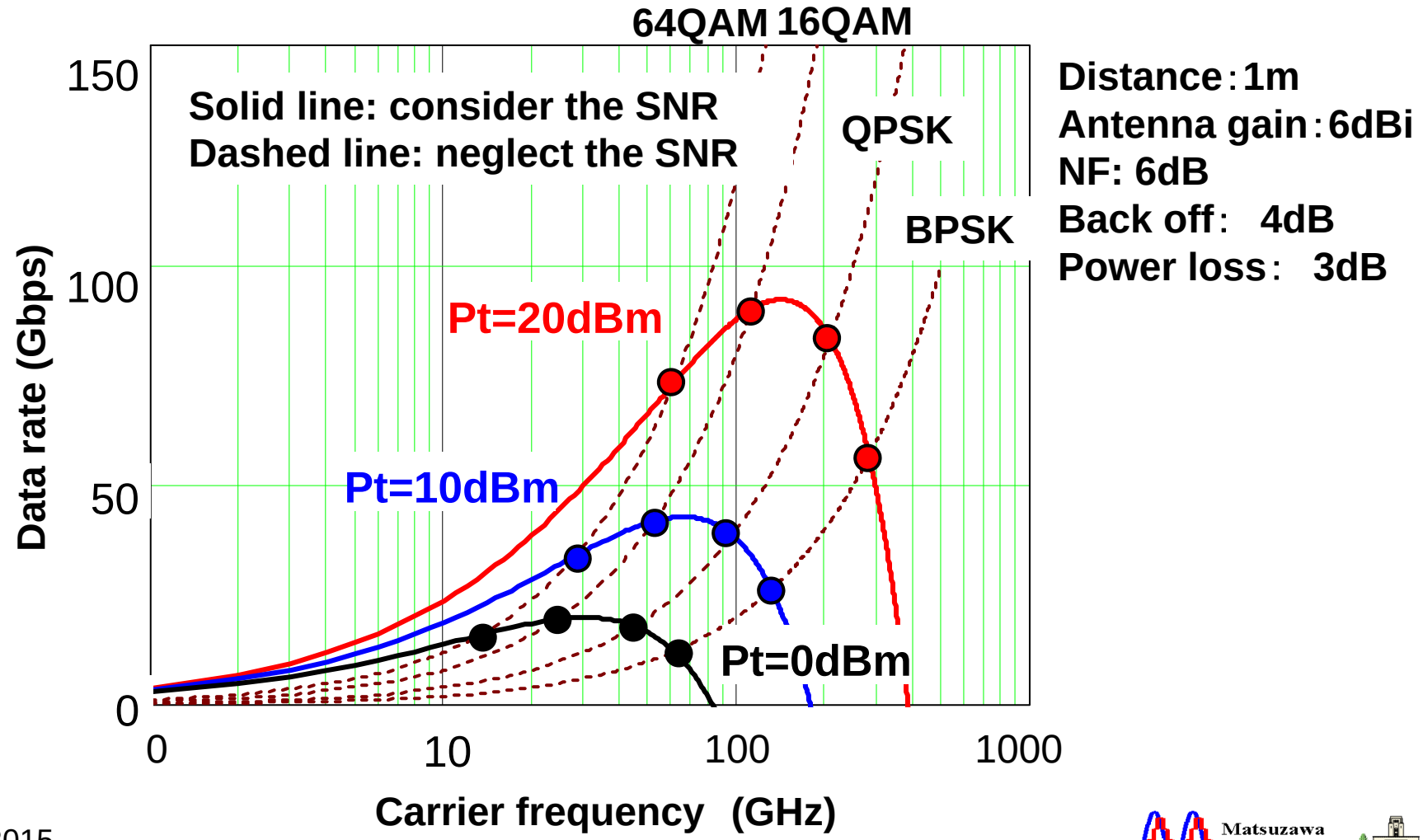
Noise

$$P_n(dBm) = -174 + 10\log BW + NF$$

Estimated data rate

TOKYO TECH Pursuing Excellence

There is an optimum frequency for the maximum data rate.
Higher Tx power is required to increase the data rate.
16 QAM looks the best to attain the maximum data rate.



Distance : 1m
Antenna gain : 6dBi
NF: 6dB
Back off : 4dB
Power loss : 3dB

Matsuzawa & Okada Lab.

Future direction

TOKYO TECH Pursuing Excellence

Future direction should be chosen by the usage model

High frequency and high power → **Best but very difficult !!**

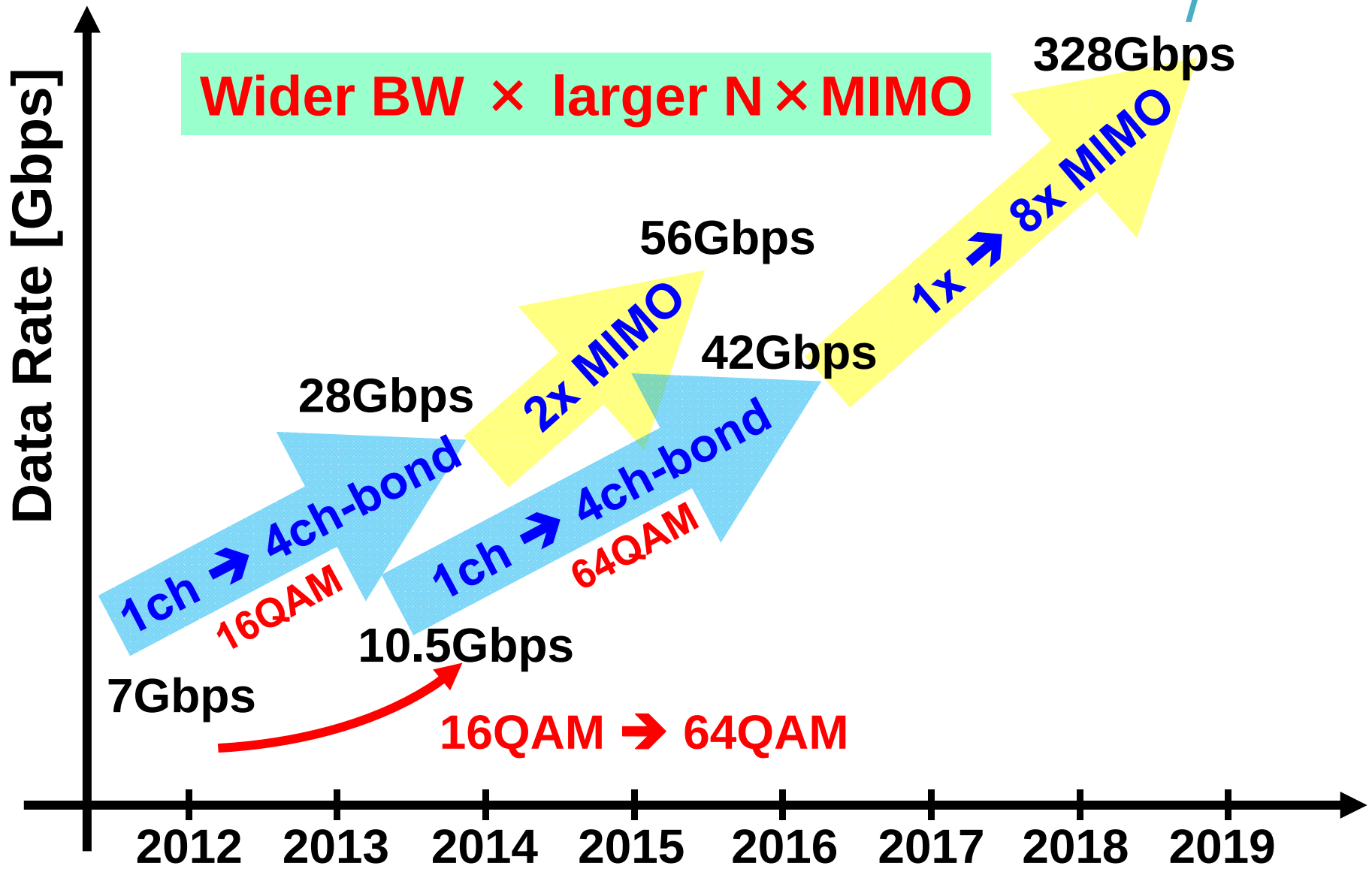
High frequency but low power

- High gain antenna → **Sharp beam** → **Fixed point only !**
- Low gain antenna → **Short distance only !**

Medium frequency but high power

- **Reasonable high data rate**
- **Reasonable long distance**

Our roadmap for 300Gbps data transfer



Summary

- High data rate wireless communication is demanded
- 28 Gb/s has been realized
- Wider bandwidth and higher SNR are the keys
  - Multi-cascaded amplifier
  - Passive mixer with resistive feedback
  - Injection locked I/Q oscillator
  - 7 bit ADC with time domain processing

$$D_{rate} = BW \log_2\left(1 + \frac{S}{N}\right)$$

- Accurate RF modeling and measurement up to 100 GHz is fundamentally important
- Optimum frequency for the maximum data rate.
  - Higher frequency does not guarantee the higher data rate
  - Higher Tx power is required to increase the data rate.
- Future direction should be chosen by the usage model
  - Long distance with reasonable data rate
  - Short distance with high data rate

Acknowledgement

TOKYO TECH Pursuing Excellence

- **I would like to thank Prof. K. Okada and this work was partially supported by MIC, SCOPE, MEXT, STARC, Huawei, Canon Foundation, STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc., and Agilent Technologies Japan, Ltd.**

And also,

Acknowledgement

TOKYO TECH Pursuing Excellence

Thanks lot to students