High Data Rate 60 GHz CMOS Transceiver Design

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ABSTRACT This paper discusses 60 GHz CMOS transceiver design focusing on the techniques to increase the transmission data rate. Basic design key points are the increase of bandwidth, the increase of SNR of ADC, and the decrease of phase noise in quadrature oscillator. Thus we selected the direct conversion architecture and used multi-cascading RF amplifiers. The resistive feedback amplifier is effective to realize the wideband impedance matching. The injection locking method is applied to the 60 GHz quadrature oscillator. A 7 bit, 2.2 GSsp ADC has been developed by using the voltage to time conversion in dynamic amplifier and the time domain signal folding with logic gates. Our developed 60 GHz CMOS transceiver realized the world's first 64QAM system and the full four channels 16QAM system and attained the world's highest data rate of 28 Gbps in 60 GHz wireless communication. Finally we estimated the data rate as a function of the career frequency and TX power. It suggests the importance of the increase of TX power for the further increase of the data rate.

Index Terms: CMOS, 60 GHz, transceiver, data rate, ADC, wide band, phase noise, injection locking, time base processing,

I. Introduction

Increase of data rate in wireless systems is fundamentally important not only to address the future huge traffic increase but also to shorten the activation time of the wireless devices. We have been developing high data rate 60 GHz CMOS Transceivers for a long time, as shown in Fig. 1.

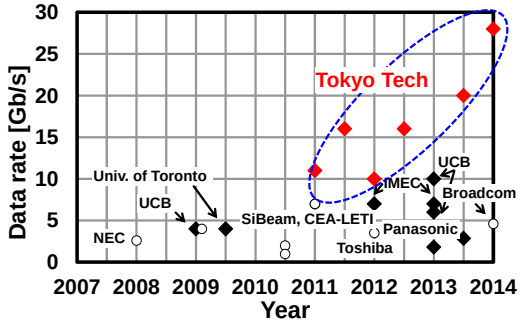


Fig.1. The data rate of 60 GHz transceivers.

We published the first paper of 60GHz CMOS transceiver on ISSCC 2011 [1] and it attained the date rate of 11 Gbps and recently the transceiver published on ISSCC 2014 attained 28 Gbps [2]. This paper discusses the key techniques to increase the data rate in wireless transceivers through our development experience.

Fig. 2 shows the 60GHz bandwidth allocation on IEEE802.ad [3]. Bandwidth of about 9 GHz is available from 57.24 GHz to 65.88 GHz. The number of channels is four and each bandwidth is 2.16 GHz.

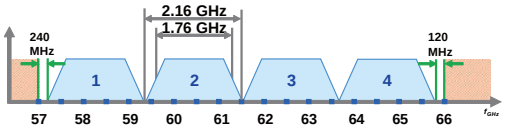


Fig. 2. 60GHz bandwidth allocation on IEEE802.ad.

The data-rate of communication systems, D is basically determined by the signal bandwidth, BW and the number of bit for the symbol, N shown in the following equation.

$$D = BW \times N \quad (1)$$

Therefore, we can increase the data rate by increasing the signal bandwidth and the number of bit for the symbol. Table 1 lists the possible data-rate for the four modulation methods and the available number of channels in 60 GHz range.

Table 1. Possible data-rate in 60GHz range.

	BPSK	QPSK	16QAM	64QAM
1ch	1.76	3.52	7.04	10.56
2ch	3.52	7.04	14.08	21.12
3ch	5.28	10.56	21.12	31.68
4ch	7.04	14.08	28.16	42.24

II. High Data Rate 60 GHz CMOS Transceiver

We developed 28 Gbps 60 GHz transceiver [2]. Fig. 3 shows a block diagram.

A direct conversion method is used to increase the bandwidth and to reduce the power consumption. 60 GHz

quadrature LC oscillators are employed and 20 GHz PLL drives them to realize an injection locking. The TX power is 10.3 dBm and the noise figure of RX is 4.2 dB.

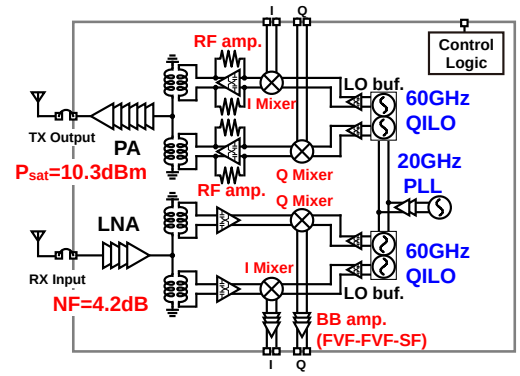


Fig.3. Block diagram of 60 GHz CMOS transceiver.

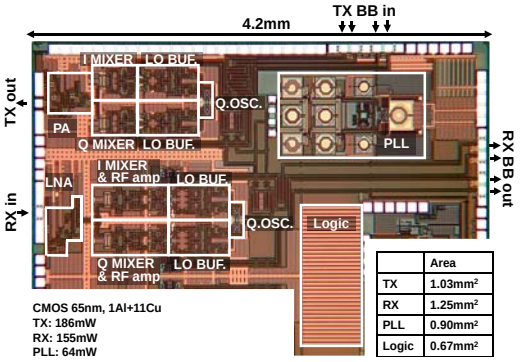


Fig. 4. Chip photograph.

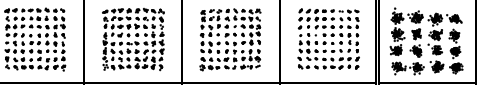
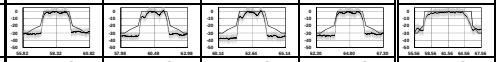
The chip was fabricated in 65 nm CMOS technology, as shown in Fig. 4. The fabricated chip was mounted in the evaluation board with 14-dBi horn antenna and the performance was measured with 25-GS/s Arbitral Waveform Generator and 100-GSps Oscilloscope, as shown in Fig. 5.

Fig. 5. Chip measurement setup.

Table 2 summarizes the performance. All four channels could realize 64QAM communication and attained the data rate of 10.56 Gbps with good EVM (TX-RX) of -24 dB to -26 dB. Furthermore, the four channel bonding was realized and attained 28.16 Gbps with 16QAM. The power consumptions of TX and RX including PLL are 251 mW and 220 mW, respectively.

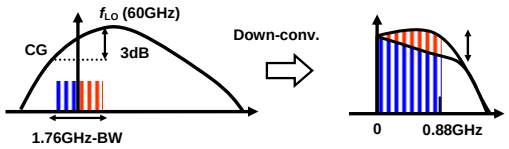
The realization of 64QAM and the full four channel bonding with 16QAM were the world's first achievements. Furthermore attained data rate of 28.16 Gbps is the world's highest data rate in 60 GHz range.

Table 2. Measured chip performance.

Channel	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 bond
Modulation	64QAM				16QAM
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s	28.16Gb/s
Constellation					
Spectrum					
TX EVM	-27.1dB	-27.5dB	-28.0dB	-28.8dB	-20.0dB
TX-to-RX EVM	-24.6dB	-23.9dB	-24.4dB	-26.3dB	-17.2dB

III. High Data Rate Circuit Design

Wide bandwidth, high SNR, and low distortion are the basic requirements for the high data rate circuit design. To keep the gain flat in wide bandwidth is crucially required. Fig. 6 shows the effect of gain flatness to the constellation of QAM signals. 2 dB gain difference in a bandwidth increases the bit error rate in the QAM signals. The gain difference causes ISI (Inter Symbol Interference) since the gain to the plus frequency is not equal to that for the minus frequency of signals. The gain flatness should be less than 1 dB over the target bandwidth.



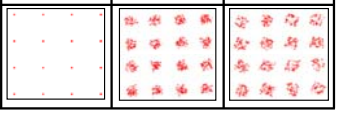
Gain Flatness	0dB	2dB	3dB
BER	~0	1.3e-5	3e-3
Constellation			

Fig. 6. The effect of the gain flatness for QAM signals.

Fig. 7 shows the power amplifier and the low noise amplifier. These amplifiers use four stage cascaded topology. One reason is to enhance the gain and the other reason is to realize good gain flatness by shifting resonant frequency.

The mixer in TX should be located as close to the power amplifier. Furthermore LC impedance matching method

should be avoided to realize the wide gain flatness, since reactive components have non-flat frequency characteristics essentially.

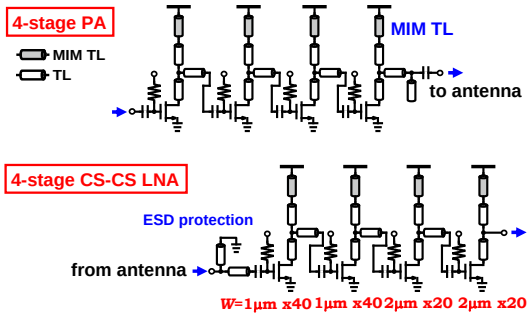


Fig. 7. Multi-cascaded RF amplifiers.

The passive mixer circuit should have flat impedance characteristics over the wide bandwidth. Fig. 8 shows the mixer circuit in TX. The input impedance of this mixer circuit is given by

$$Z_{in}(\omega) \approx 200\Omega // \left\{ R_{SW} + \frac{8}{\pi^2} \mathrm{Re}\left[Z_{RF}(\omega_{LO}) \right] \right\} \quad (2)$$

where Z_{RF} is the input impedance of RF amplifier [4]. The input impedance can be kept almost same value by using the resistive feedback.

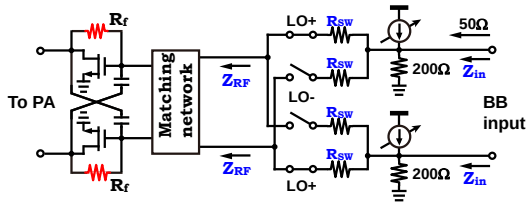


Fig. 8. The mixer circuit in TX.

Fig. 9 shows the measured gain of theTX circuit from DC to 4.32 GHz. The gain flatness of about 2 dB is realized.

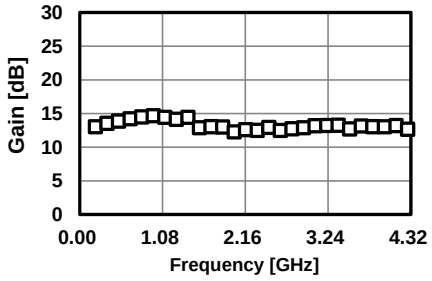


Fig.9. Measured gain of TX circuit.

The phase noise of the quadrature oscillator degrades the error rate of communication. Fig. 10 shows the effect of phase noise of oscillator to the wireless communication systems. For QPSK system, a poor phase noise oscillator can be accepted. For 8PSK system, the phase noise less than -87 dB can be used if the 1 dB reduction of CNR is allowed. For 16QAM system, the phase noise less than -90 dB is required.

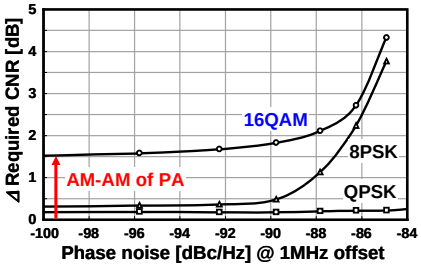


Fig. 10. Effect of the phase noise of oscillator.

The phase noise of the conventional VCO is mainly determined by the Q of LC tank circuit. The higher Q is the better for the phase noise. The Q of inductance can be increased by selecting the proper inductance to the target frequency, however the Q of capacitance with switch is rapidly degraded with frequency, as shown in Fig. 11. The Q of capacitance is less than 10 at 60 GHz. Therefore it is almost impossible to realize the high Q resonator at 60 GHz and it results in phase noise degradation. To solve this issue, we used the injection locking method. The 60 GHz quadrature LC oscillator is driven by the injection signal from the 20 GHz PLL of which phase noise is much better than that of the 60 GHz oscillator, as shown in Fig. 12 [1][5].

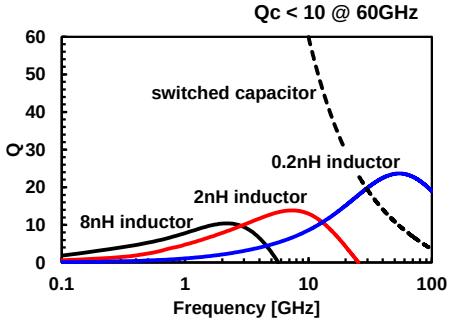


Fig. 11. Q of inductors and capacitor.

The phase of the injection signal determines the phase of the IL oscillator. The phase noise of the IL oscillator is given by

$$PN_{OSC}(dB) = PN_{INJ}(dB) + 20\log M \quad (3)$$

where M is the ratio between the oscillation frequency and the injection frequency.

Fig. 13 shows the measured phase noise of the IL oscillator.

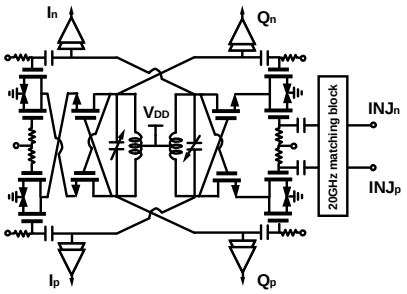


Fig. 12. Injection locked 60 GHz quadrature oscillator.

The phase noise of the IL oscillator at 1MHz is -86 dBc/Hz and that of 20 GHz PLL is -106 dBc/Hz. M is 3 (10 dB) and the phase noise of the IL oscillator is -96 dBc/Hz. This is low enough for 16QAM system and accepted for 64QAM system.

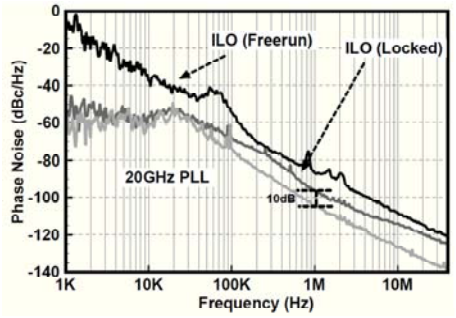
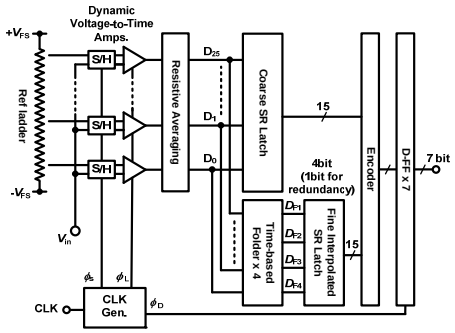


Fig. 13. Measured phase noise of the IL oscillator.

IV. High Speed and Low Power A/D Converter

A high speed A/D converter (ADC) is a core circuit to realize the high data rate wireless communication systems, as well as wideband RF circuits.



14. Block diagram of the 7-b 2.2 GSps ADC.

The sampling rate in 60 GHz range is about 2.2 GSps to 3 GSps for the single channel and the required resolution is conventionally 5 bit for QPSK and 7 bit for 16QAM. We developed 7-b 2.2 GSps ADC for the 16QAM system [6]. Fig.14 shows a block diagram of the ADC.

A conventional high speed ADC uses a flash architecture, however the power consumption and the occupied area are exponentially increased with the resolution. To address this issue, the use of folding and interpolated ADC architecture is one candidate, however it consumes large power. Thus we used dynamic amplifiers to reduce the power consumption and to realize the voltage to time conversion.

Fig. 15 shows a dynamic amplifier and voltage to time conversion. In initial state, the output nodes are pre-charged. When CLK is enabled, the upper side switches are opened and the lower side switch is closed. The drain currents of MOS transistors flow and the output voltages V_{oa}, V_{ob} are going down. Through this process, the timing difference appears between the two signals. The timing difference at the logic threshold voltage is given by

$$\Delta T = \frac{\Delta V_{in}}{V_{eff}} T_0 \quad (4)$$

where T_0 is the time when the average of the output voltages V_{oa} and V_{ob} crosses the logic threshold voltage, V_{eff} is the effective gate voltage (V_{GS}-V_T) of MOS transistor. Thus the input voltage difference is converted to the timing difference.

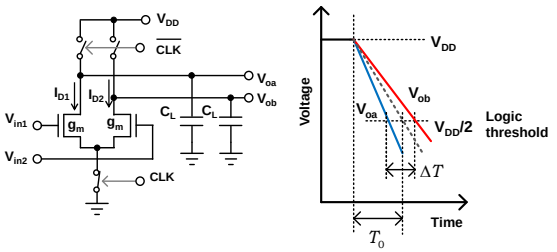


Fig. 15. V to T conversion using a dynamic amplifier.

Fig. 16 shows the dynamic amplifiers and the output voltages. The timing difference of the differential output voltage is proportional to the voltage difference. After the voltage difference is converted to time difference, the folding of signal is realized by the logic gates, as shown in Fig. 17. The AND gate selects the late pulse and the OR gate select the early pulse.

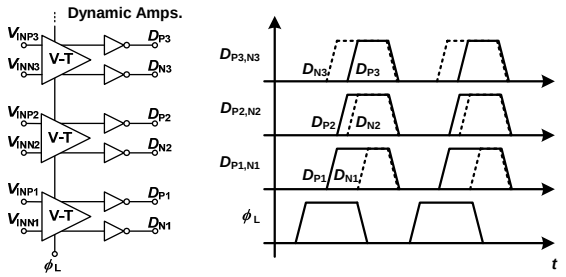


Fig. 16. Dynamic amplifiers and the output voltages.

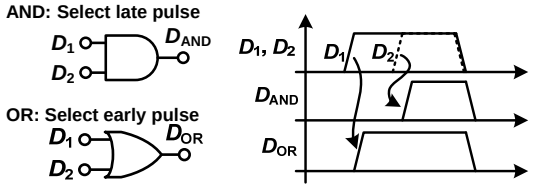


Fig. 17. Logic gates as selectors of early and late pulse.

Fig. 18 shows the signal folding using AND and OR gates. The signal can be folded easily by using timing difference and simple logic gates.

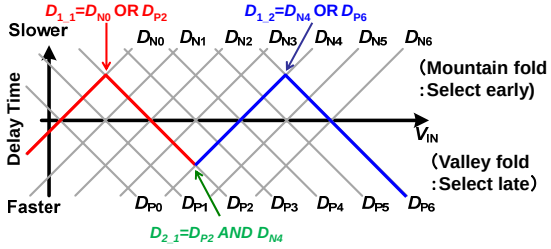


Fig. 18. Signal folding by using AND and OR gates.

Finally the generated folding signals are interpolated to generate the more fine resolution signals. The interpolation can be made by the gate-weighted inverters.

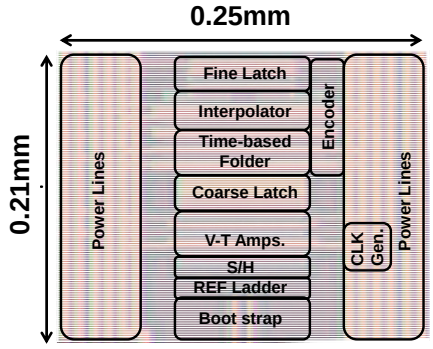


Fig. 19. Chip photo of time-based folding ADC.

Fig. 19 shows the chip photograph of this ADC fabricated in 40 nm CMOS technology.

It can be operated with the sampling rate of 2.2 GSps, consumes 27.4 mW, and attained SNDR of 37.4 dB at the Nyquist input frequency. The FoMs is 210 fJ/conv.-steps and FoMw is 143.3 dB. This ADC attained the highest SNDR as an ADC operated with several GSsp. The power consumption is a little large but it can be reduced down to the half by the circuit optimization.

V. Future Prospect of High Data Rate Wireless Systems.

The future prospect should be discussed to indicate the research direction in high data rate wireless communications.

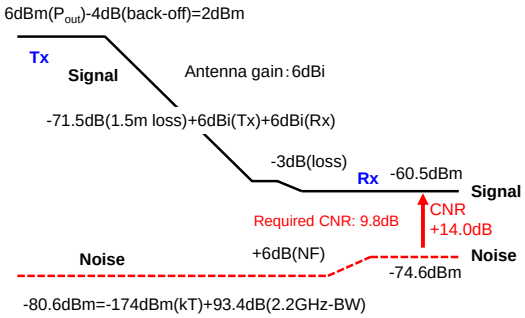


Fig. 20. Link budget example of the wireless system.

Fig. 20 shows a link budget example of the wireless system. The data rate, D is determined by bandwidth, BW and signal to noise ratio, SNR given by the Shannon's theory.

$$D = BW \log_2(1 + SNR) \quad (5)$$

This equation can be modified

$$D \approx BW \frac{\log_{10}(SNR)}{0.3} = BW \frac{SNR(dB)}{3} \quad (6)$$

The received signal power P_{RX} is

$$P_{RX}(dB) = P_{TX} - B_{OFF} + G_{AT} + G_{AR} - I_L - S_{LOSS} \quad (7)$$

where P_{TX} is the T_X output power, B_{OFF} is the back-off margin, G_{AT} and G_{AR} are the antenna gains of the TX side and the RX side, IL is the implementation loss, and S_{loss} is the space loss. The S_{loss} is given by Friis's equation.

$$S_{LOSS} = -20\log\left(\frac{\lambda}{4\pi d}\right) = -20\log\left(\frac{c}{4\pi d f_c}\right) = 20\log\left(\frac{4\pi}{c} d f_c\right) \quad (8)$$

where d is the distance between the TX antenna and the RX antenna, c is the light velocity, f_c is the career frequency. Basically the space loss is increased by the distance and career frequency. Increase of antenna area

can increase of the antenna gain and improve the space loss at the higher career frequency, however it results in beam narrowing and makes the antenna alignment more difficult.

In Fig. 20, P_{out} (=P_{TX}) of 6 dBm with B_{OFF} of 4 dB is decreased down to -60.5 dBm at the RX with distance of 1.5 m in 60 GHz wireless communication system. On the other hand, the noise power, P_n is given by

$$P_n(dBm) = -174 + 10\log BW + NF \quad (9)$$

where the first term expresses the thermal energy kT and NF is the noise figure of the RX.

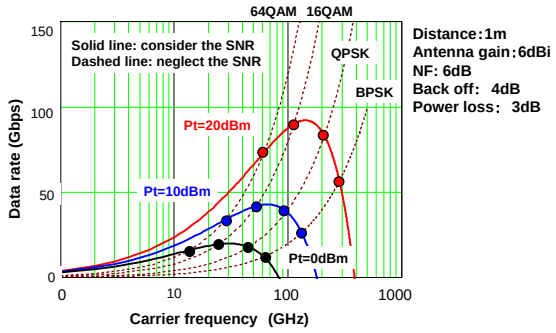


Fig. 21. Data rate vs. career frequency.

We estimated the possible data-rate of wireless communication systems as a function of carrier frequency and TX power, as shown in figure 21. If we neglect the SNR, the data rate is merely increased with the increase of the career frequency and the large number QAM is the better. However if we consider the SNR, the peak career frequencies appear, such as 30 GHz for Pt of 0 dBm, 70 GHz for Pt of 10 dBm, and 150 GHz for Pt of 20 dBm. Interestingly 16QAM gives the highest data rate for all cases. The 64QAM can increase the date rate potentially, however requires severe high SNR and it is degraded rapidly with increase of the special loss. Low TX power doesn't give the sufficient SNR and results in lower data rate.

This estimated result suggests us that the increase of career frequency doesn't guarantee the increase of the data rate and the increase of TX power is very important. If we can't increase the TX power, high data rate will be realized only for the short distance. The higher antenna gain can increase the communication distance, however it theoretically narrows the bean angle and only the fixed point communication will be available.

VI. Conclusion

We have been developing high data rate 60 GHz CMOS transceivers. Basic design key points are the increase of bandwidth, the increase of SNR of ADC, and the decrease of phase noise in the quadrature oscillator. we selected the direct conversion architecture and used multi-cascading RF amplifiers. The resistive feedback amplifier is effective to realize the wideband impedance matching. The injection locking method is applied to the 60 GHz quadrature oscillator. A 7 bit, 2.2 GSsp ADC has been developed by using the voltage to time conversion in the dynamic amplifier and the time domain signal folding with logic gates. Our developed 60 GHz CMOS transceiver realized the world's first 64QAM system and the full four channels 16QAM system and attained the world's highest data rate of 28 Gbps in 60 GHz wireless communication. Finally we estimated the data rate as a function of the career frequency and TX power. It suggests the importance of increase of TX power for the further increase of the data rate.

Acknowledgement

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