A 9-bit 1.8 GS/s Pipelined ADC Using Linearized Open-Loop Amplifiers

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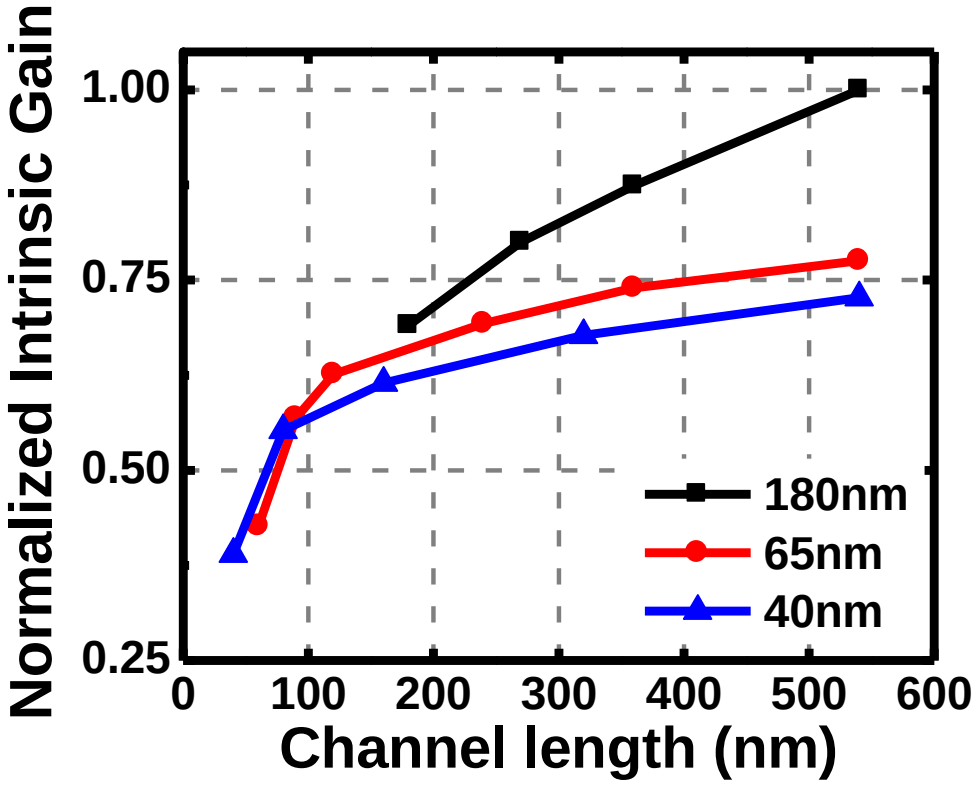
Outline

- Motivation
- Prior Arts
- Proposed Open-Loop ADC
- Measurement Results
- Conclusion

Advanced Process

- **Intrinsic gain is decreasing under more advanced process**



Key Challenges

- **Reduced gain**
- **Reduced headroom**
- **Power efficiency**

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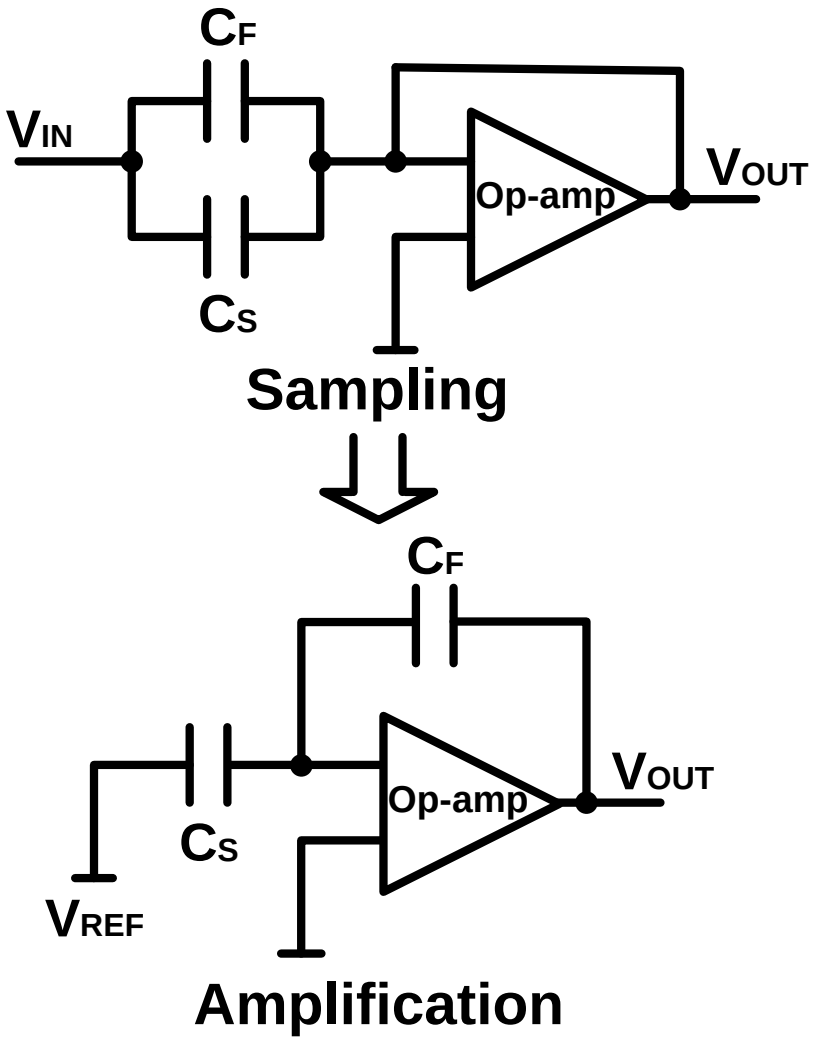
Conventional Pipelined ADCs (1/2)

- **Closed-loop based amplification**



Requirements:

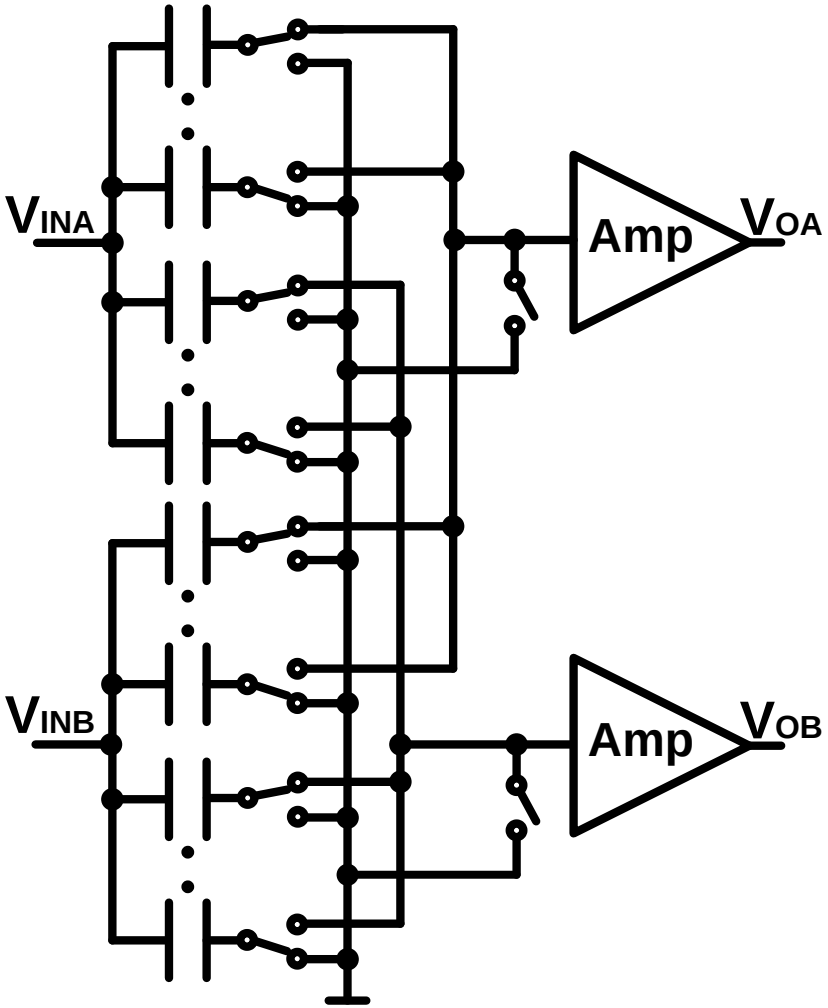
- **high gain of Amp.**
  - **multi-stage Amp. [1]**
  - **extra technique [2]**
- **stability**
  - **2^{nd} pole > 3×1^{st} pole**

$$Power \propto (3+x)\cdot BW$$

[1] Y. J. Kim, *et al*., CICC 2009.
[2] Y. Chiu, *et al*., JSSCC 2004.

Conventional Pipelined ADCs (2/2)

- **Interpolation based amplification [3]**



Requirements

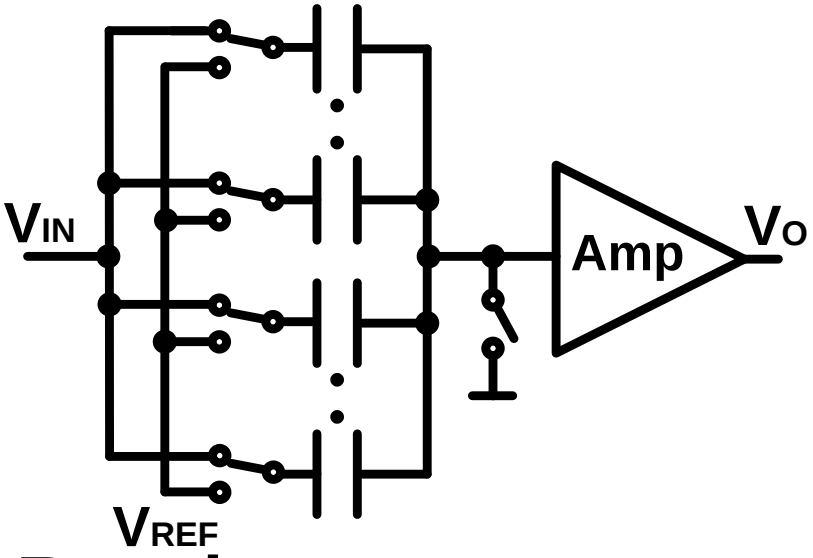
- ➢ **two Amp. and CDAC**
  - **doubled power**
- ➢ **relative gain accuracy**

$$Power \propto 2 \cdot BW$$

[3] M. Miyahra, *et al*., VLSI 2011.

Open-Loop Structure

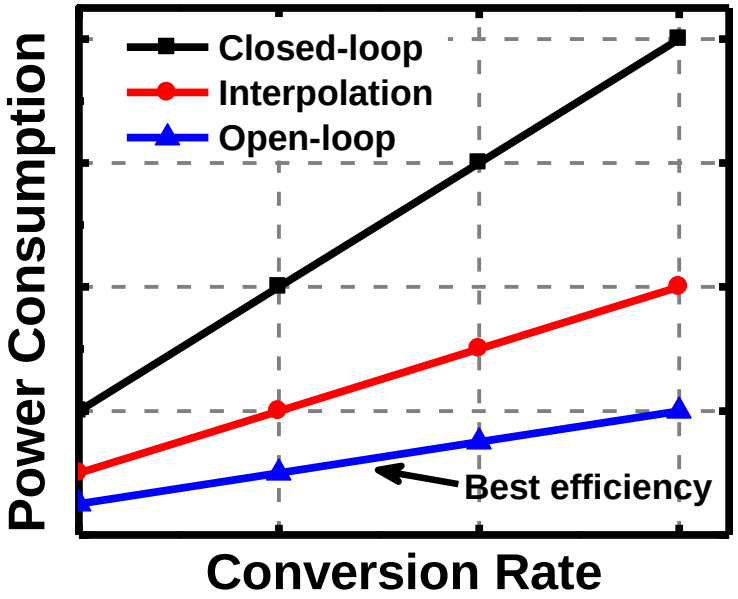
- **Open-loop based amplification**



Requirements

- ➢ **One Amp. and CDAC**
- ➢ **Accurate gain**

$$Power \propto 1 \cdot BW$$



However, due to the nonlinearity of open-loop amplifier, resolution is limited. [4]

[4] D. Shen, *et al*., JSSC 2007.

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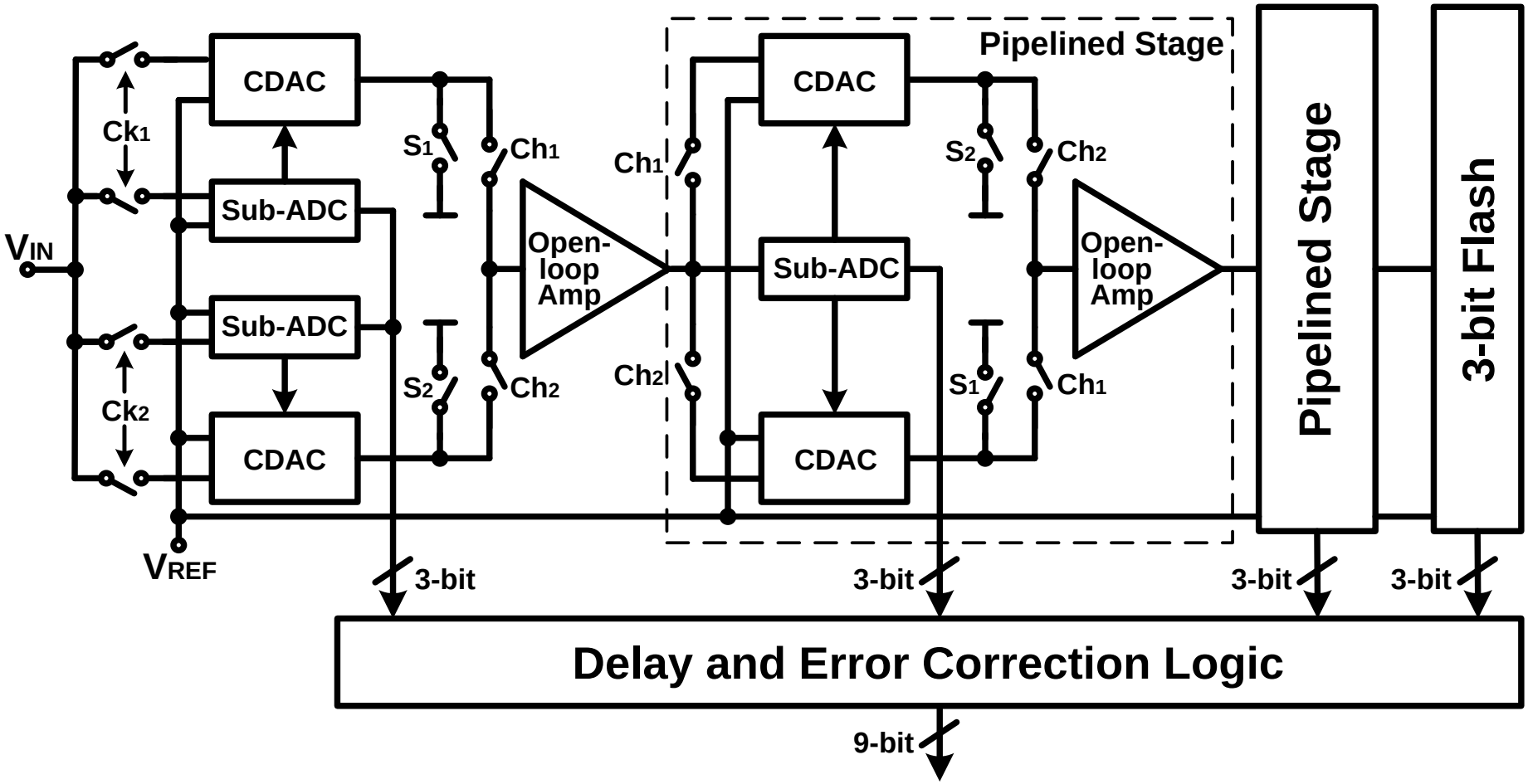
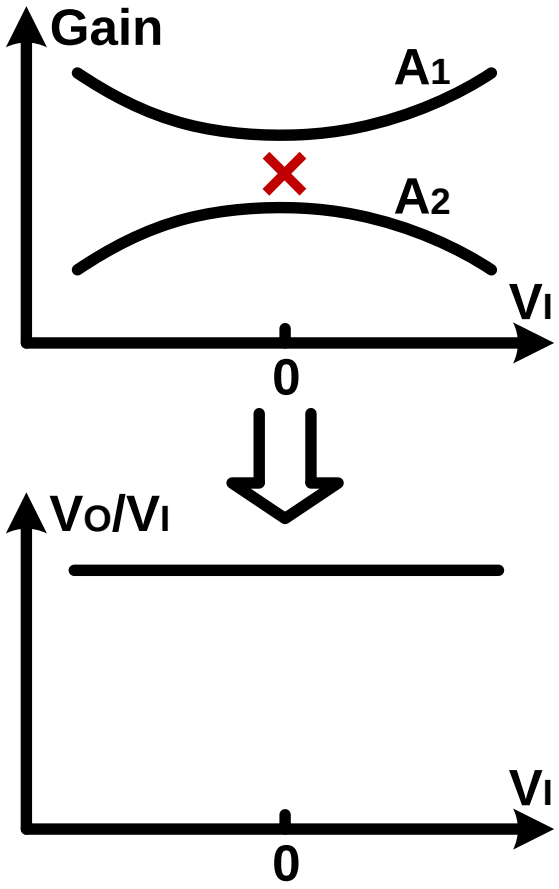
9-bit 1.8 GS/s 44 mW pipelined ADC

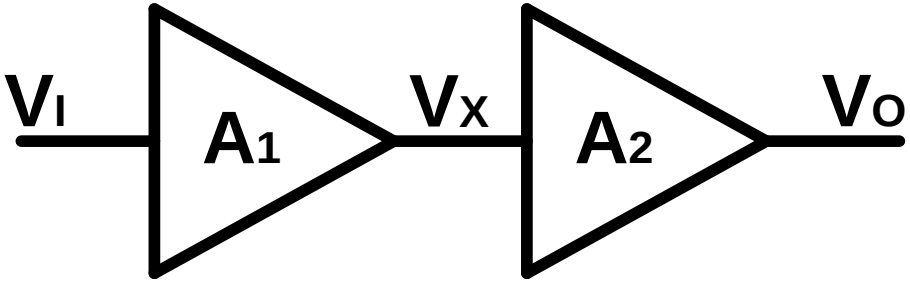


- Linearized open-loop amplifier
- CDAC gain calibration
- Double sampling and top-plate sampling

Linearized Open-Loop Amplifier (1/5)

- **A product of two reversed nonlinearity**





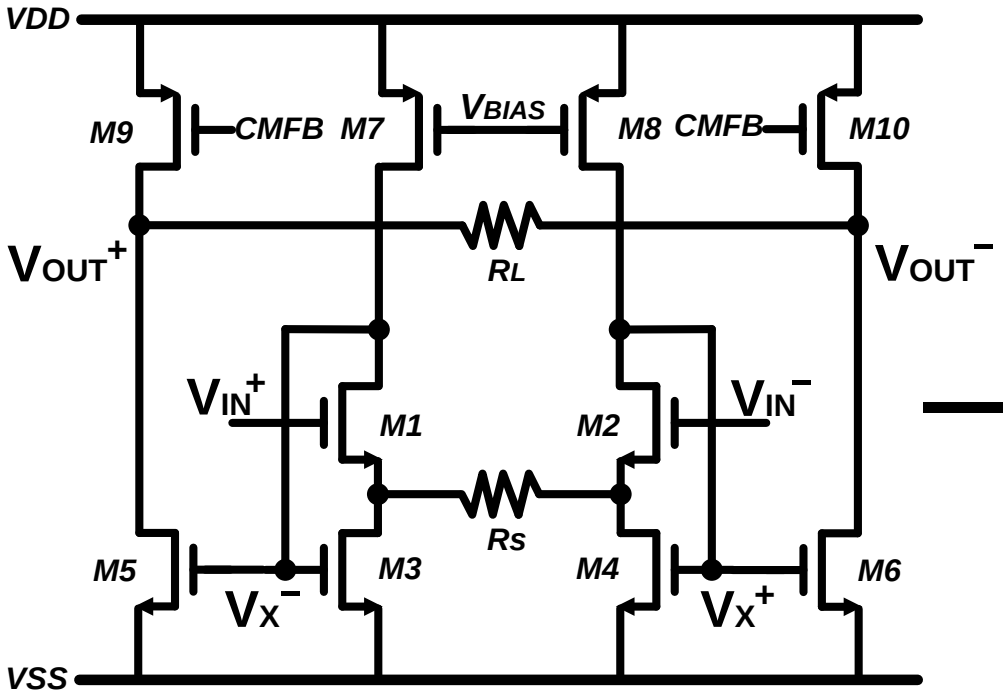
$$V_X = \alpha_1 V_I + \beta_1 V_I^3 \quad V_O = \alpha_2 V_X + \beta_2 V_X^3$$

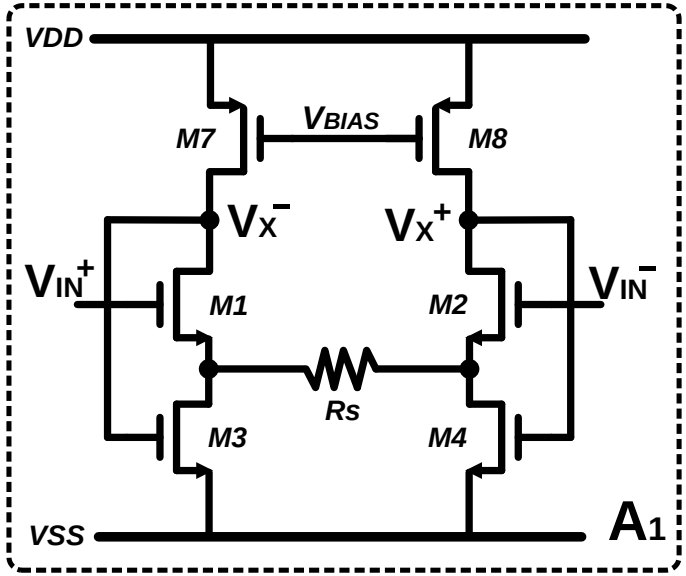
$$V_O \approx \alpha_1 \alpha_2 V_I + (\alpha_1^3 \beta_2 + \alpha_2 \beta_1) V_I^3$$

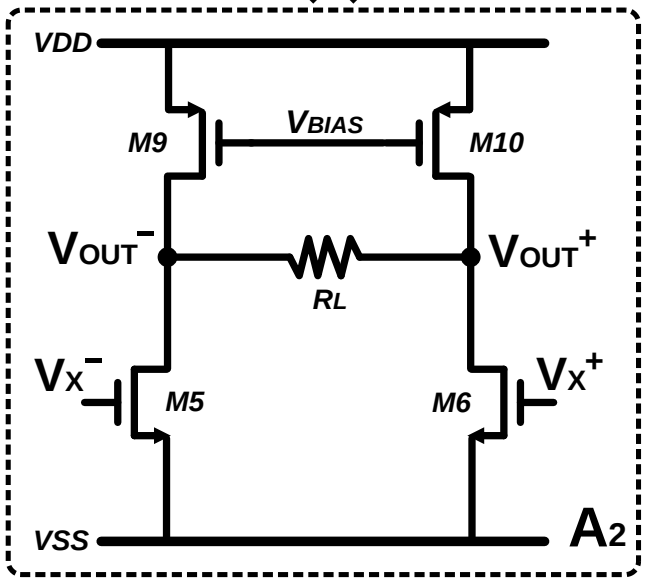
α_i, β_i represents the 1st and 3rd order coefficient of A_1 and A_2, respectively

Linearized Open-Loop Amplifier (2/5)

- **Circuit implement**



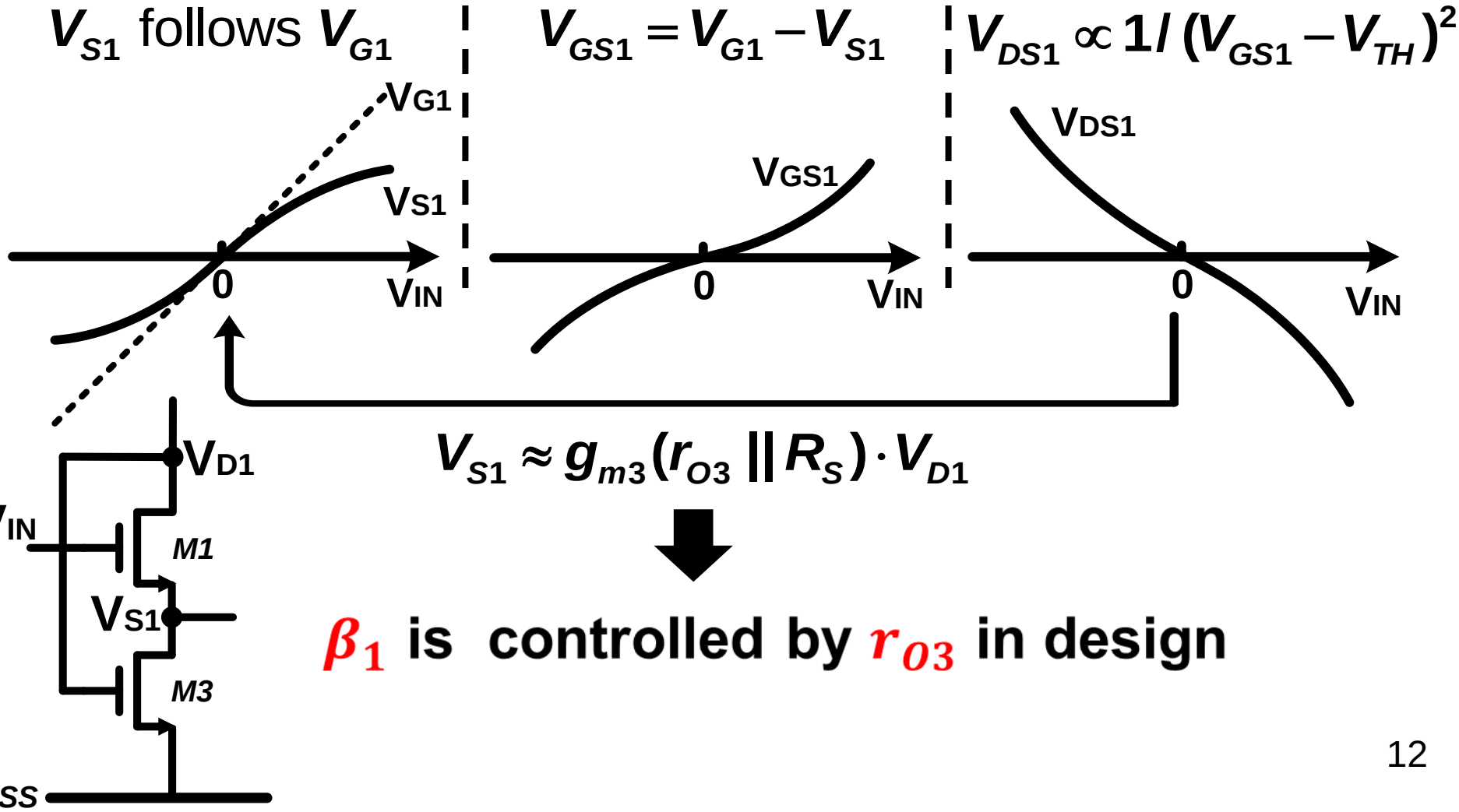




Key is to generate an A_1 with proper β_1

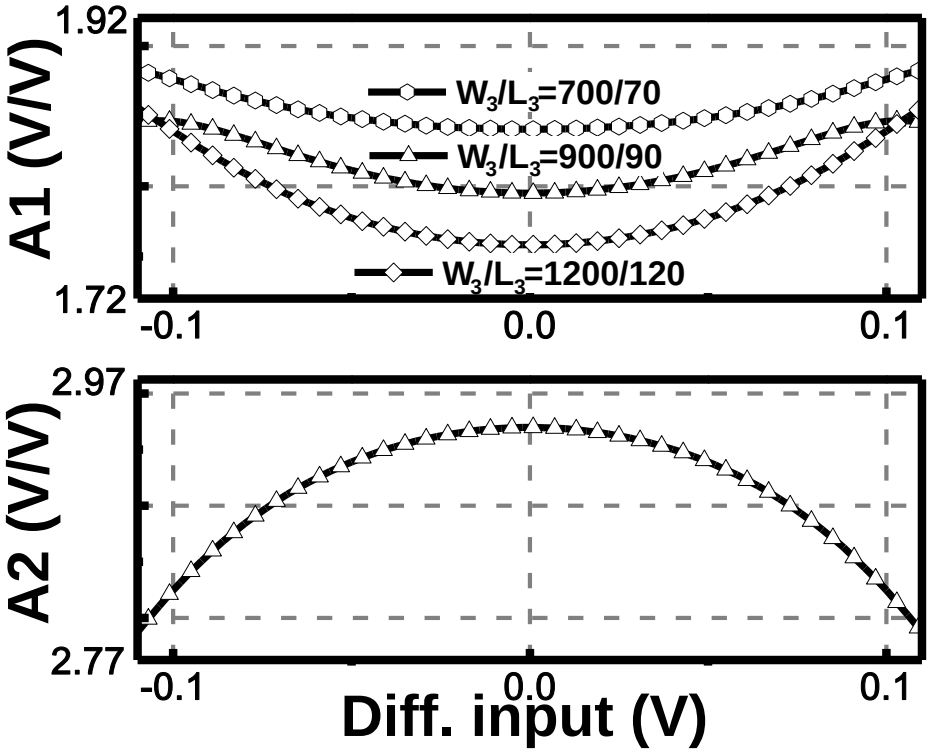
Linearized Open-Loop Amplifier (3/5)

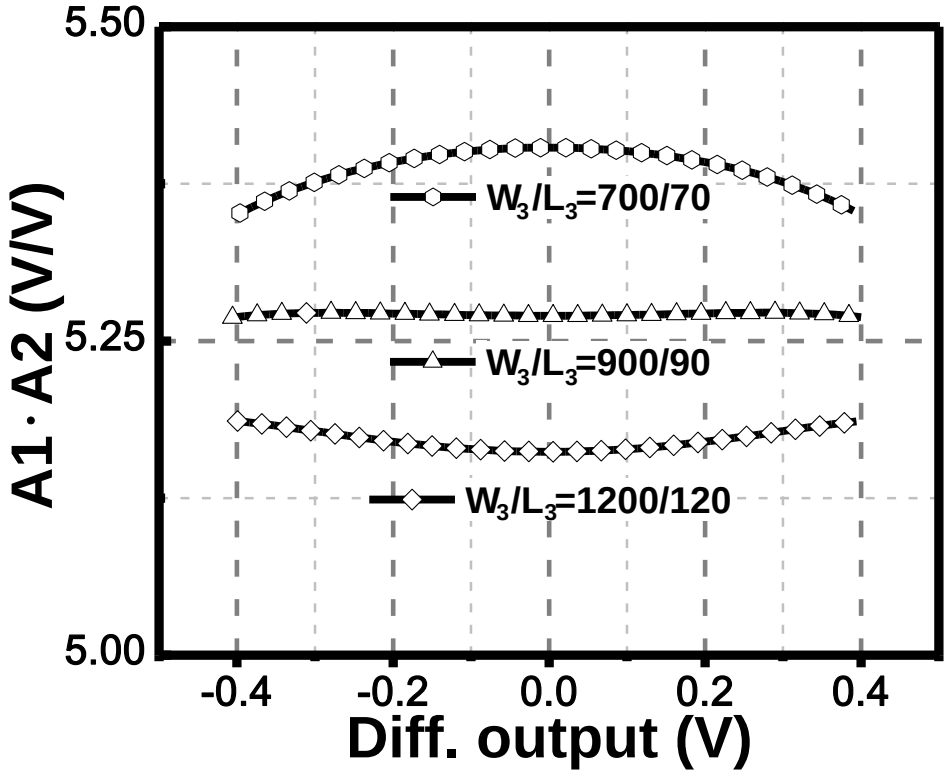
- Generation of A_1



Linearized Open-Loop Amplifier (4/5)

- Linearity vs. r_{O3}

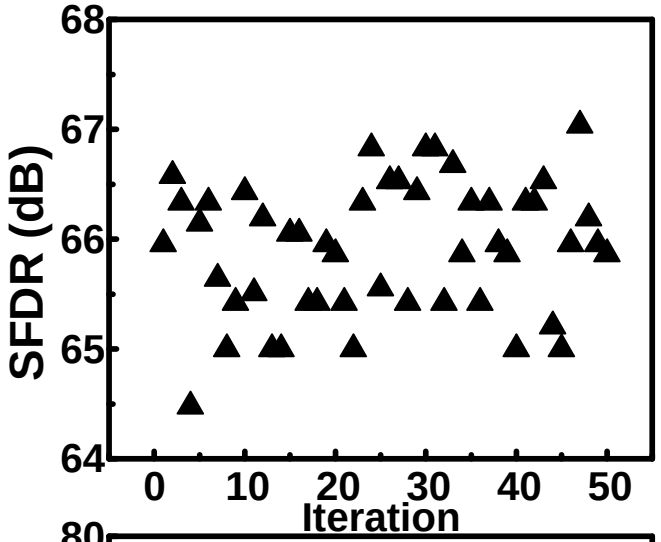


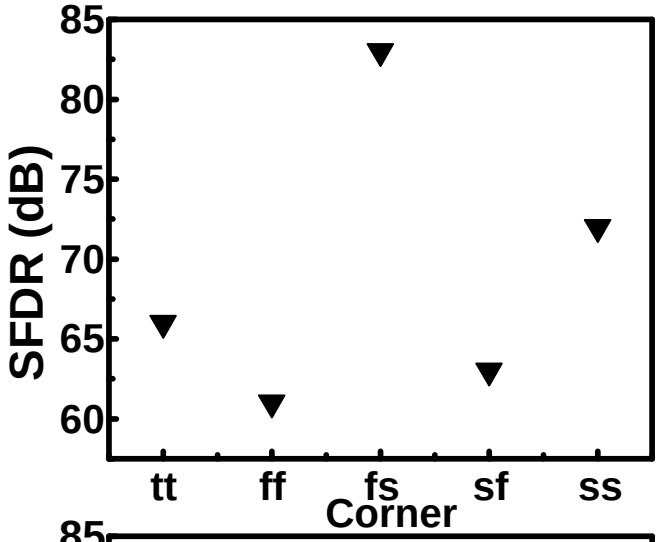


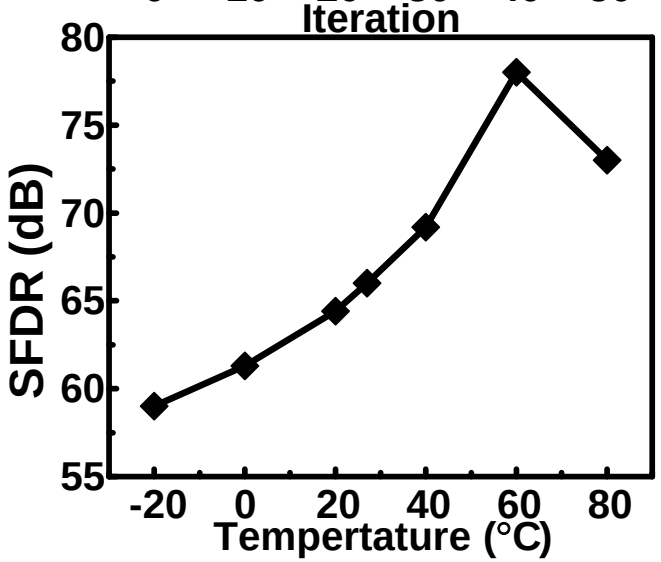
The linearized open-loop Amp. can support 9-bit resolution, while source-degenerated Amp. supports 6-bit [4]

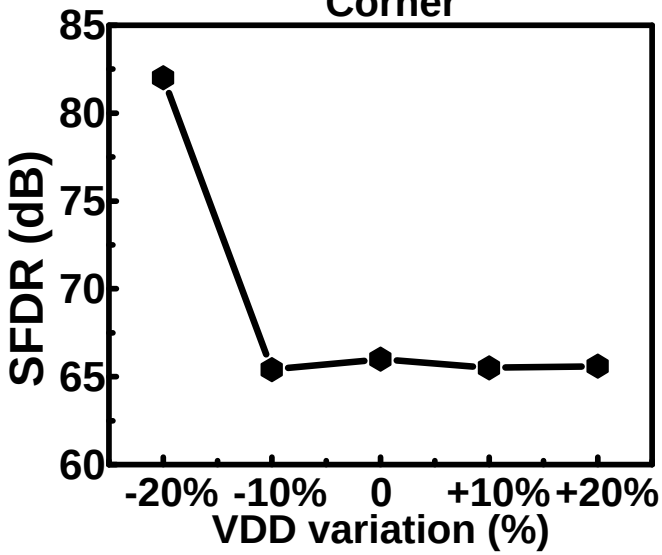
Linearized Open-Loop Amplifier (5/5)

- **PVT variations**



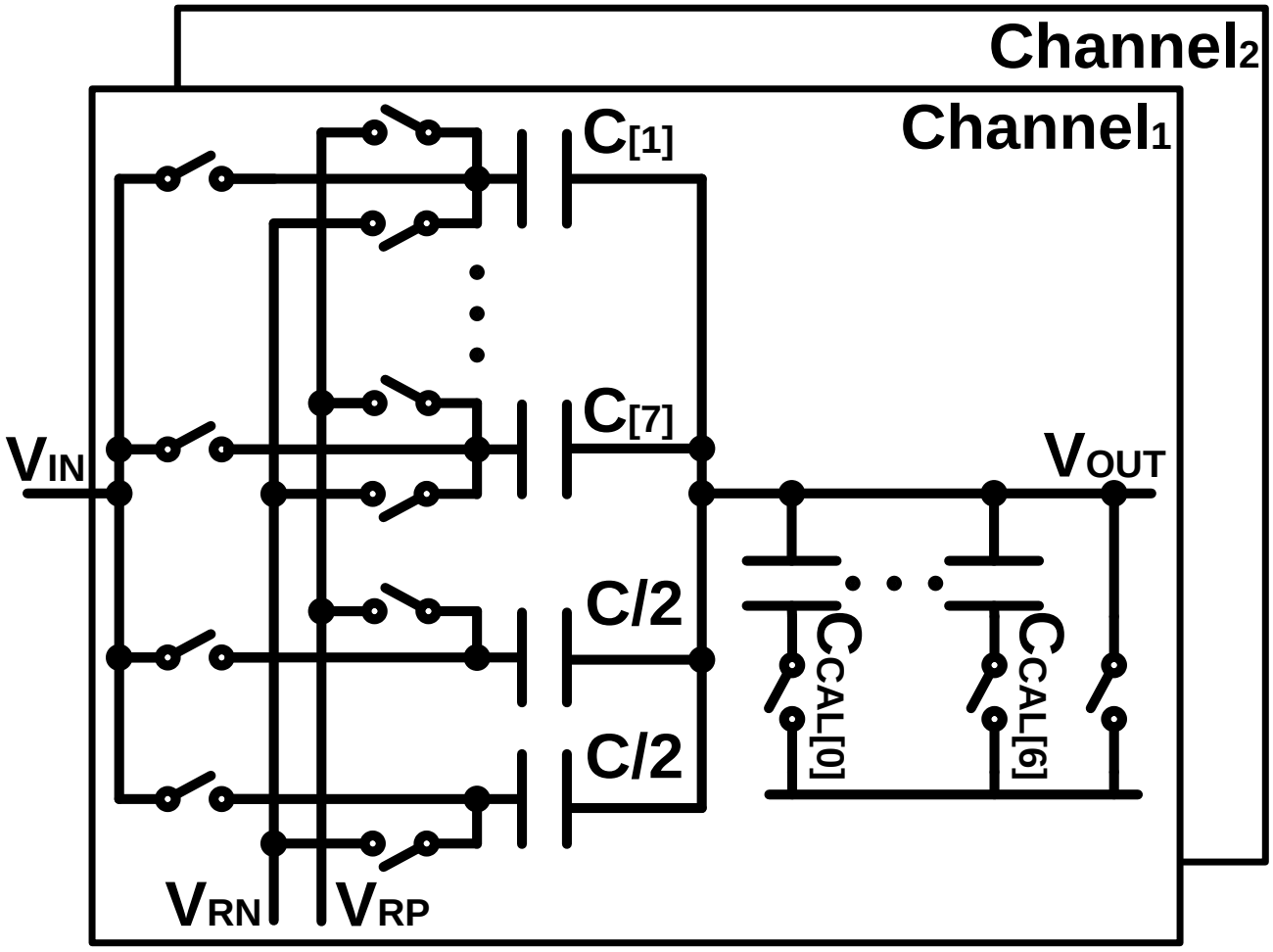






CDAC Gain Calibration

- **Stage gain is controlled by CDAC**



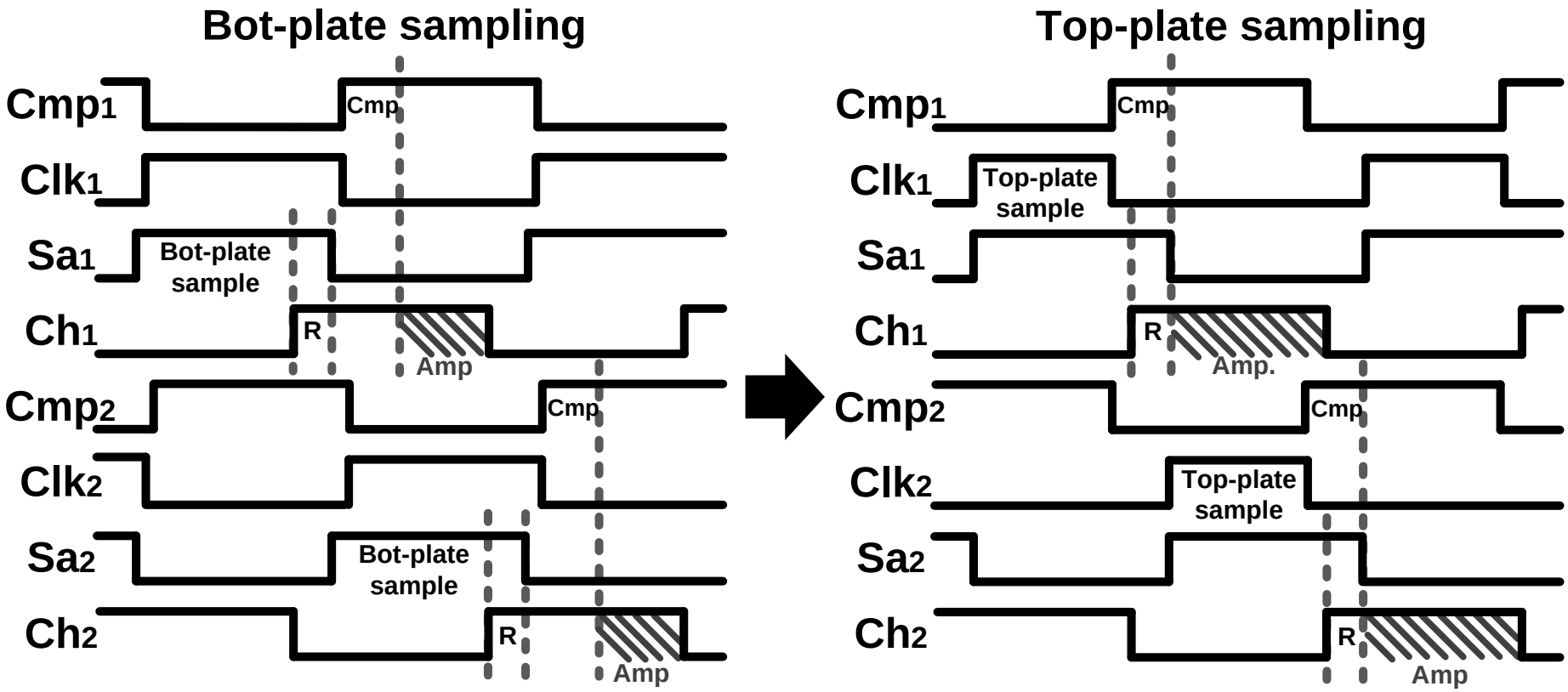
Stage gain

$$= \frac{8C}{8C + C_{CAL}} \cdot A$$

Won't affect the linearity of Amp.

Top-plate Sampling

- **Efficiency enhanced timing for memory effect in double sampling**



Top-plate sampling increases 50% amplify time

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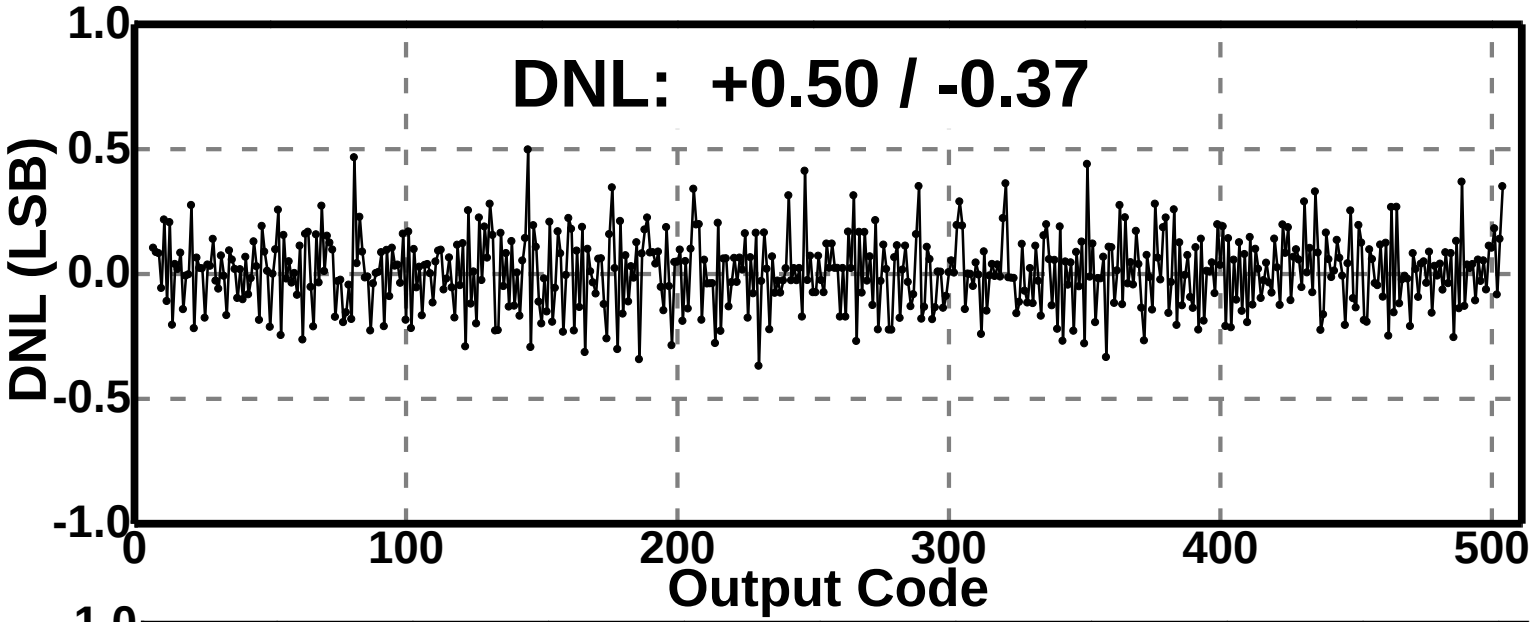
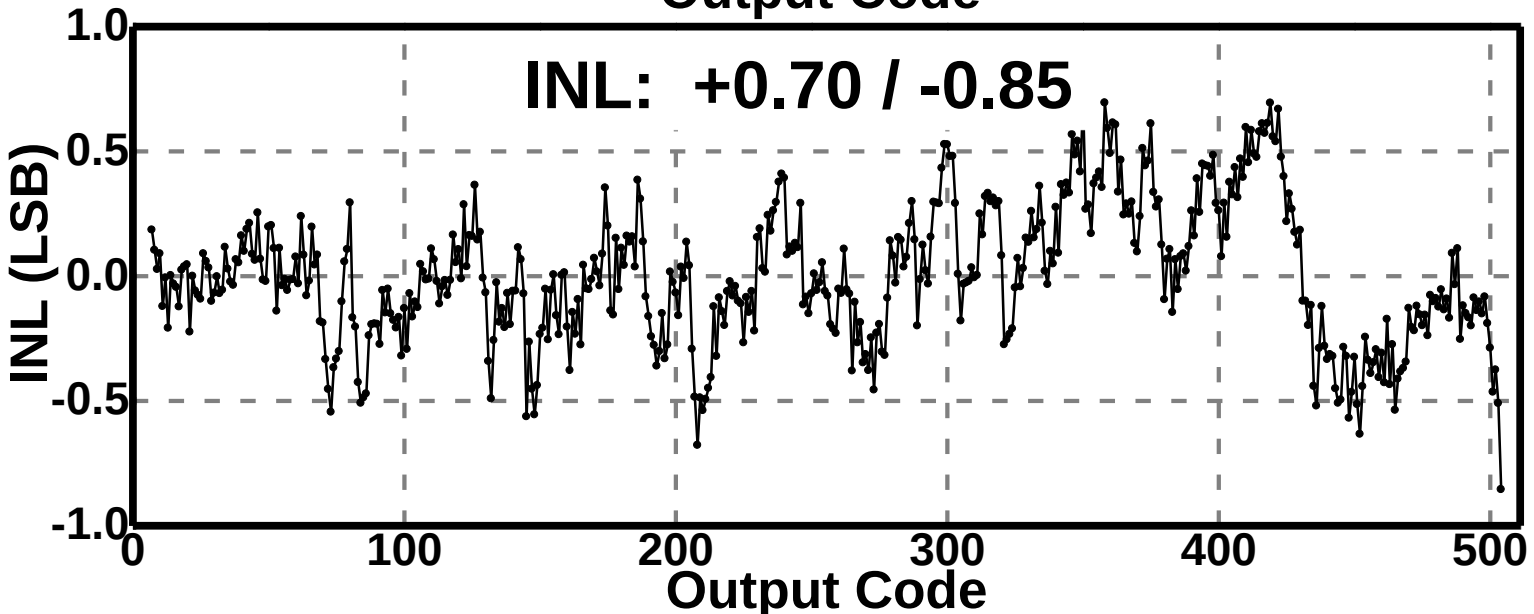
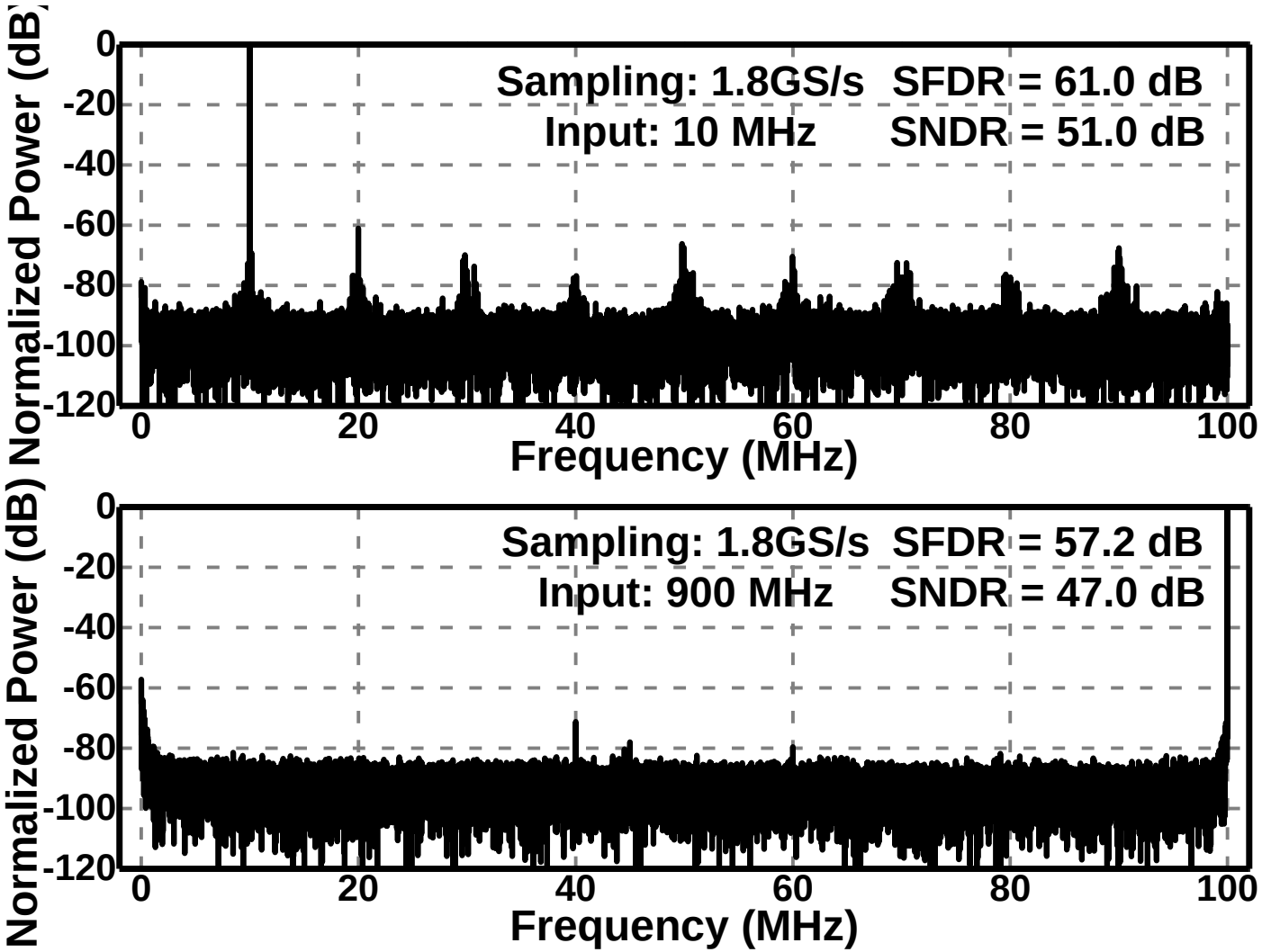
Measured DNL and INL



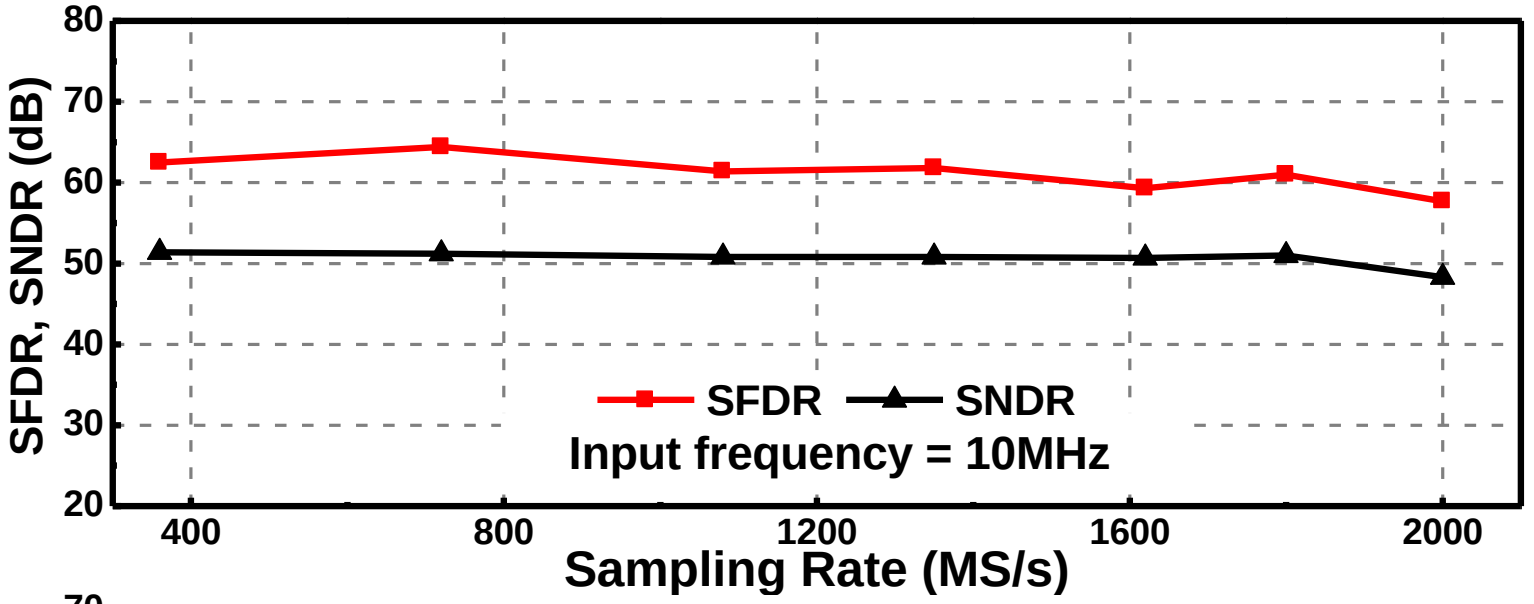


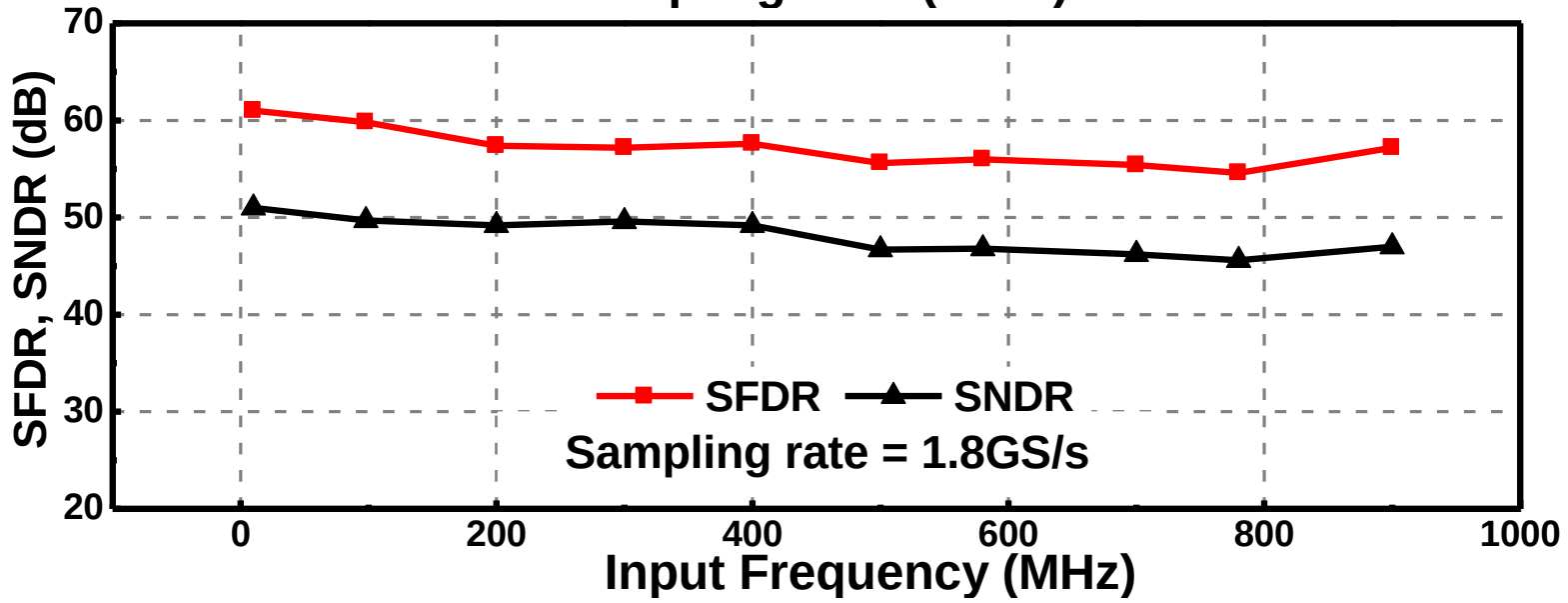
Measured SNDR and SFDR (1/2)

- **Output code is divided by 9**



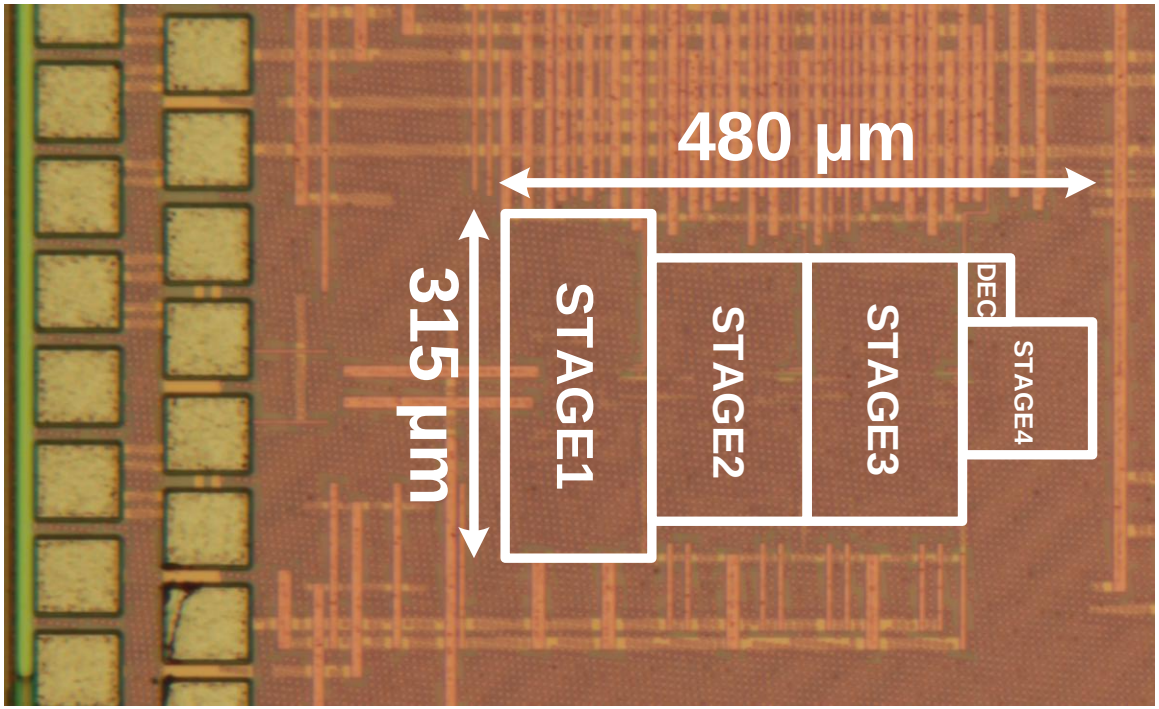
Measured SNDR and SFDR (2/2)





Chip Photo

- **Prototype ADC is fabricated in 65 nm CMOS**
- **The occupied active area is 0.15 mm^2**



Performance Comparison

- **Pipelined ADCs with similar resolution and sampling rate**

	VLSI 2013 [5]	CICC 2013 [6]	VLSI 2011 [7]	ESSCIRC 2013 [8]	This work
Architecture	Pipe, closed-loop	Pipe, open-loop	Pipe, closed-loop	Pipe, closed-loop	Pipe, open-loop
Technology	65 nm	65 nm	45 nm	45 nm	65 nm
f_S (GS/s)	0.8	1.0	1.3	2.0	1.8
Resolution (bit)	10	9	7	9	9
Power (mW)	19	7.1	22	45	44
SNDR (dB) Low Freq./ Nyquist	55 / 52	51 / 48	41 / 33	48 / 44	51 / 47
FoM (fJ/c.-s.) @ Low Freq.	53	25	190	116	83
FoM (fJ/c.-s.) @ Nyquist	71	34	460	167	134
Area (mm^2)	0.18	0.1	0.023	0.22	0.15
Amp. Nonlinearity Calibration	Off-chip	Off-chip	No	No	No

[5] Chiang, *et al*., VLSI 2013.
[6] S. Hashemi, *et al*., CICC 2013.
[7] T. Yamase, *et al*., VLSI 2011.
[8] J. Pernillo, *et al*., ESSCIRC 2013.

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Conclusion

- **A 9-bit 1.8 GS/s 44 mW open-loop pipelined ADC is developed.**

- **Proposed:**

Linearization technique, stage gain calibration, top-plate sampling

→ needs no nonlinearity calibration

→ realizes Giga Hertz sampling rate

→ enhances power efficiency

Acknowledgement

This work was partially supported by MIC, Huawei, Mentor Graphics for the use of the Analog FastSPICE (AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

Thank you for your interest!

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