A 3.6 GHz Fractional-N Digital PLL Using SAR-ADC-Based TDC with -110 dBc/Hz In-Band Phase Noise

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Outline

- Motivation
- Phase Detector
- Circuit Design
- Measurement Results
- Conclusion

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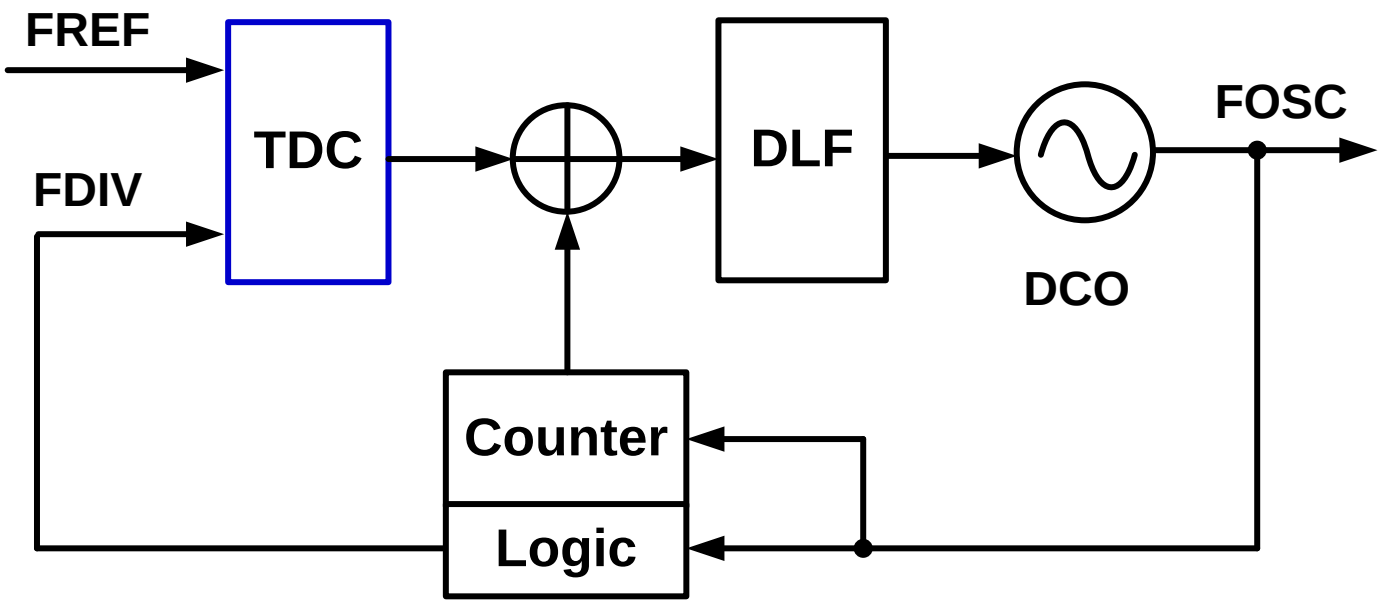
Motivation

- **Digital fractional-N PLL**
  - **Digital friendly, small area, and less folded ΔΣ noise**
  - **The critical building block: TDC**



Motivation

- **A digital PLL with low in-band phase noise**
  - **→ Wide loop BW to relax DCO requirement**
  - **→ Low integrated jitter**

- **Required TDC performance**
  - **– High resolution, sufficient range**
  - **– Low power, and small**

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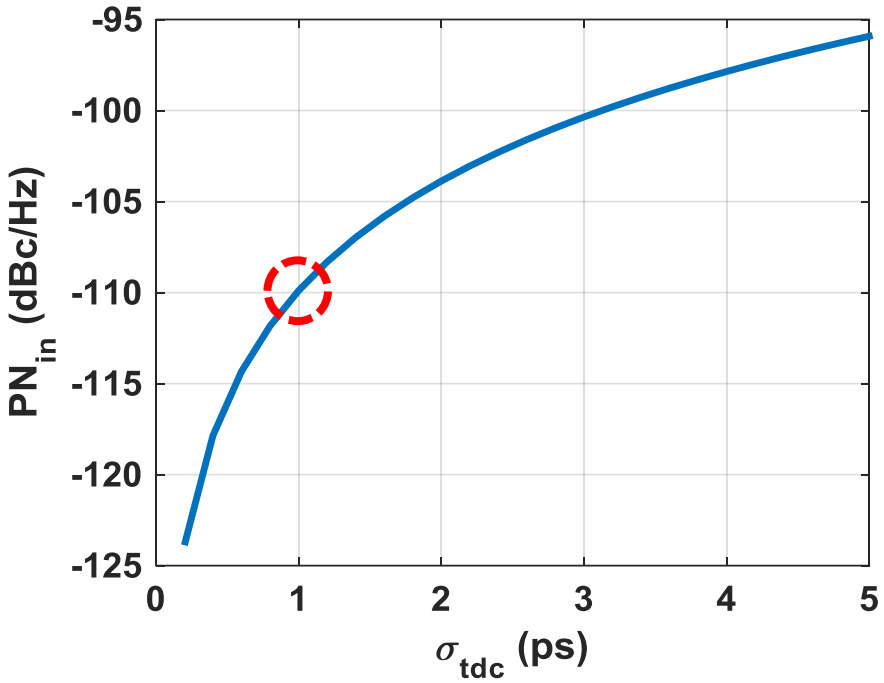
Target PN and TDC Performance

- **High dynamic range TDC is required**

$$PN_{in} = \frac{(2\pi\sigma_{tdc} f_v)^2}{f_{ref}}$$

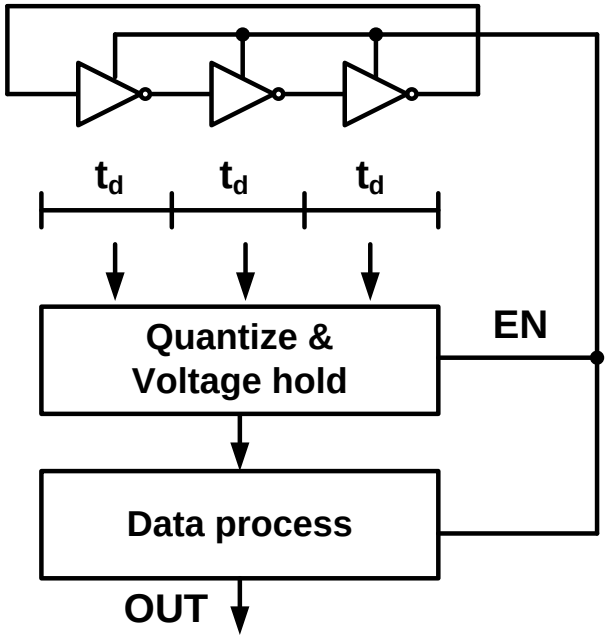
σ_{tdc}: quan. + jitter

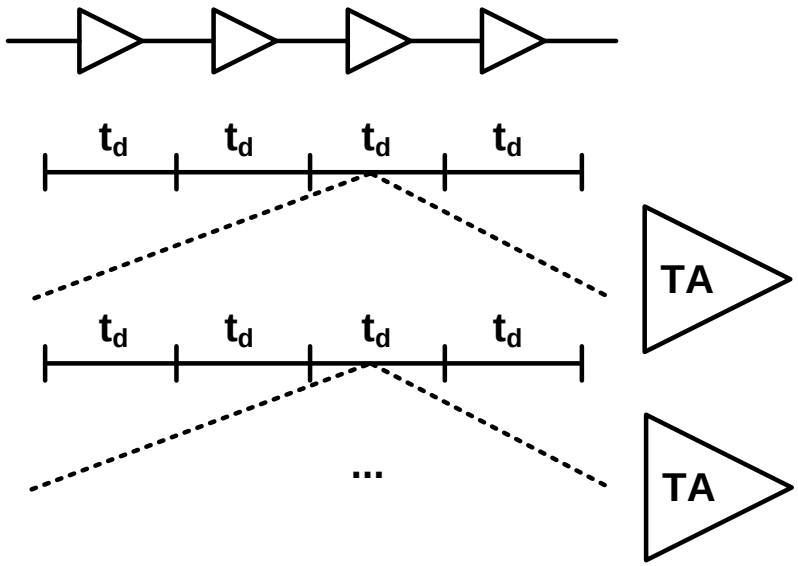


Ref. freq.	50 MHz
Out freq.	3.6 GHz
Target PN_{in}	-110 dBc/Hz
Req. σ_{tdc}	**≤ 1 ps**
Req. range	**> 9 bit**

Previous High Resolution TDCs

- **Noise shaping and sub ranging TDCs**
  - **Complex overhead addressing delay chain's limitation**
  - **Power and area consuming**



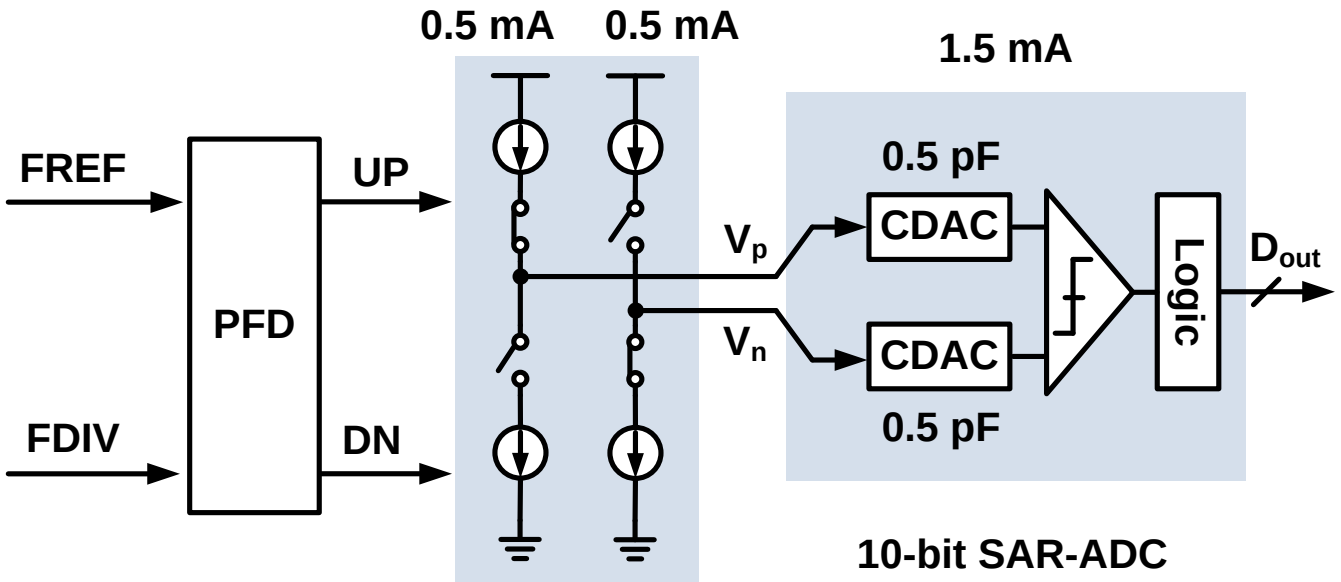


GRO [M. Z. Straayer, JSSC`09]

[M. Lee, JSSC`08]

Previously Proposed TDC

- **PFD and charge pump + SAR-ADC**
  - **No delay chain's limitation**
  - **0.8 ps resolution, 10-bit, ~2.5 mW@50MHz, and 0.018 mm^2**

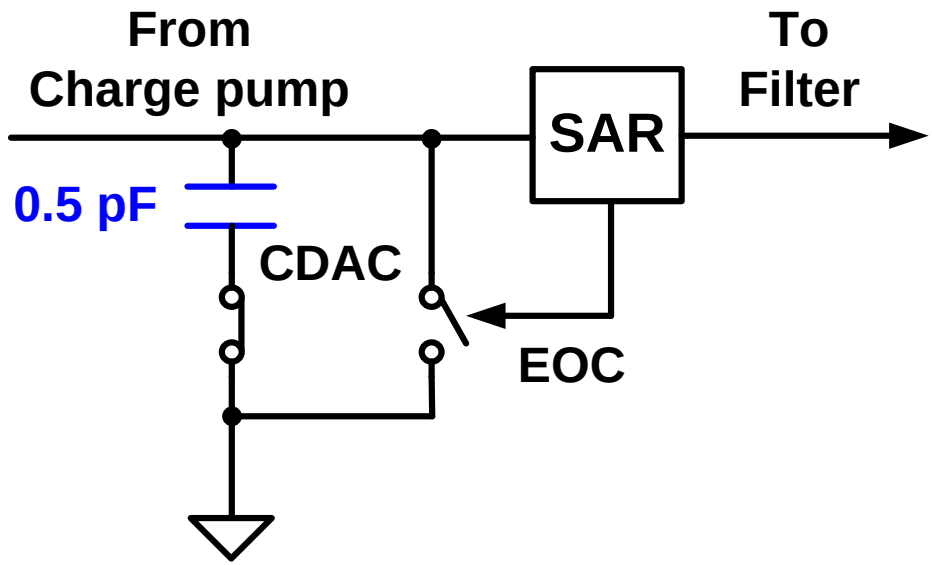


[Z. Xu, CICC`13] [Z. Xu, SSDM`14]

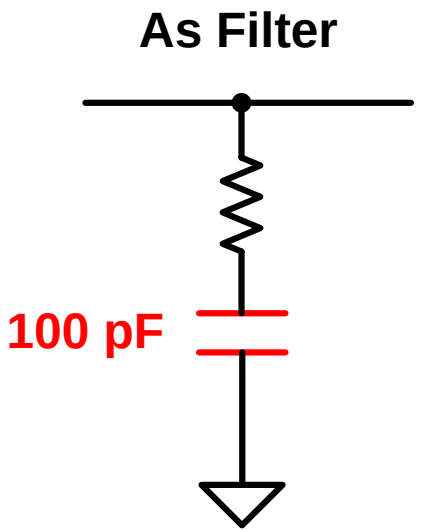
When Applied in Digital PLL

- Not used for filtering
- → Smaller area

This work

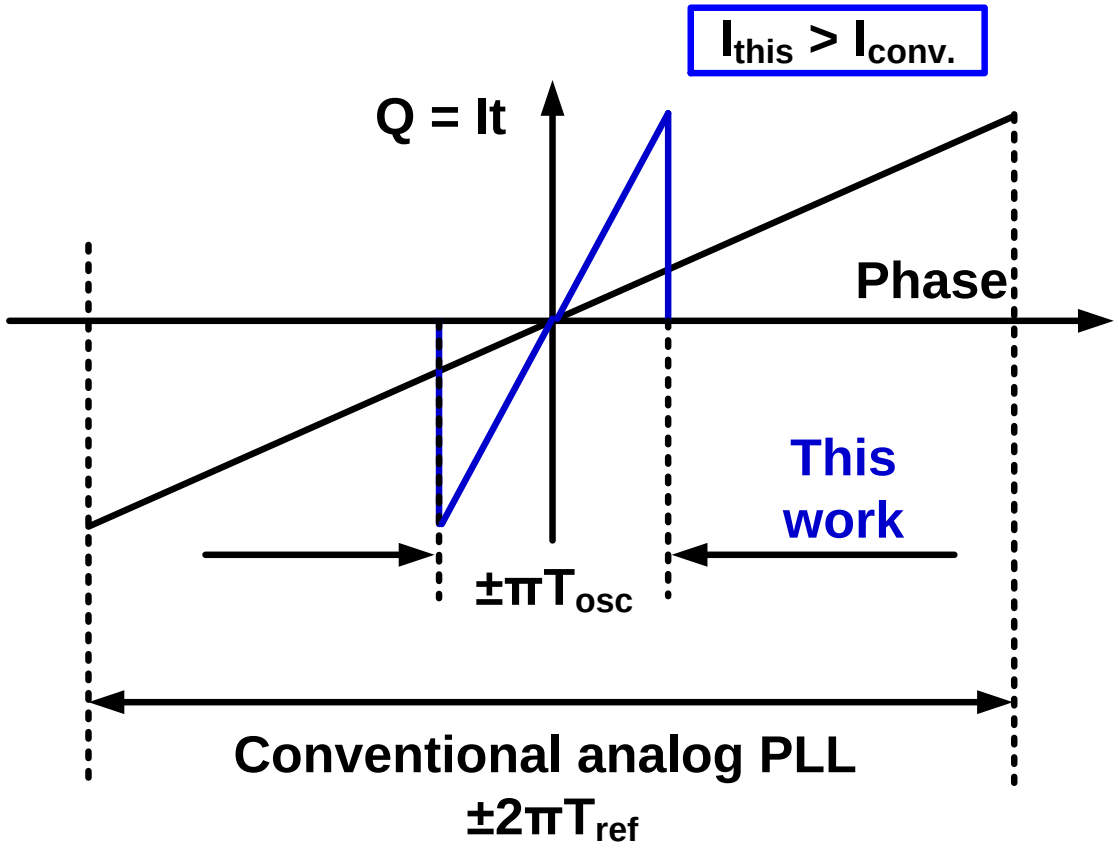


Analog one



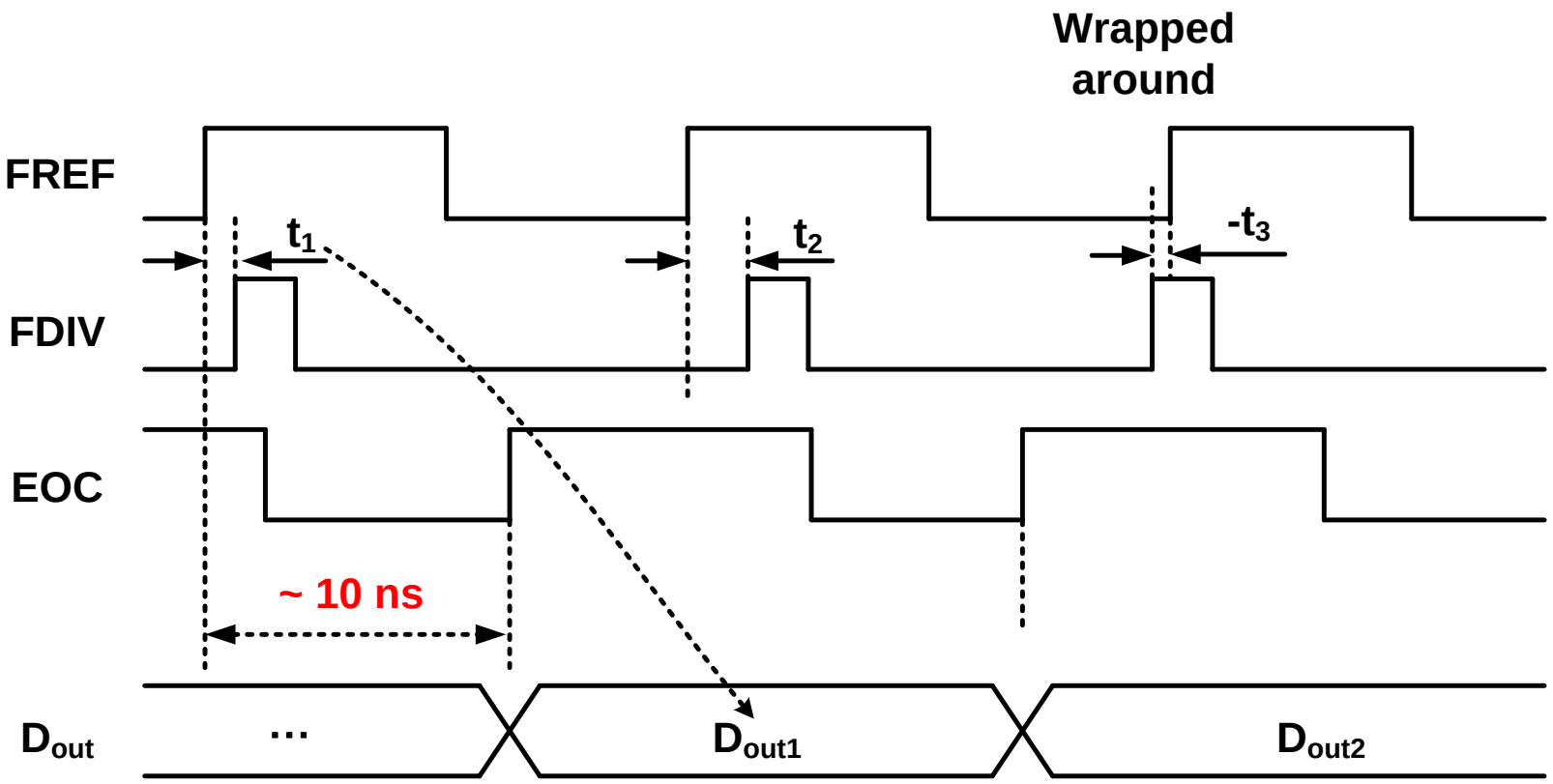
When Applied in Digital PLL

- Not used for acquisition
- → Higher detection gain (resolution)



To Accommodate the TDC

- **Conversion latency SAR-ADC**
- **Phase needs to be wrapped around**



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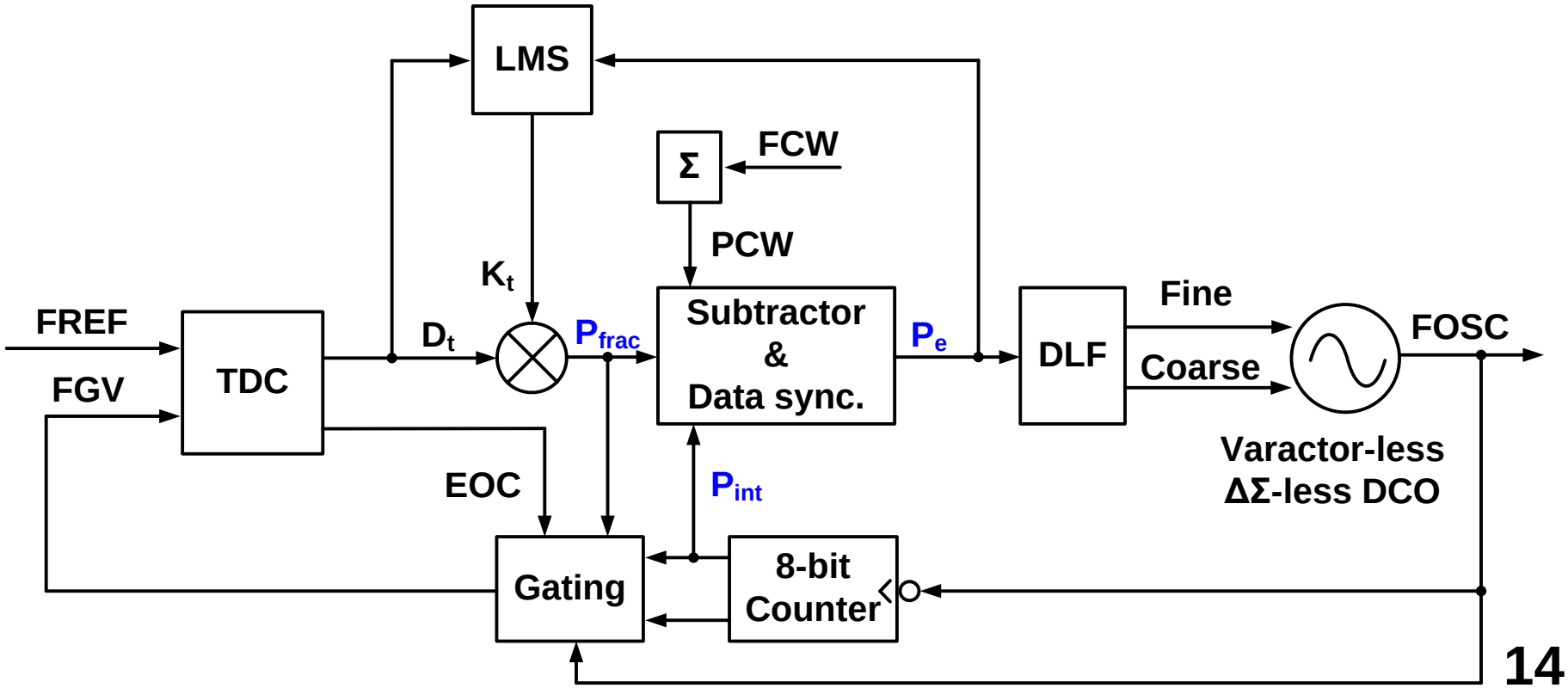
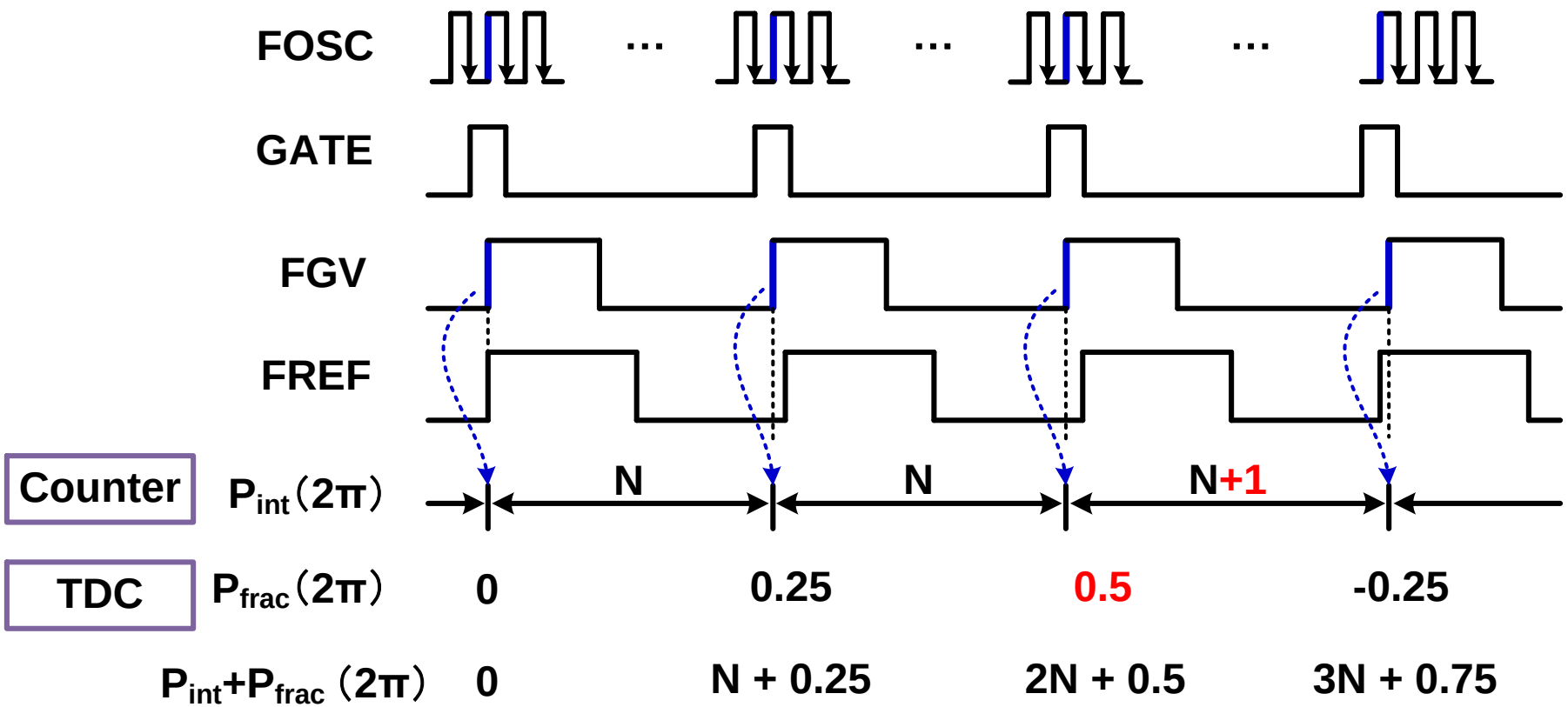
Architecture

- Counter-based architecture
- Gating FOSC addressing TDC's latency issue

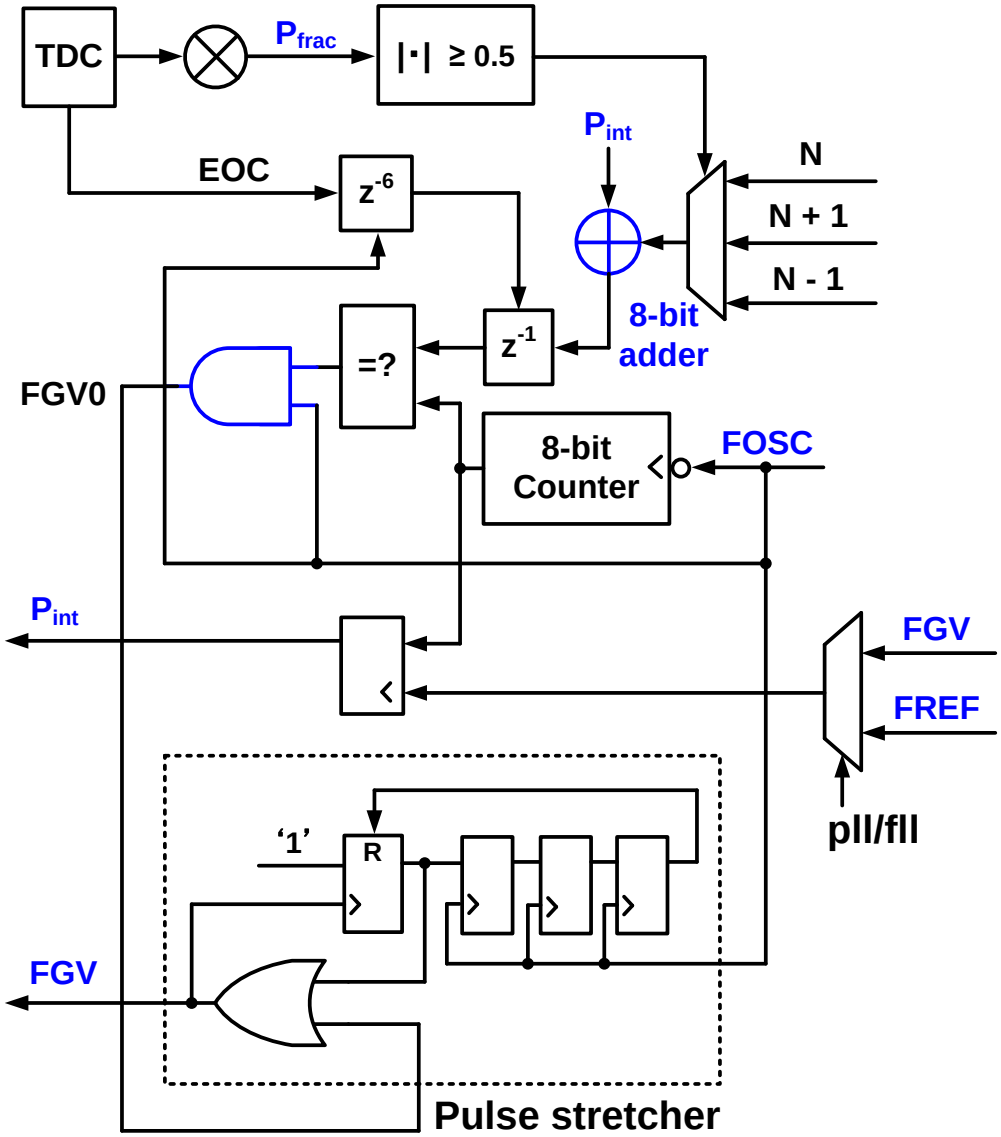


Pulse Gating

- **Similar behavior as that of a synchronous divider**



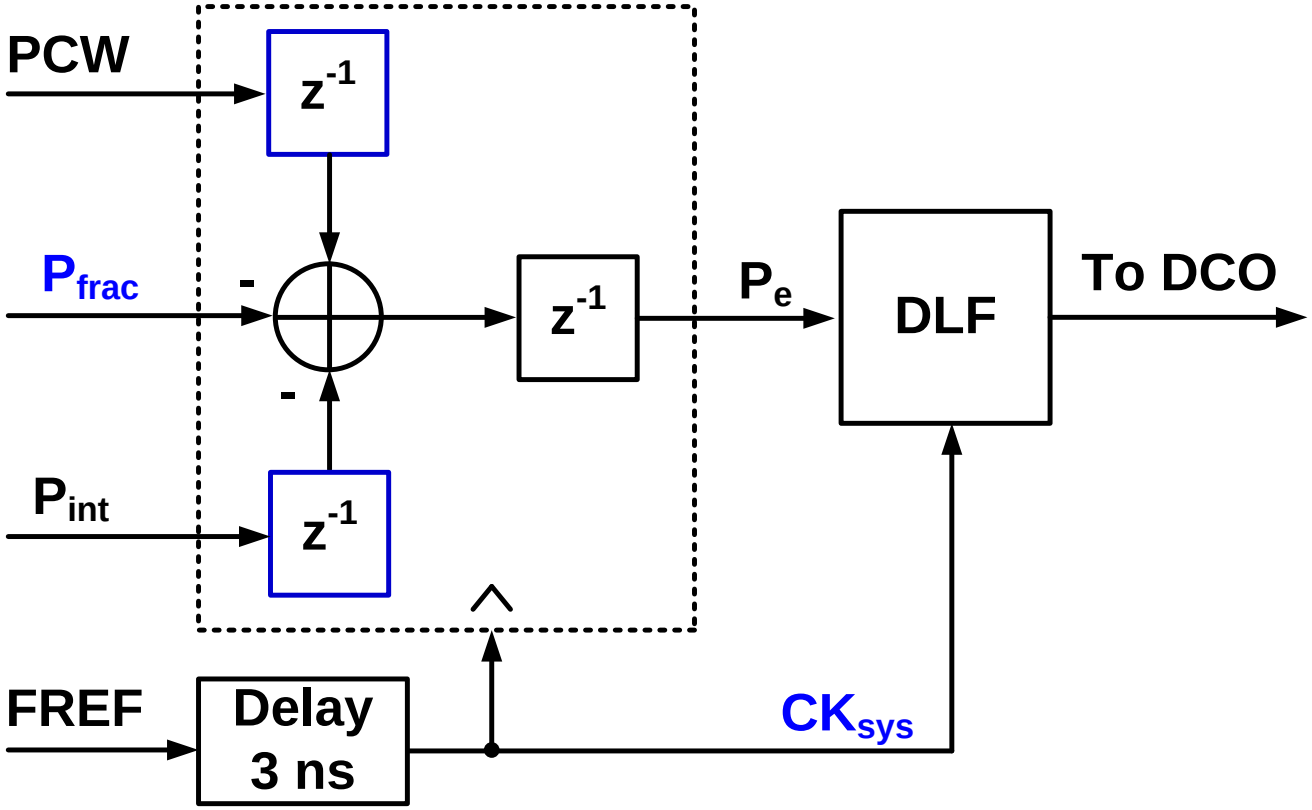
Pulse Gating



- **Same adder bit width as that of the counter**
- **Re-sample target value using delayed EOC**
- **Need no clock re-timer**

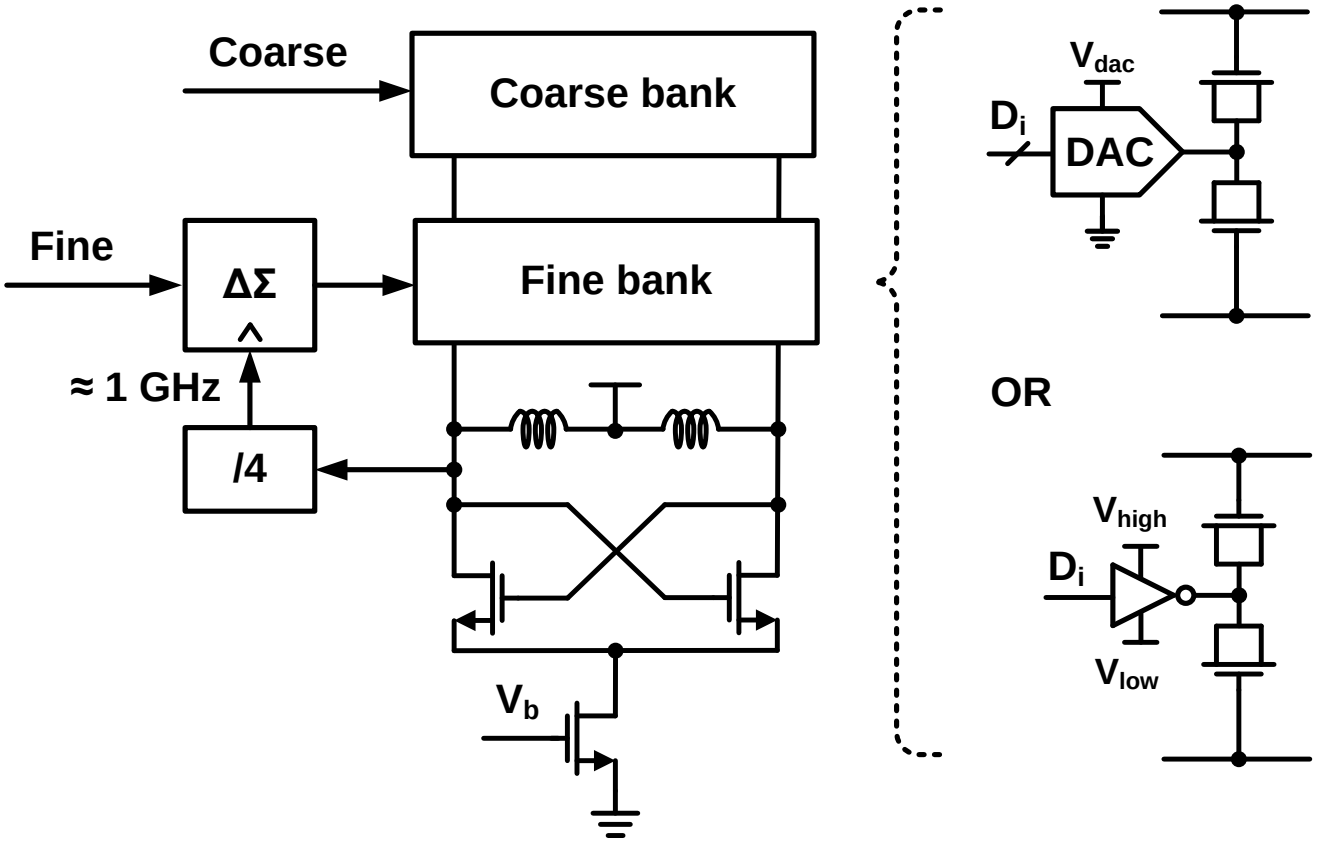
Data Synchronization

- **One more cycle delay in the loop, but not harmful to the stability**



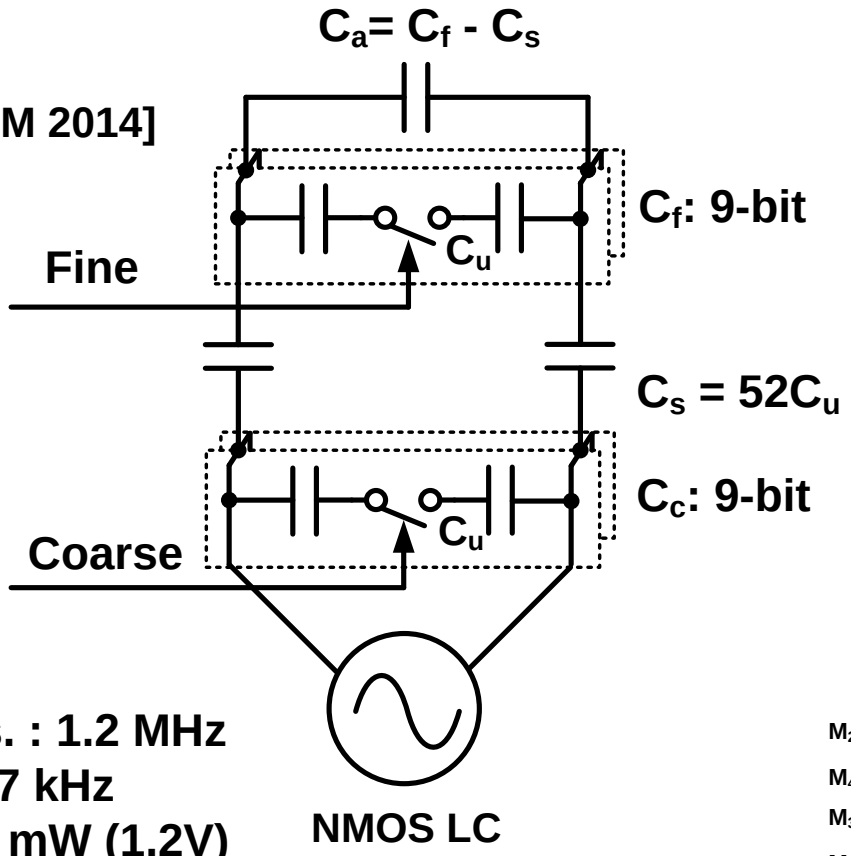
Conventional DCOs

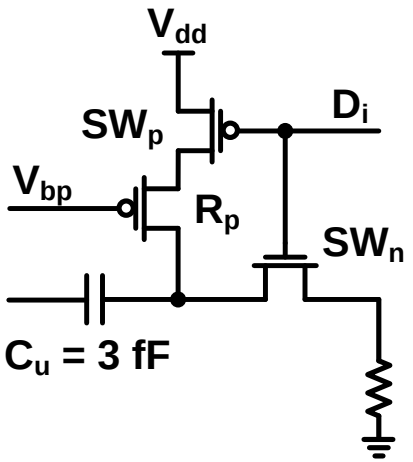
- **Extra power and noise from ΔΣ modulator**
- **Voltage-sensitive MOS varactors**

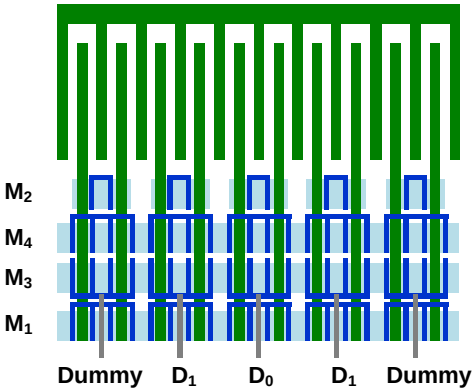


DCO in This Work

- **Only switched MOM capacitors**
- **Capacitive bridging for fine resolution**







Coarse res. : 1.2 MHz
Fine res. : 7 kHz
Power: 4.8 mW (1.2V)
Area: 0.26 mm^2

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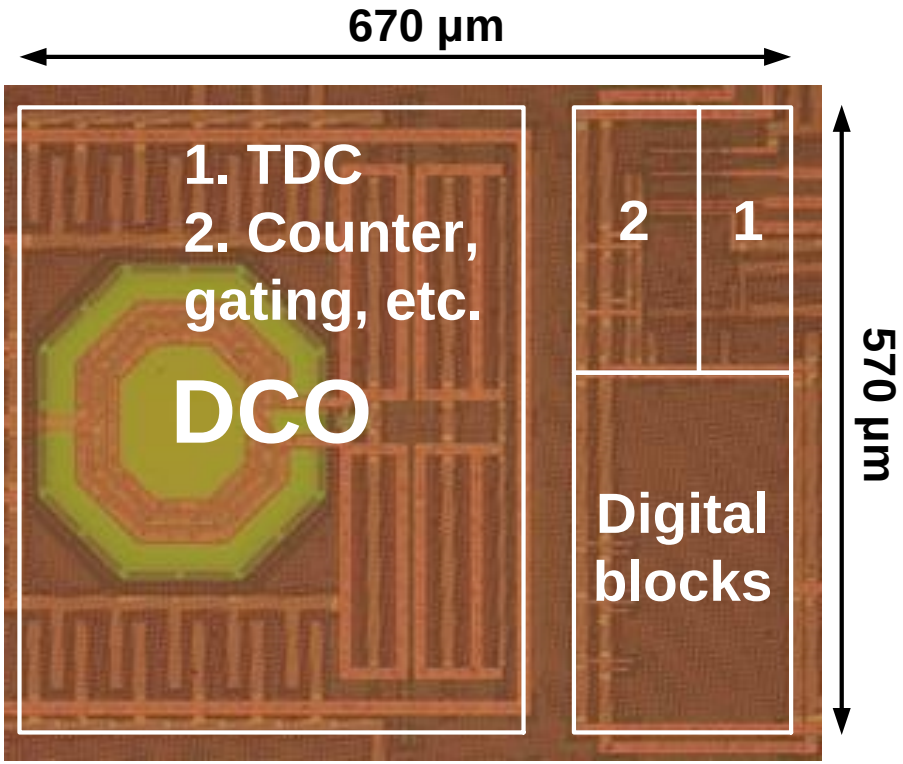
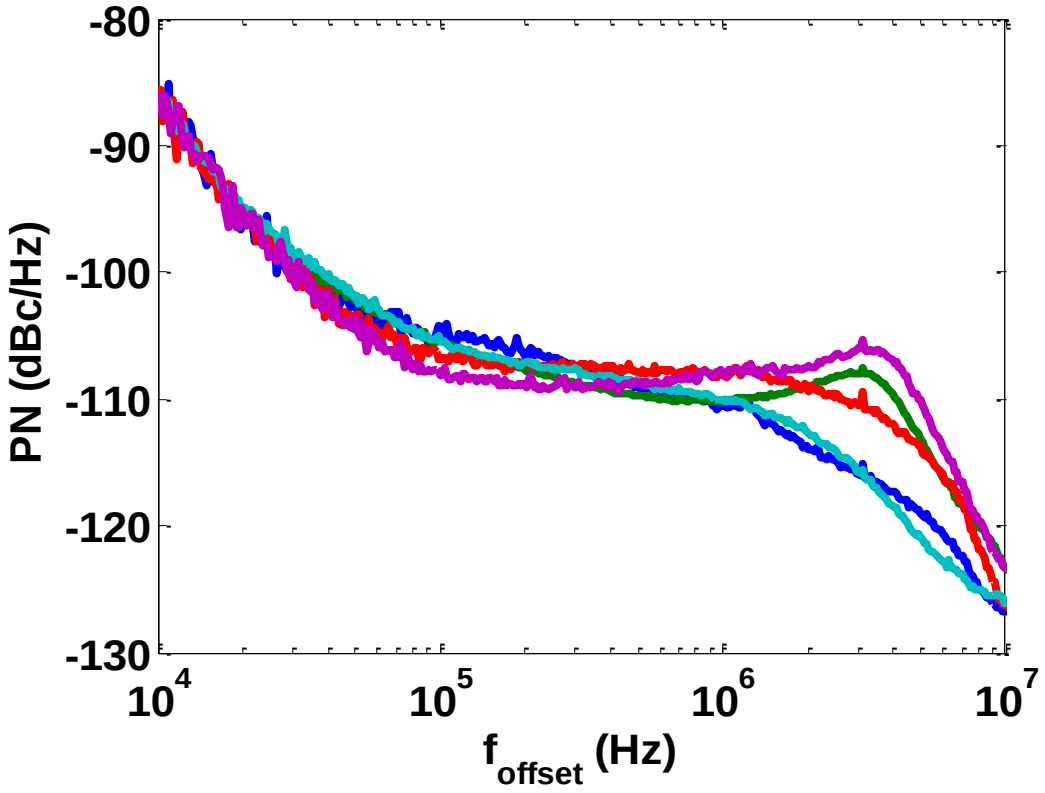
Implementation



- CMOS 65 nm
- Core area: 0.38 mm^2
- Supply voltage: 1 V
- Power (50 MHz ref.): 9.7 mW

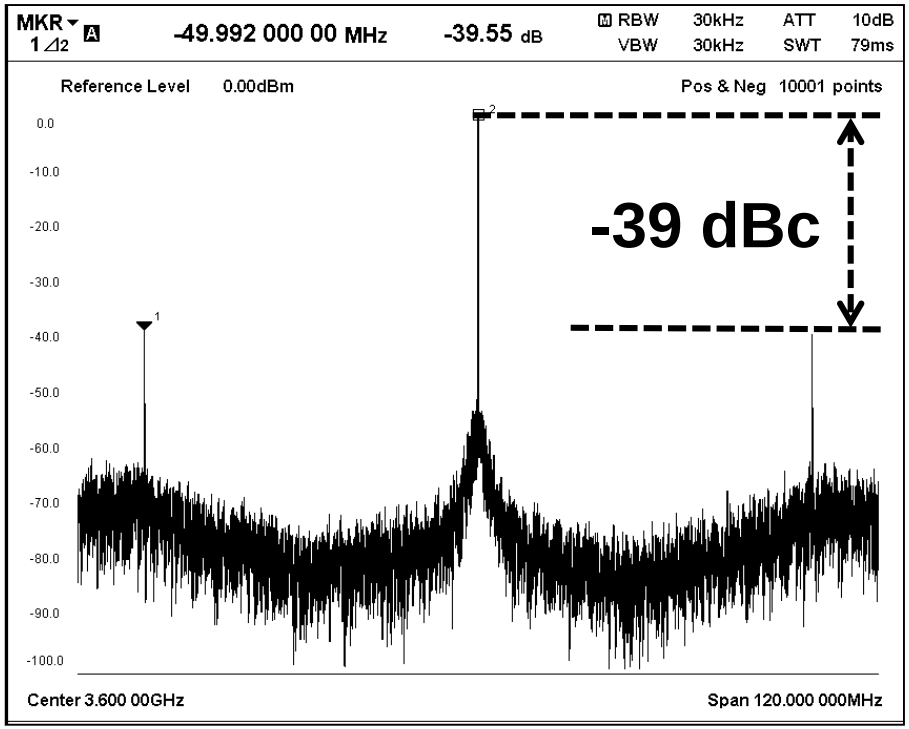
In-Band Phase Noise @3.625 GHz

- **Loop BW: 1 – 5.4 MHz**
- **In-Band PN: -107 – -110 dBc/Hz, consistent with measured TDC's resolution**

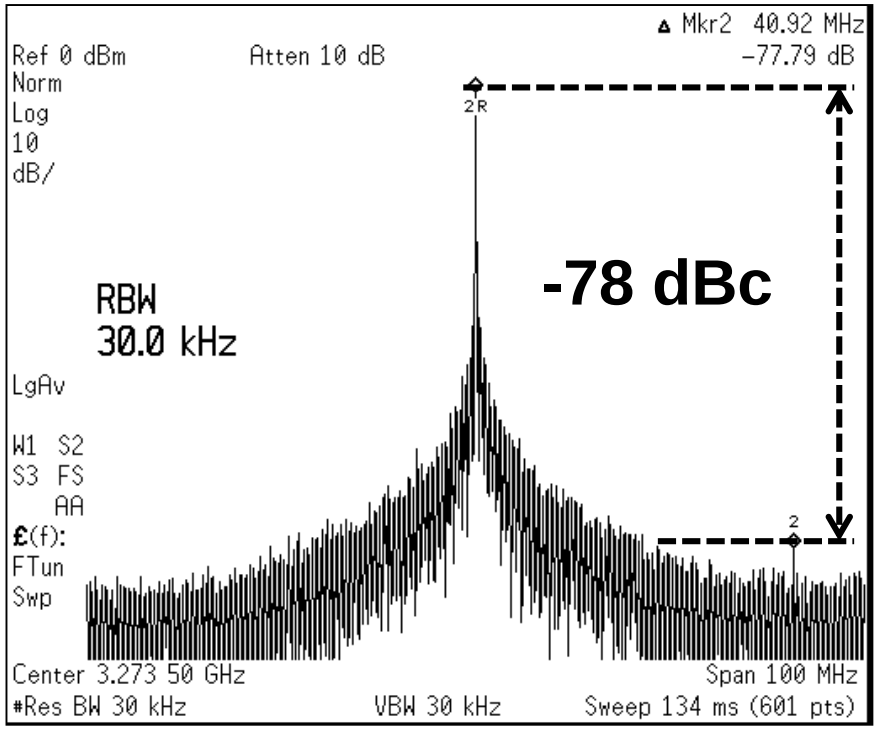


Reference Spur

-39 dBc reference spur due to improper grounding and output buffer



Improved grounding and output buffer in our another work



Performance Comparison

- **Comparable in-band phase noise**
- **Lower power/area consumption**

	This work		Venerus JSSC`15 [6]	Yao JSSC`13 [5]	Hsu JSSC`08 [2]	Lee JSSC`09 [3]
CMOS (nm)	65		65	180	130	65
Technique	Charge pump + SAR-ADC		ΔΣ FDC using ADC	GRO +ADC	GRO	TA
Out. Freq. (GHz)	3.625 (3.3 – 3.8)		3.5 (2.8 – 3.5)	3.2 (2.8 – 3.2)	3.67 (N/A)	1.6824 (N/A)
Ref. Freq. (MHz)	50		26	52	50	25
Loop BW (MHz)	5	2	0.04	0.95	0.5	0.7
In. PN (dBc/Hz)	-110.0	-108.3	-70	-108.4	-108.0	-116
RMS Jitter (fs)	560	415	N/A	230 (1k – 40 MHz)	204 (1k – 40 MHz)	495 (1k – 10 MHz)
	(10k – 10 MHz)					
FoM (dB)	-235.1	-237.8	N/A	-240.4	-237.1	-225.3
Power (mW)	9.7		21.0	17.0	39	121.0
Area (mm^2)	0.38		0.56	0.62	0.95	2.25

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Conclusion

- **Digital fractional-N PLL with -110 dBc/Hz phase noise, consistent with TDC's resolution, 9.7 mW, and 0.38 mm^2**
- **0.8 ps-resolution TDC with low-power and small area using charge pump and SAR-ADC, accommodated without divider+ΔΣ-modulator**
- **ΔΣ-less and varactor-less DCO using bridging capacitor enhancing frequency resolution**

Acknowledgement

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Thank you for your interest!

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