Substrate Noise Isolation Improvement by Helium-3 Ion Irradiation Technique in a Triple-well CMOS Process

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Outline

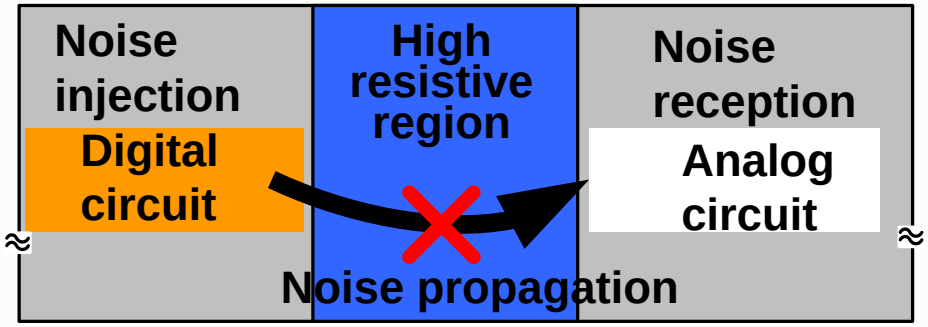
- **Background**
- **Methods to improve isolation**
- **Helium-3 ion irradiation**
- **Simulation results**
- **Experimental results**
- **Conclusion**

Background

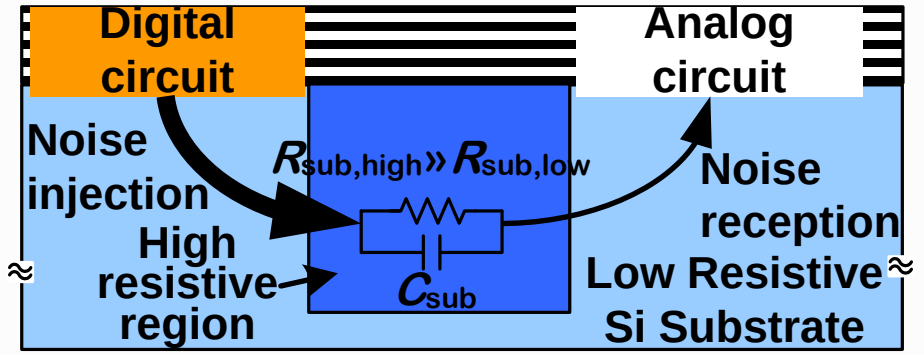
- **Analog and digital circuits are integrated on the same chip.**
- **Increase of digital circuit speed causes more substrate noise coupling problems.**
- **Analog circuit supply voltage decreases.**

Methods to Improve Isolation

- **Decreasing noise injection and noise reception**
  - Guard rings
- **Cutting the propagation path**
  - Silicon on insulator (SOI)
    - High cost
  - Proton bombardment
    - High cost
  - Helium-3 ion irradiation



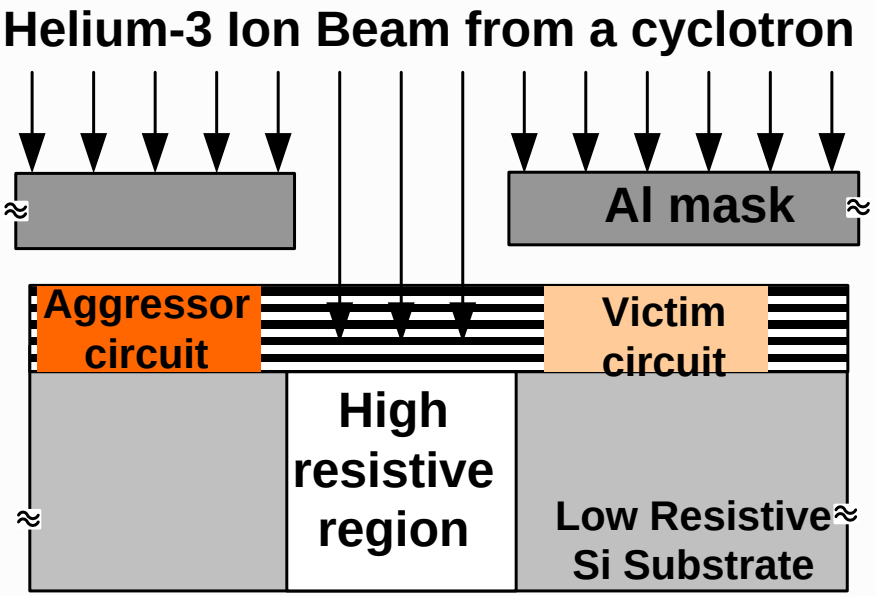
Top view



Cross view

Helium-3 Ion Irradiation

- Cutting the propagation path by increasing the substrate resistivity
- Can be integrated into the standard process
- The design margin is about 15-μm for active device [1].



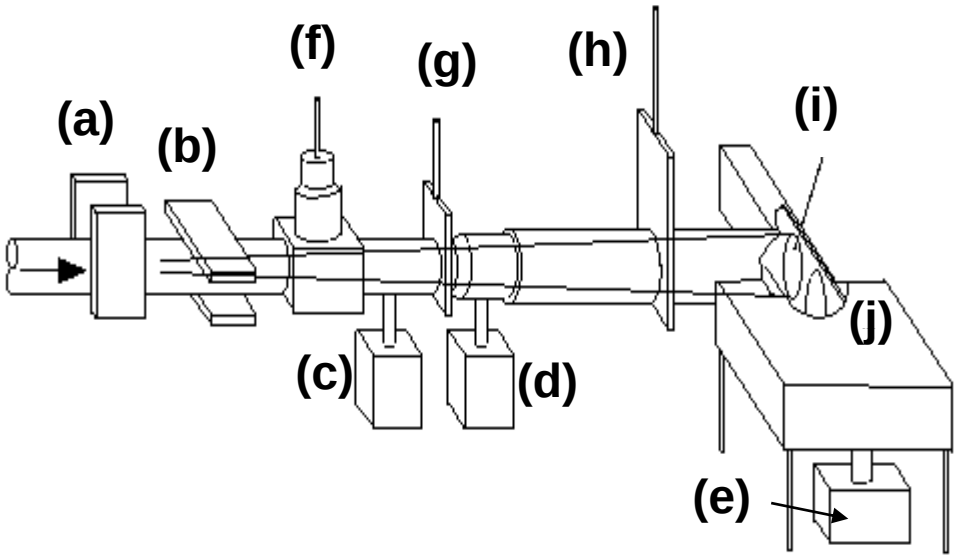
Helium-3 bombardment from front side to create a high resistive region

Helium-3

- high irradiation efficiency
- small dose
- low process cost

Ref: [1] Ning Li, et al., TED, vol. 62, no. 4, April 2015.

Helium-3 Ion Irradiation Machine



Configuration of Irradiation System

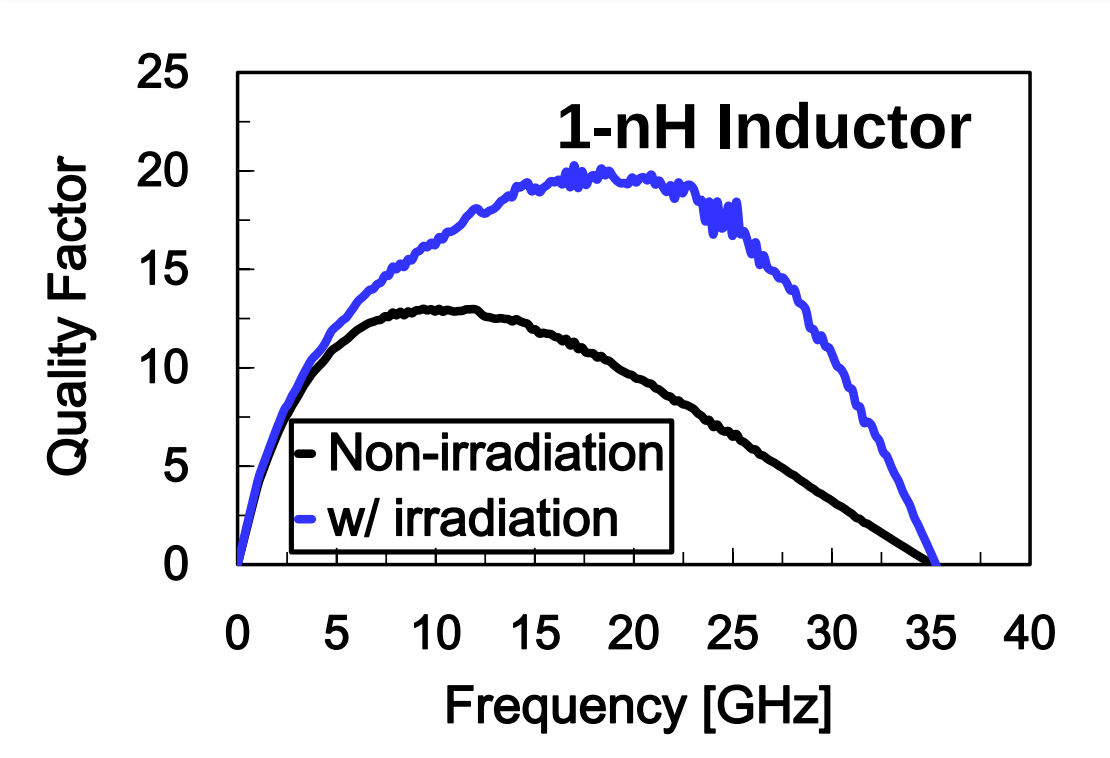
Ion irradiation machine

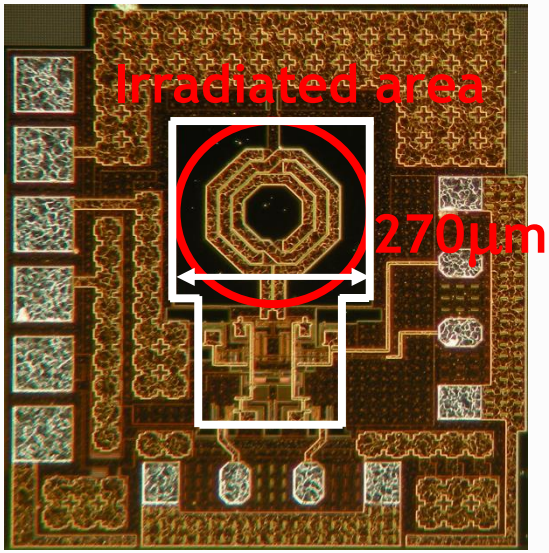
(a), (b):	Vertical/horizontal scanning magnets
(c), (d), (e):	Turbomolecular pumps
(f):	Beam shutter
(g), (h):	wafer gate valves
(i):	Wafer
(j):	Automatic wafer handling device

Ref: https://www.shiei.co.jp/english/cyclotron_iis.html

Helium-3 Ion Irradiation Applications

- For inductor
  - Improving inductor quality factor
- For voltage controlled oscillator
  - 8.5dB improvement in phase noise



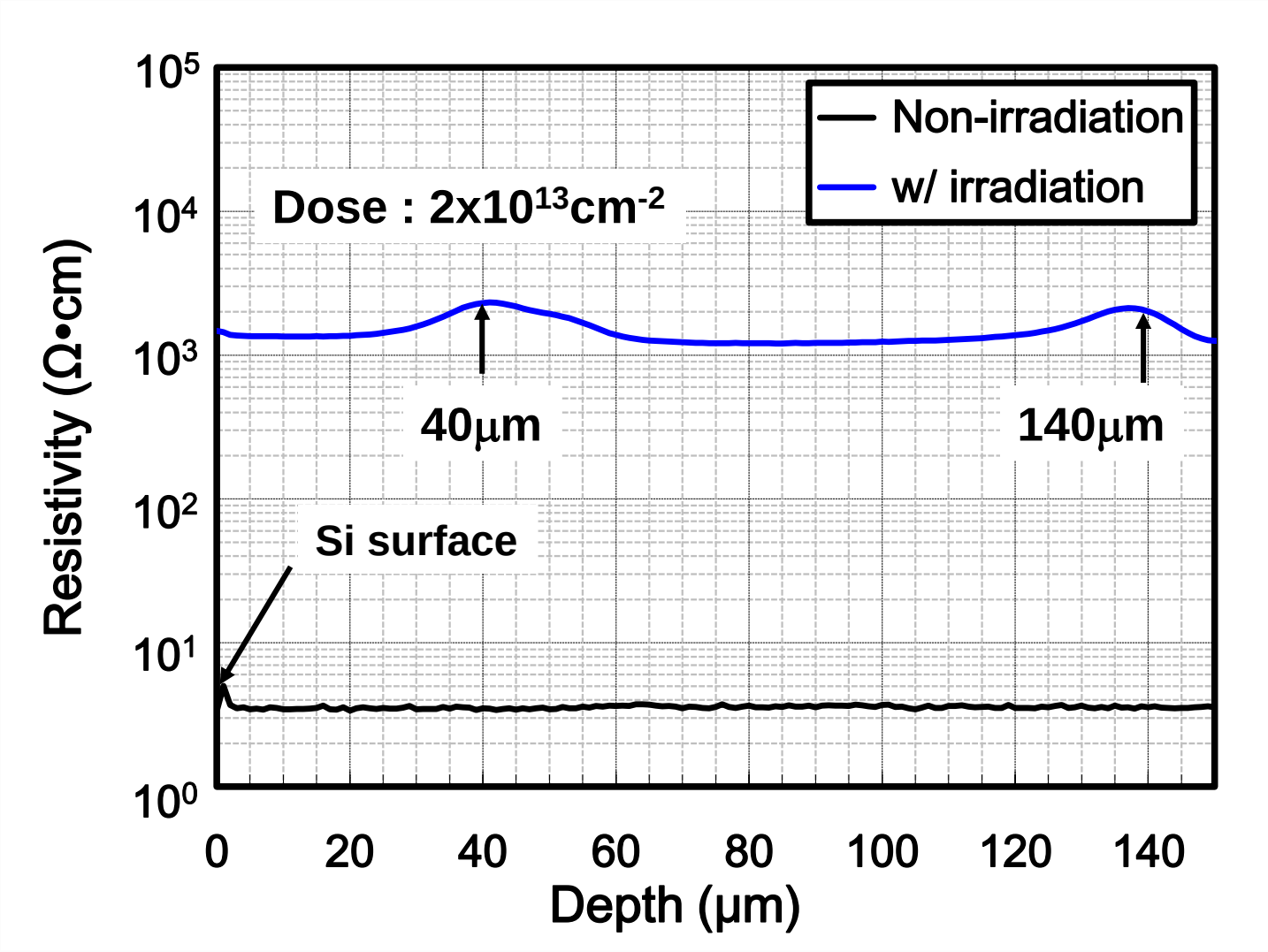


Voltage controlled oscillator

Ref.: Ning Li, et al., TED, vol. 62, no. 4, April 2015.

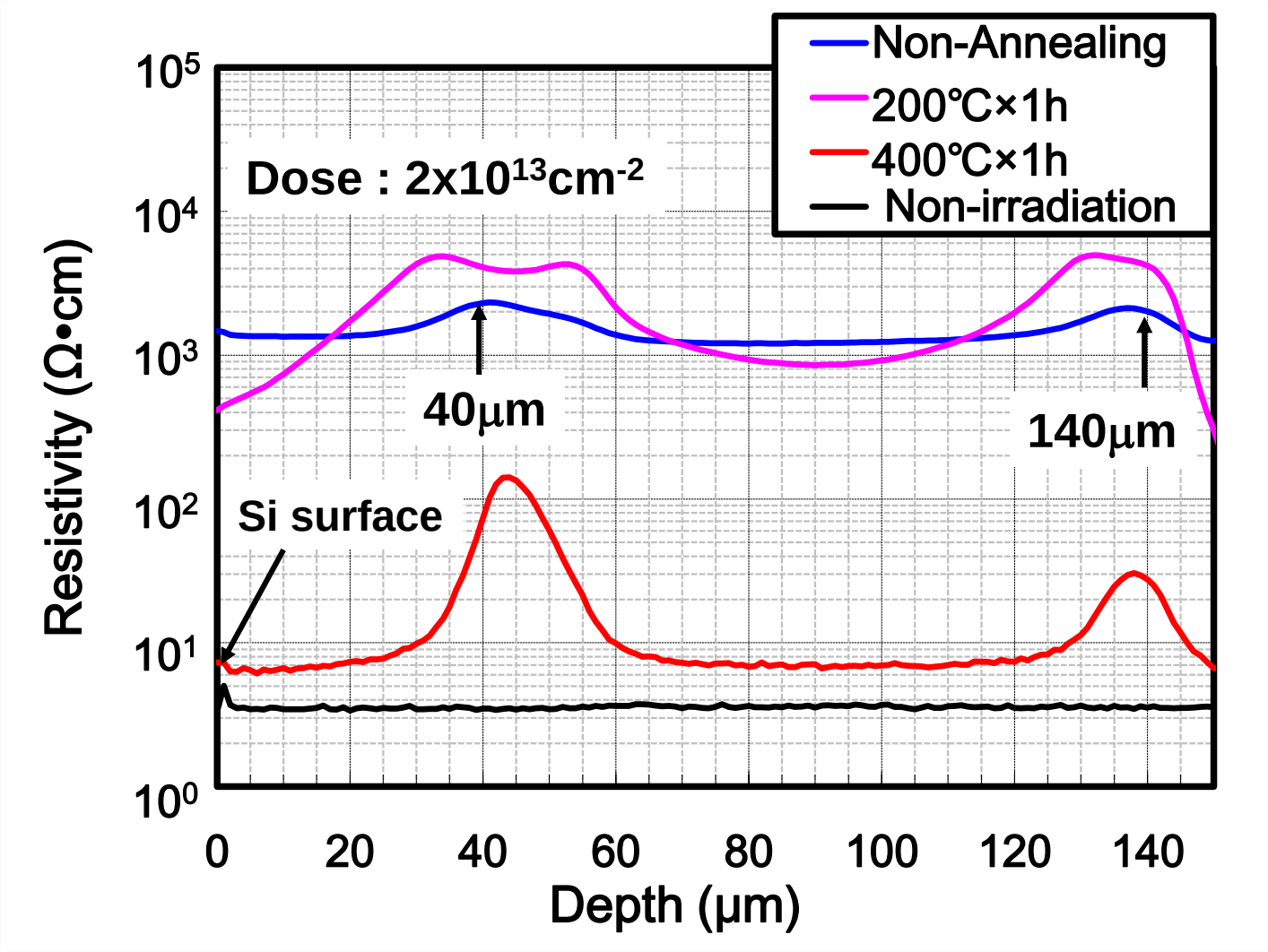
Substrate Resistivity

- **Resistivity after helium-3 ion irradiation**



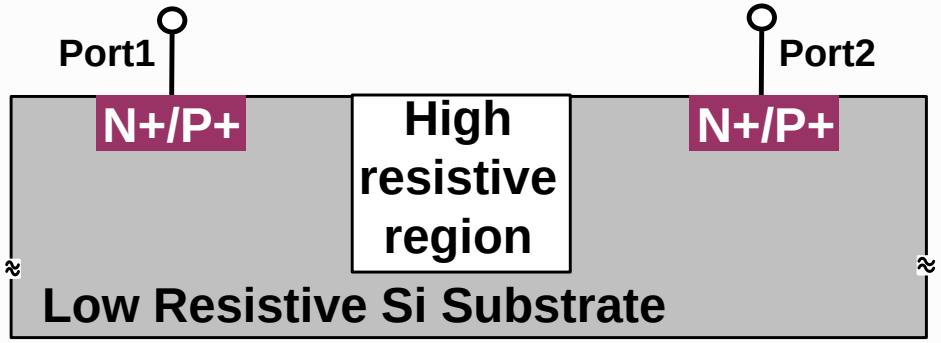
Substrate Resistivity Cont'd

- **Resistivity after annealing at 200ºC and 400ºC for 1h.**

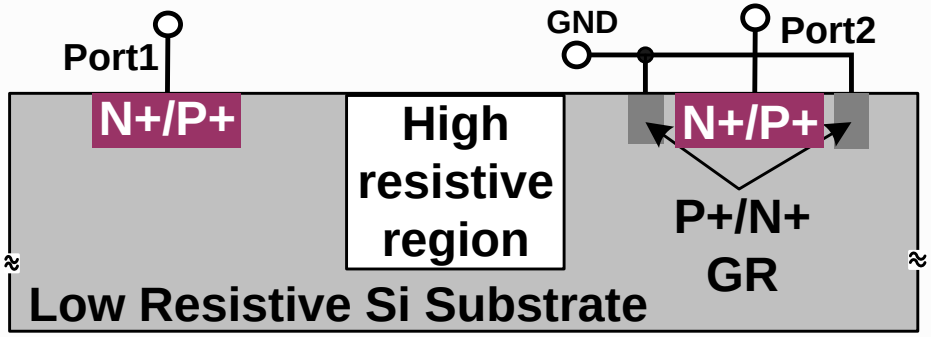


Isolation Test

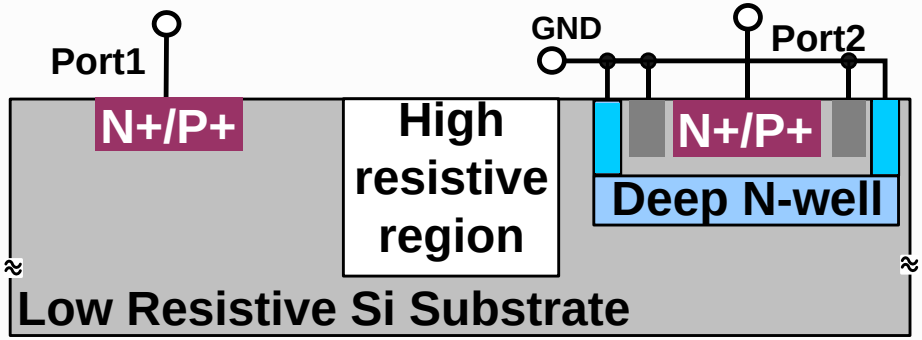
(a) diffusion taps



(b) diffusion tap with guard ring at one side

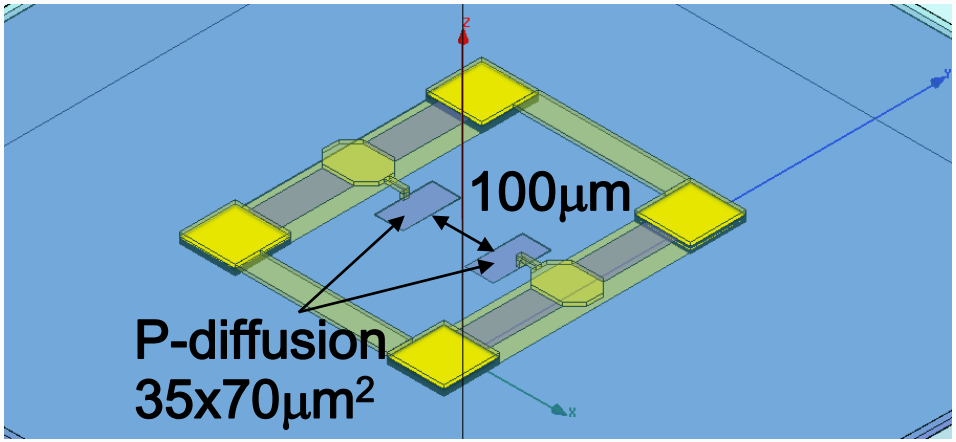


(c) diffusion tap with deep n-well (DNW) guard ring (GR) at one side

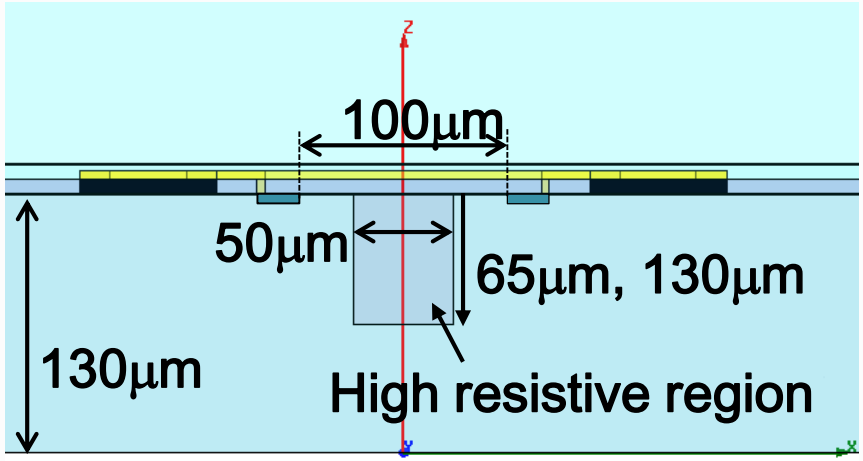


EM Simulation

- EM simulator
  - HFSS
- Two-port
- P-diff. taps
  - Area: 35x70μm²
  - Distance: 100μm
- High resistive region
  - Width: 50μm
  - Thickness
    - 65μm
    - 130μm



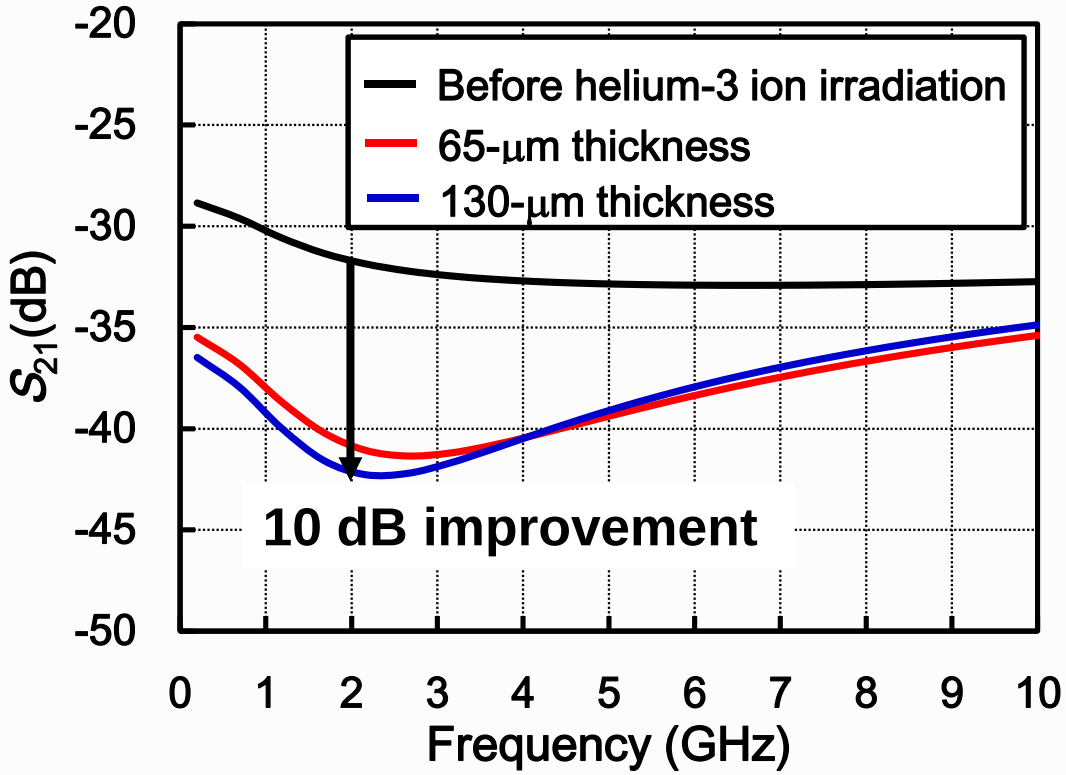
Top view



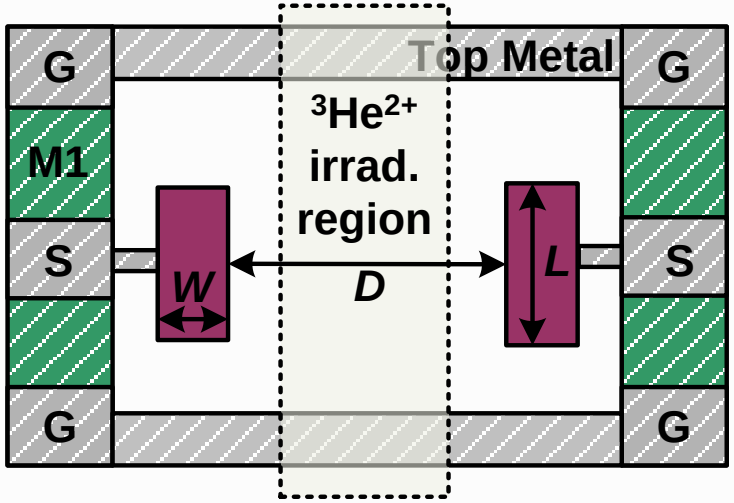
Cross view

Simulation Results

- **A 10-dB improvement at 2GHz**
- **As frequency increases, the improvement decreases due to the capacitive coupling**



Test Patterns



Top view of test structures

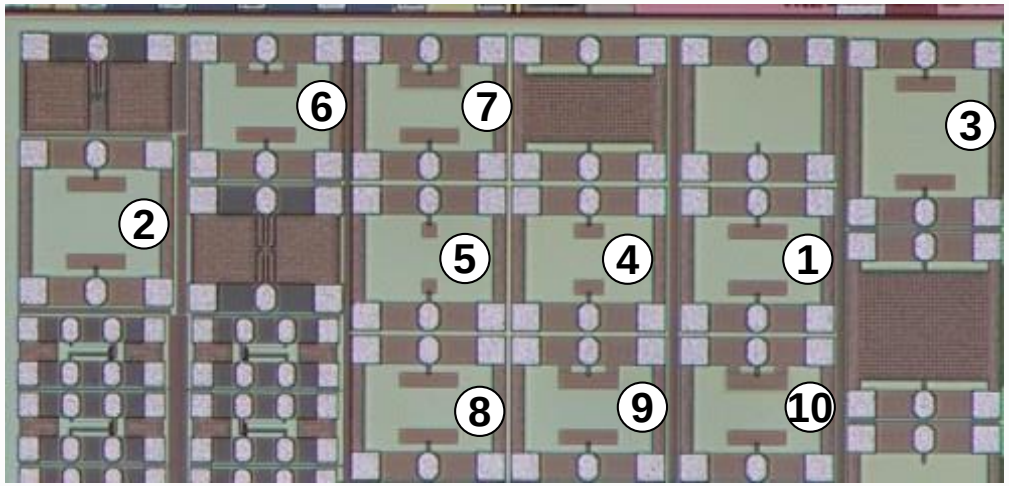
- ***W*: diffusion width**
- ***L*: diffusion length**
- ***D*: diffusion taps distance**

	Size (W*L) (μm^2)	Diff.	Guard Ring (GR)	Dist. (μm)
①	35*140	N+	None	100
②	35*140	N+	None	150
③	35*140	N+	None	200
④	35*70	N+	None	100
⑤	35*35	N+	None	100
⑥	35*140	N+	P+ GR	100
⑦	35*140	N+	P+ GR and DNW	100
⑧	35*140	P+	None	100
⑨	35*140	P+	N+ GR	100
⑩	35*140	P+	N+ GR and DNW	100

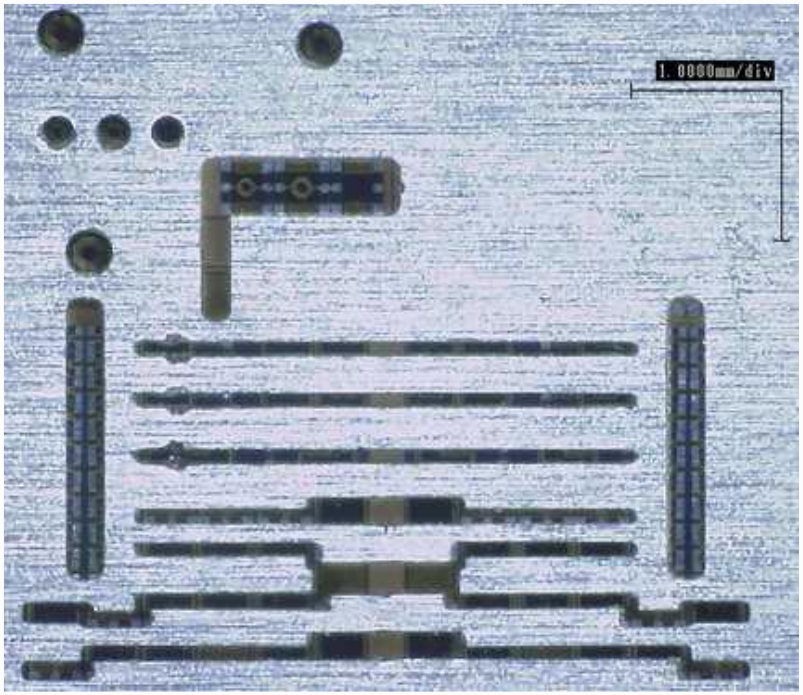
DNW: deep n-well

Chip Photo

- A 180-nm standard CMOS process
- Substrate resistivity about 3~4 Ω·cm



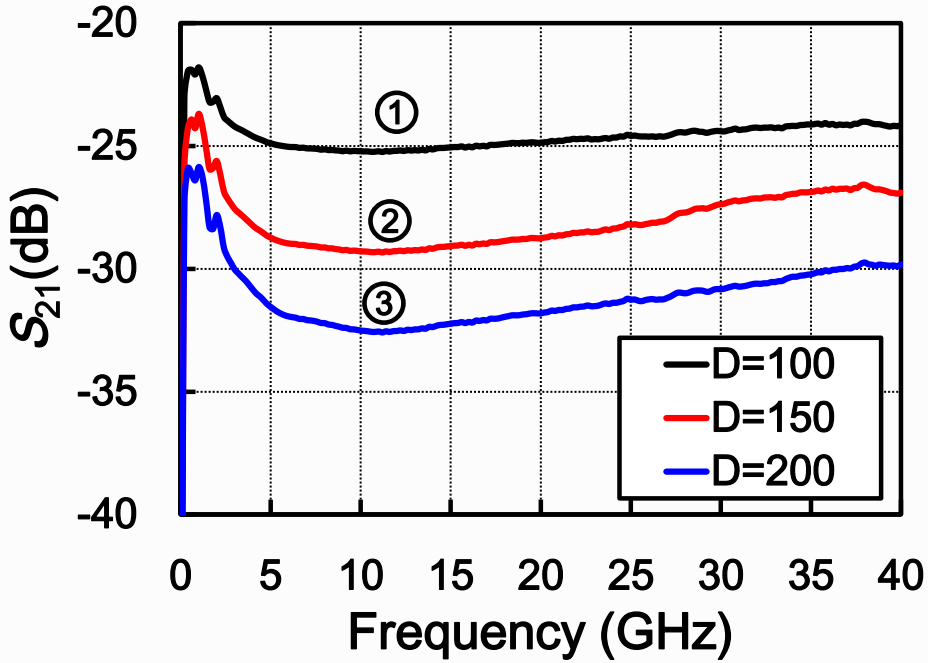
Chip photo

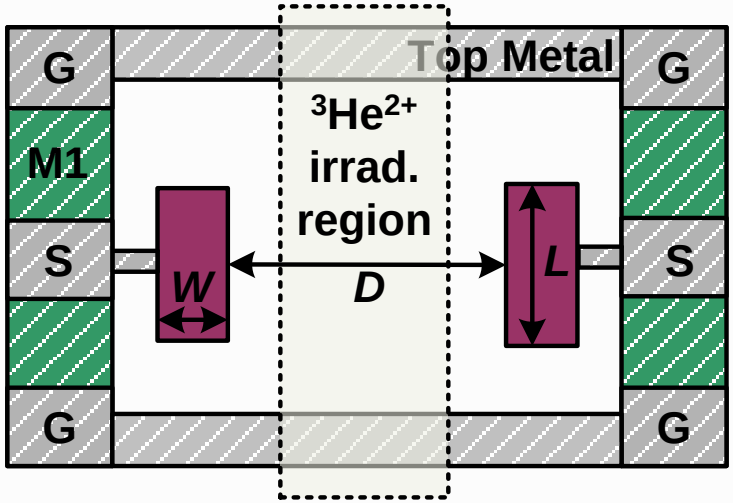


Mask

Measurement Results (1)

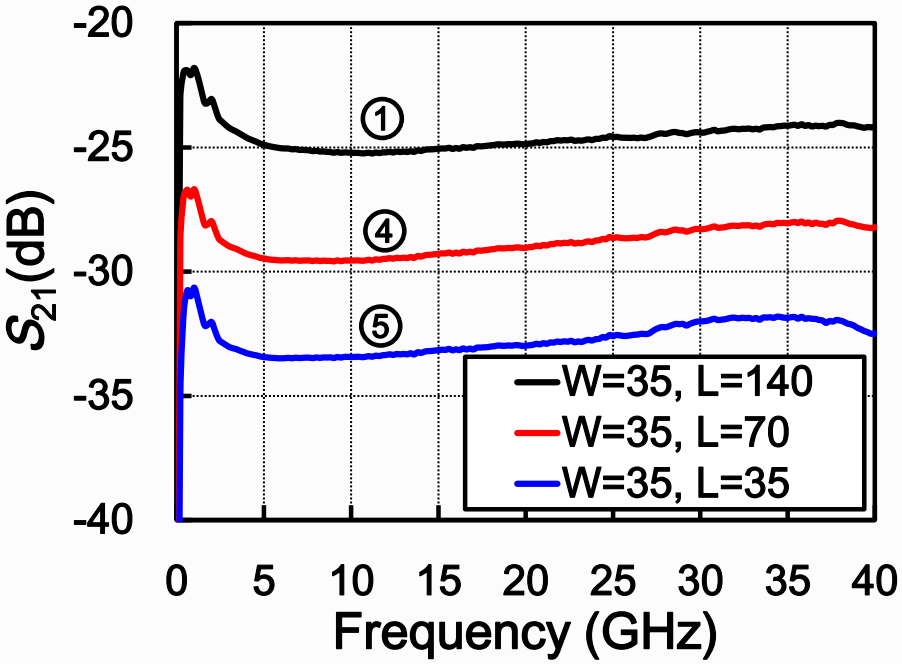
- Measured noise isolation with respect to tap distance
- Increasing *D* from 100μm to 150μm improves noise isolation 5dB, from 150μm to 200μm of 3dB at 10GHz
- Increasing *D* will increase chip area.

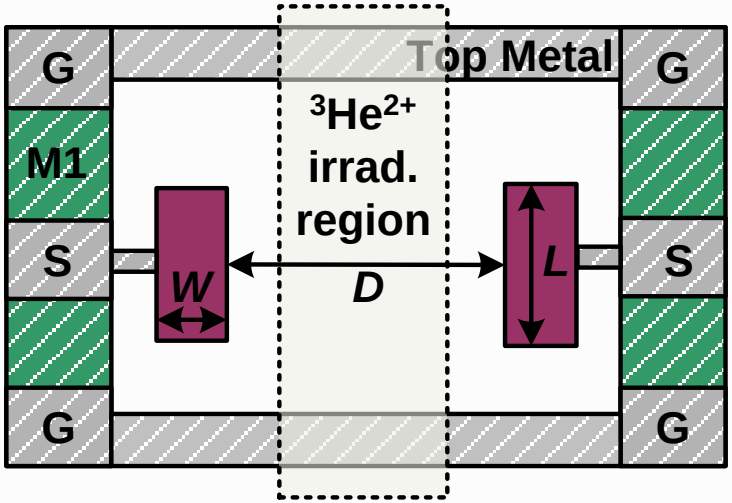




Measurement Results (2)

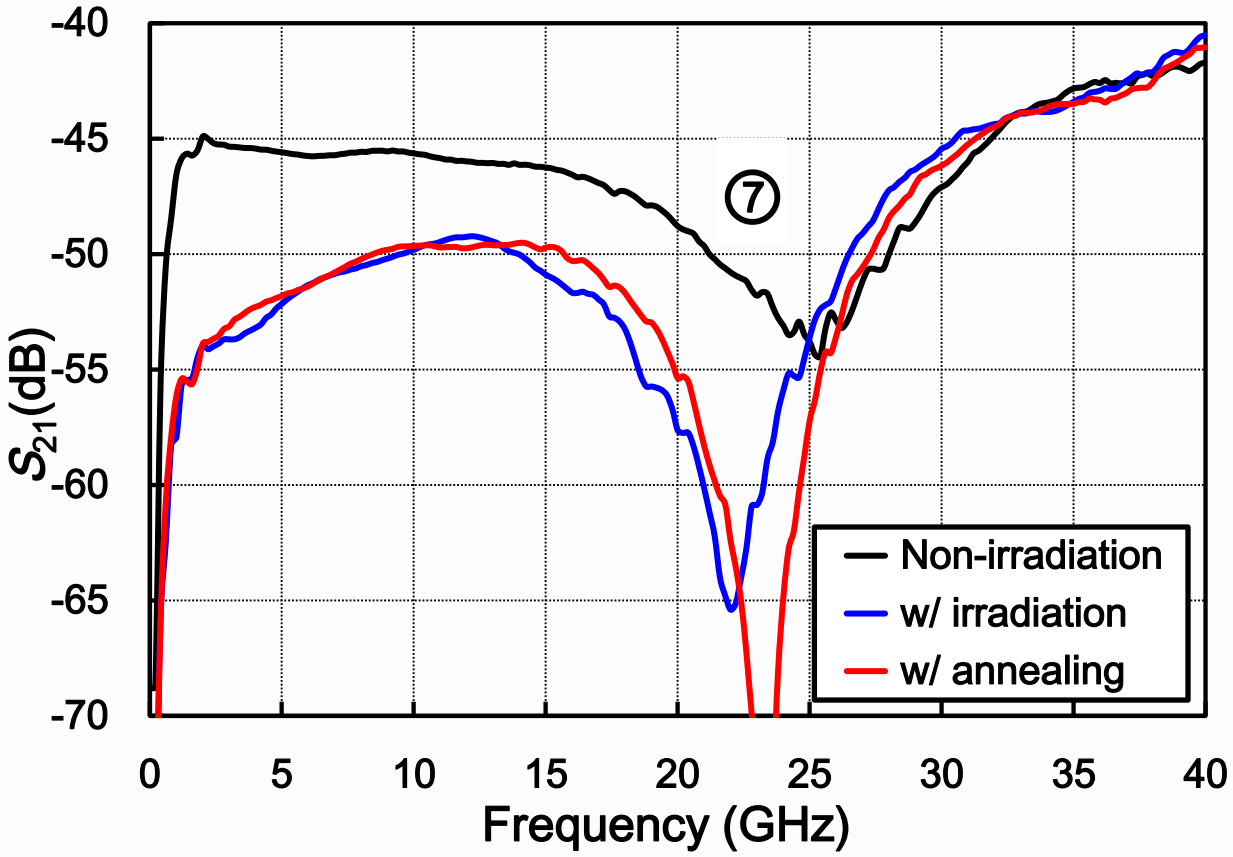
- Measured noise isolation with respect to tap size
- Large diffusion area causes more coupling.



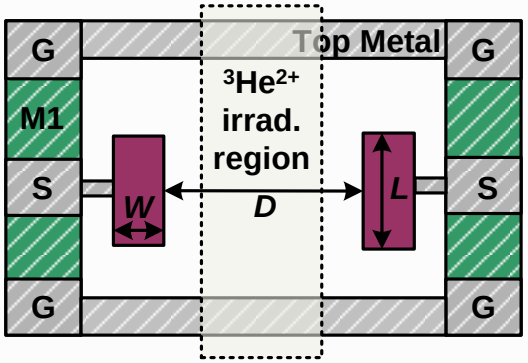


Measurement Results (3)

- **Isolation is maintained after annealing at 200ºC for 1 hour.**

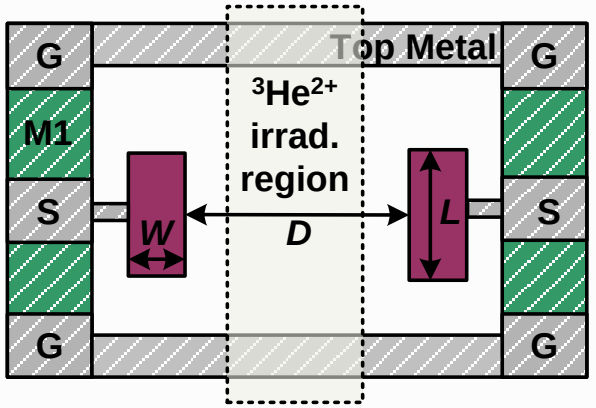


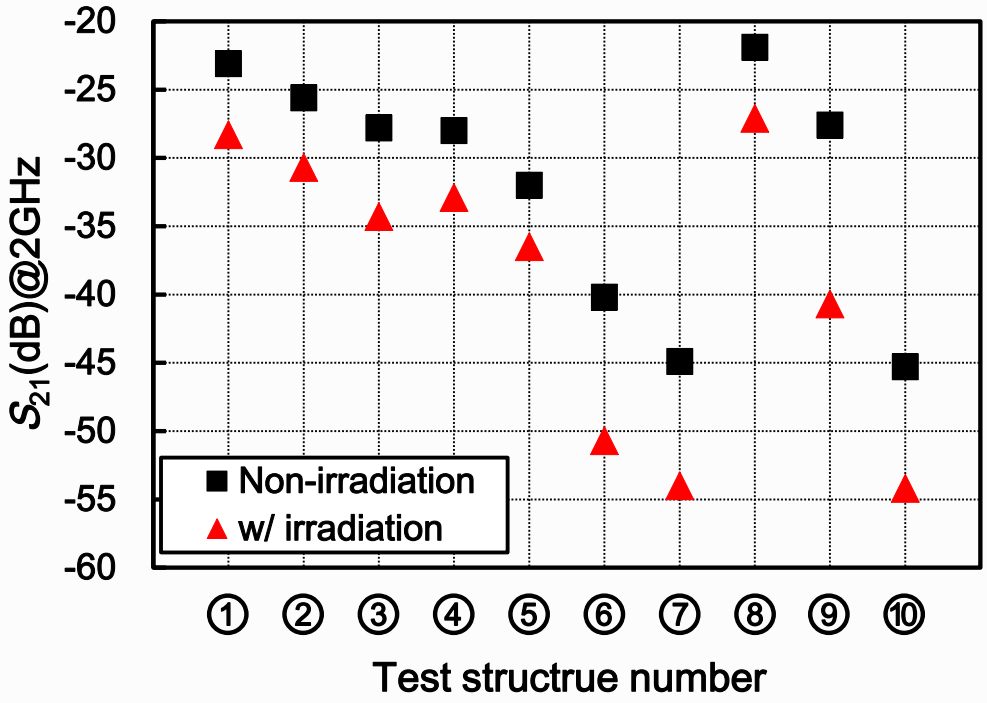
TEG	Guard Ring (GR)
⑦	P+ GR and DNW



Measurement Results (4)

- **Isolation is improved for all test patterns after helium-3 ion irradiation.**
- **A 10-dB improvement (90% noise reduction) is achieved for patters with GR.**





	Dist. (μm)
①	100
②	150
③	200

	Size (W*L) (μm^2)
①	35*140
④	35*70
⑤	35*35

	Guard Ring (GR)
①	None
⑥	P+ GR
⑦	P+ GR and DNW
⑧	None
⑨	N+ GR
⑩	N+ GR and DNW

Conclusions

- **Helium-3 bombardment is proposed to create a local semi-insulated substrate of high resistibility.**
- **Noise isolation is improved about 10dB at 2GHz after helium-3 ion irradiation.**
- **A 90% noise reduction has been achieved for test structures with guard rings.**
- **The noise isolation can be kept even after annealing at 200ºC for 1 hour.**

Acknowledgements

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Thank you for your attention