A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator aided DTC

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Contents

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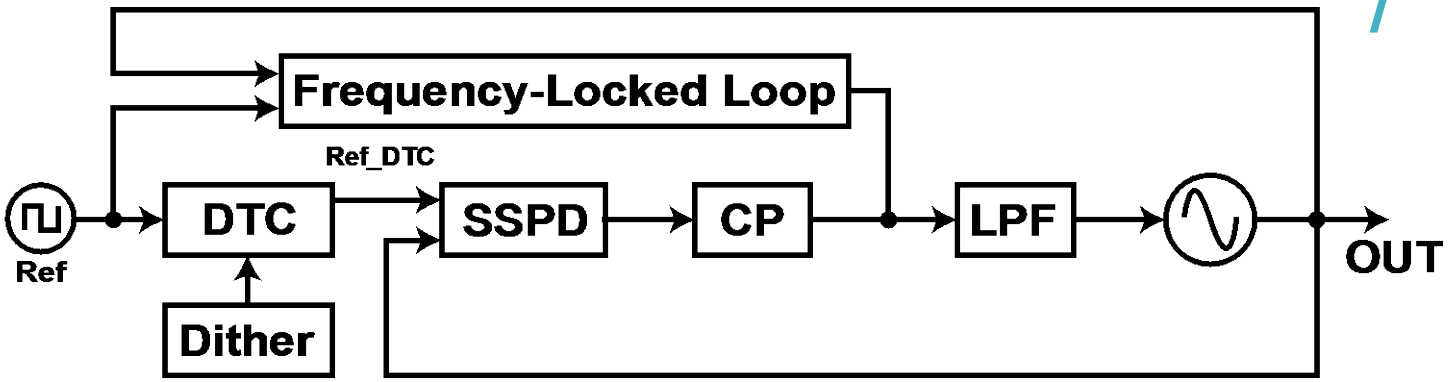
- Motivation
- Conventional Architectures
- Proposed Technique
- Noise Considerations
- Measurement
- Conclusion

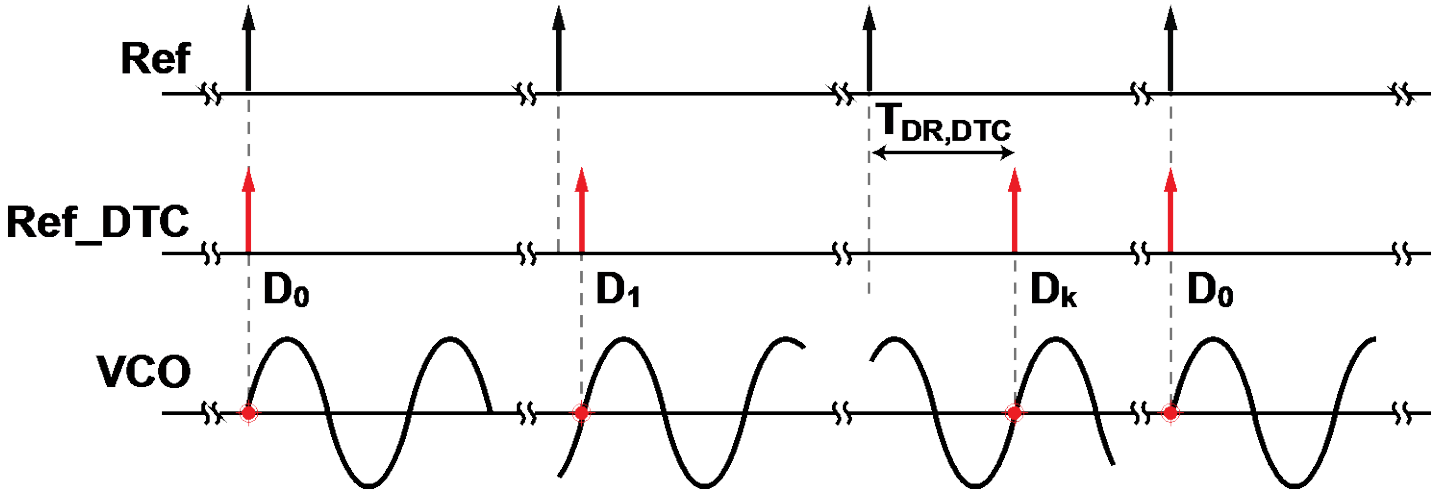
Motivation

- Wireless carrier generation requires fractional-*N* PLL.
- Fractional operation introduces additional noise.
- Conventional synthesizer architectures:
  - CP Based: Poor close-in phase noise.
  - TDC Based: Power-jitter trade-off.
  - Injection Locking: Large spurious.
  - Sub-sampling: Power-jitter tradeoff.

Aim: Low-power high-purity fractional-*N* PLL

Fractional-*N* SS-PLL: Prior Art



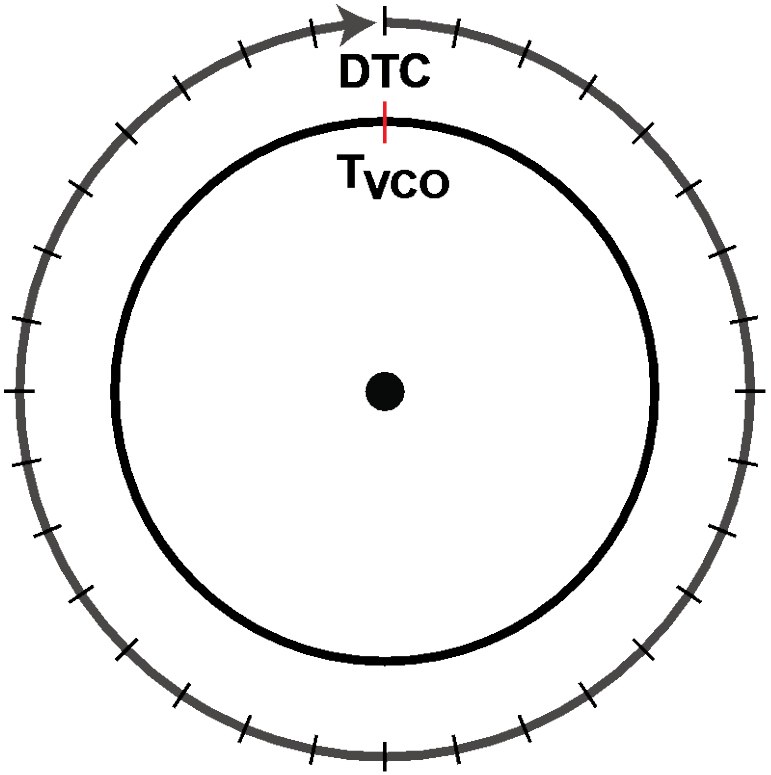


$f_{out} = (N+n) \times f_{ref}$; N- Integer part; n- fractional part

DTC in reference path enables fractional operation

*[G. Marucci, ISSCC 2014] [Po-Chun Huang, ISSCC 2014] [K. Raczkowski, RFIC 2014]

DTC Only Architecture: Challenges

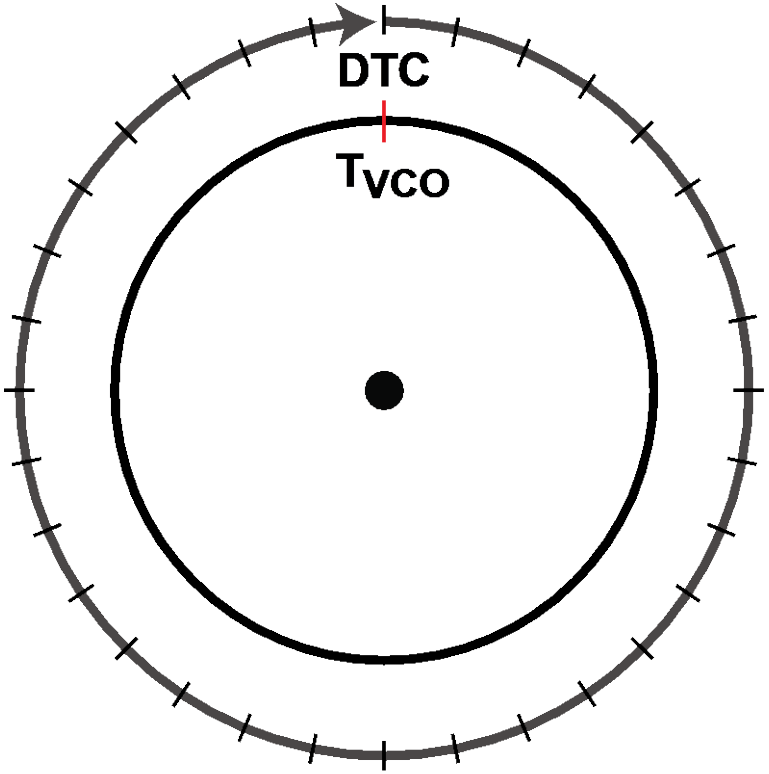


DTC Only Architecture

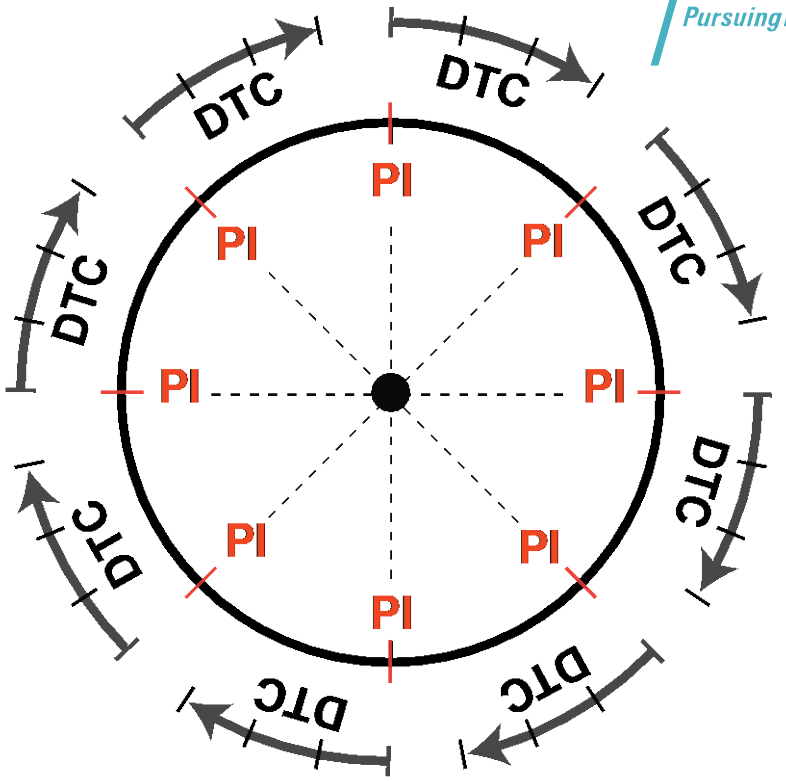
$$DR_{\mathrm{DTC}} \geq T_{\mathrm{VCO}}$$

DTC with large dynamic range is required

Proposed Technique



DTC Only Architecture



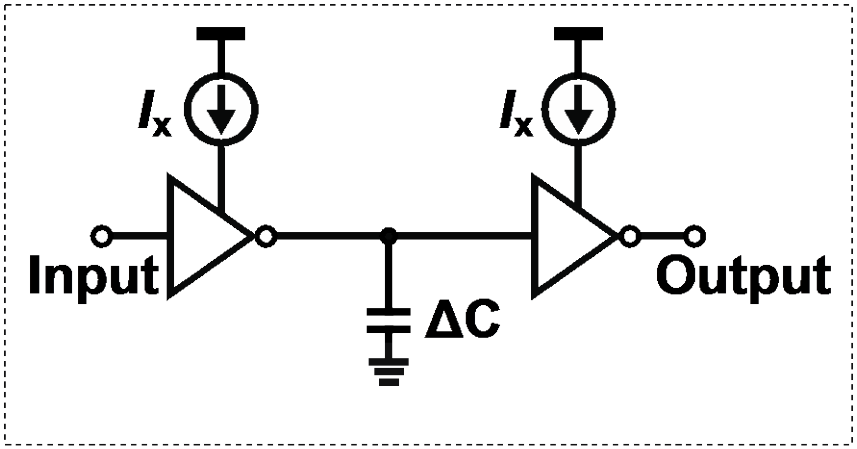
Phase Interpolator+DTC

$$DR_{\mathrm{DTC+PI}} = T_{\mathrm{VCO}}/4\left[\left(\sum_{i=0}^{n} 1/2^n\right) + 1/2^n\right]$$

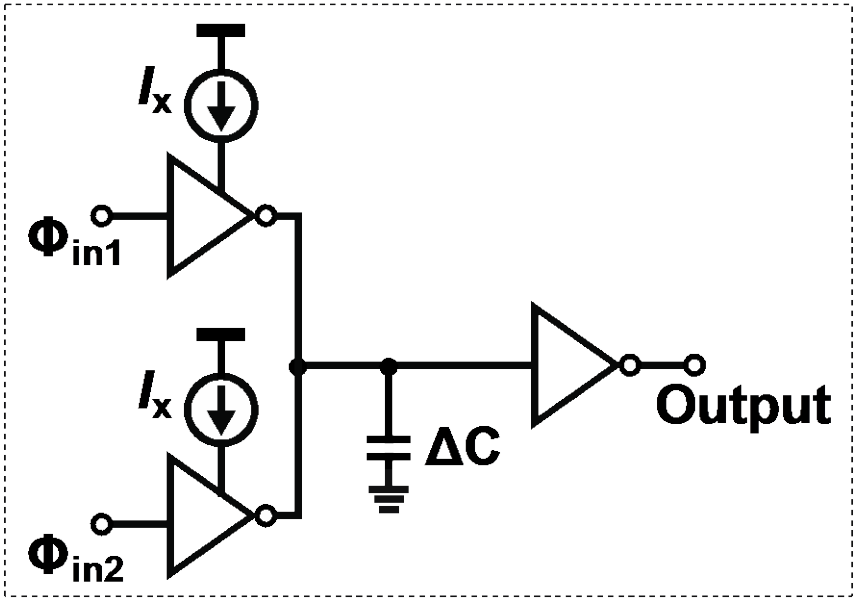
Dynamic range requirements are relaxed

Jitter Considerations

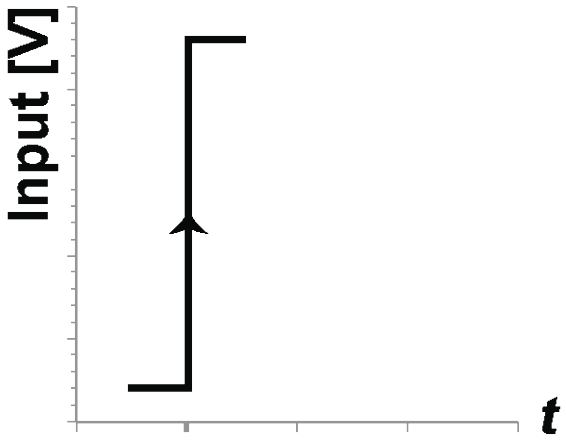
DTC

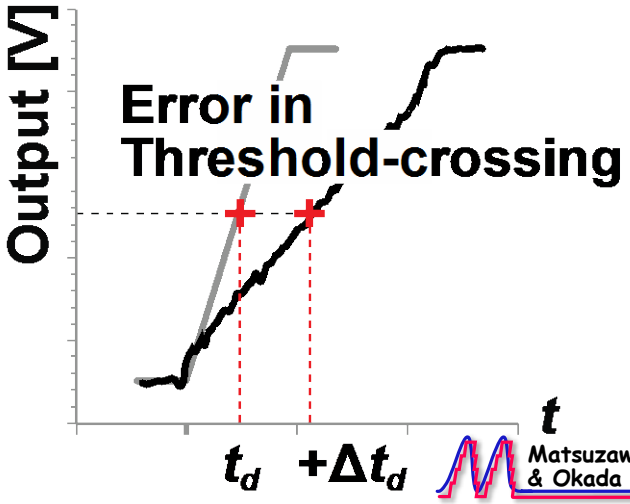


Phase-Interpolator



$$\sigma_{\tau_d}^2 = \frac{4kT\gamma\,\tau_d}{I_n(V_{DD} - V_{th})}$$



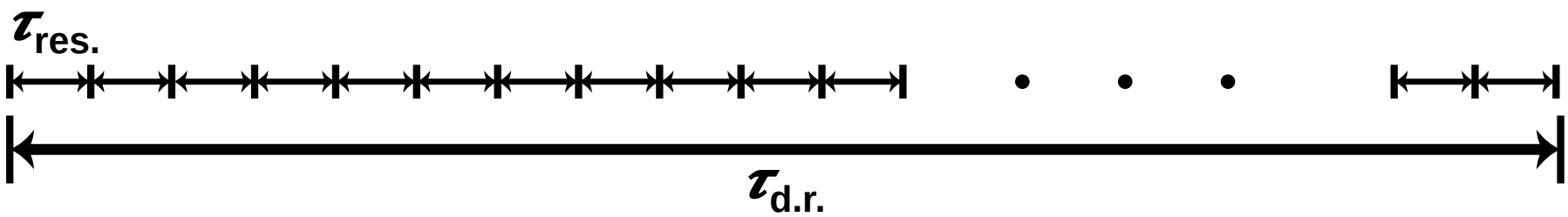


[A. Abidi, JSSCC 2006]

Intuitive Analysis: DTC Only

Large Dynamic Range [d.r.], Fine Resolution [res.]

$$\tau_{res} = \frac{\Delta C V_{\mathrm{DD}}}{2I} \qquad \sigma^2_{\tau_{\mathrm{res}}} = \frac{4\mathrm{kT}\gamma\,\tau_{\mathrm{res}}}{I(V_{\mathrm{DD}} - V_{\mathrm{th}})}$$

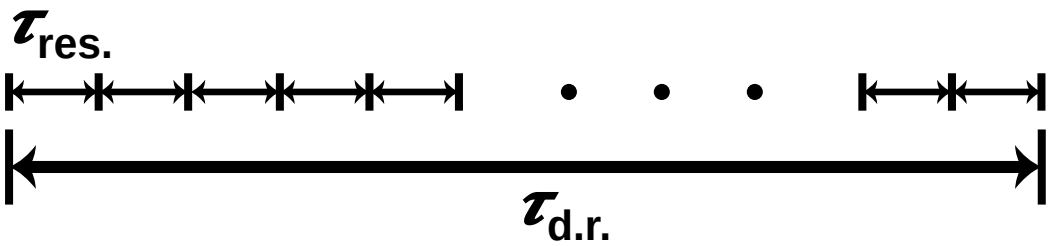


- ***Large d.r. and Fine res.***
  - **=> 'ΔC' must be large enough to assure PVT robustness.**
  - **=> '*I*' needs to be kept high for low jitter.**
- **Power-Jitter-Resolution trade-off.**

Intuitive Analysis: PI assisted DTC

Small Dynamic Range [d.r.], Fine Resolution [res.]

$$\tau_{res} = \frac{\Delta C V_{DD}}{2I} \qquad \sigma^2_{\tau_{dr}} = \frac{4kT\gamma\,\tau_{dr}}{I(V_{DD} - V_{th})}$$



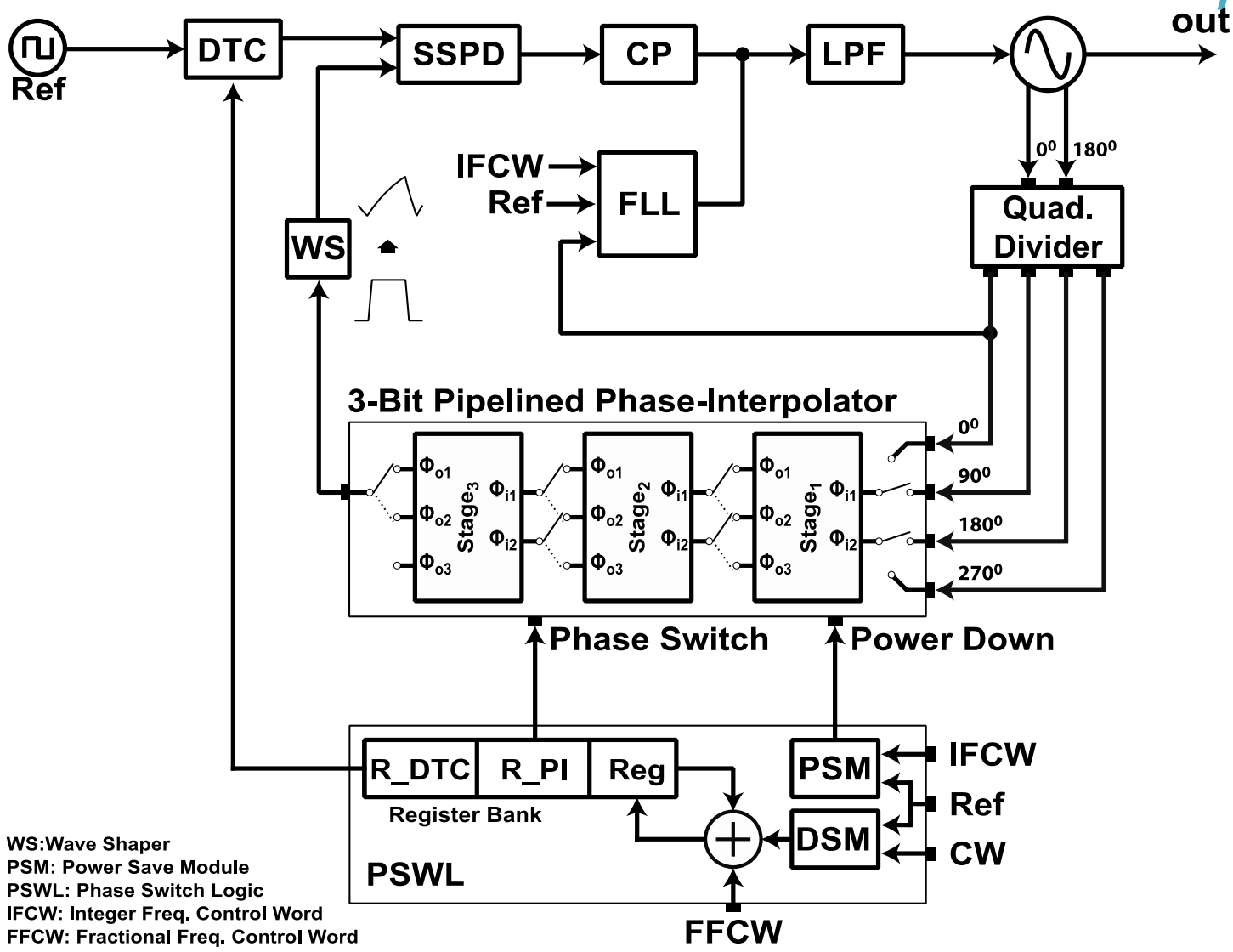
- ***Small d.r. and Fine res.***

  => Small '$\tau_{d.r.}$'

  => *'I'* can be kept acceptably high for lower jitter.

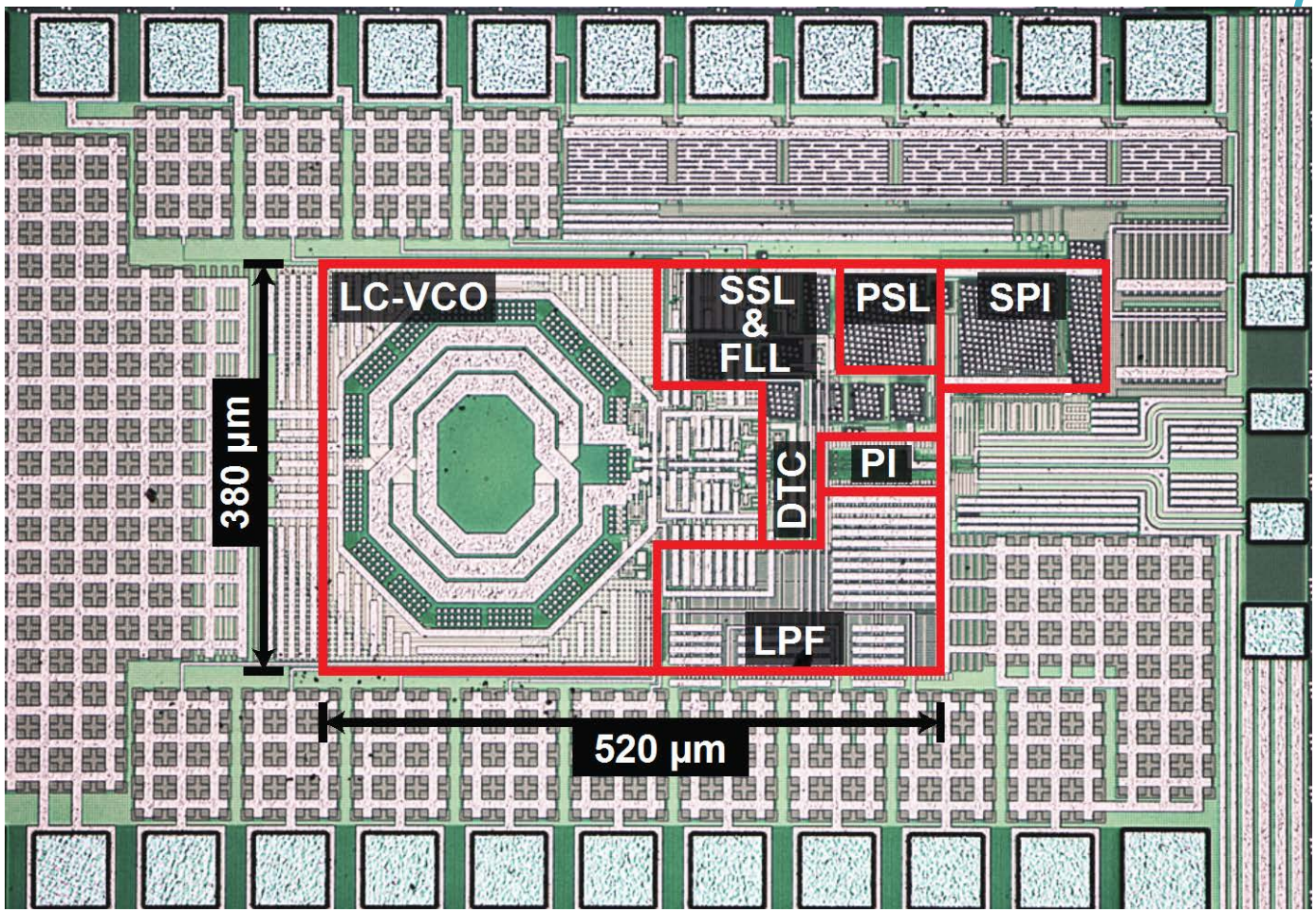
- **Proposed architecture reduces dynamic range and hence jitter.**

Proposed Fractional-*N* SSPLL



WS:Wave Shaper
PSM: Power Save Module
PSWL: Phase Switch Logic
IFCW: Integer Freq. Control Word
FFCW: Fractional Freq. Control Word

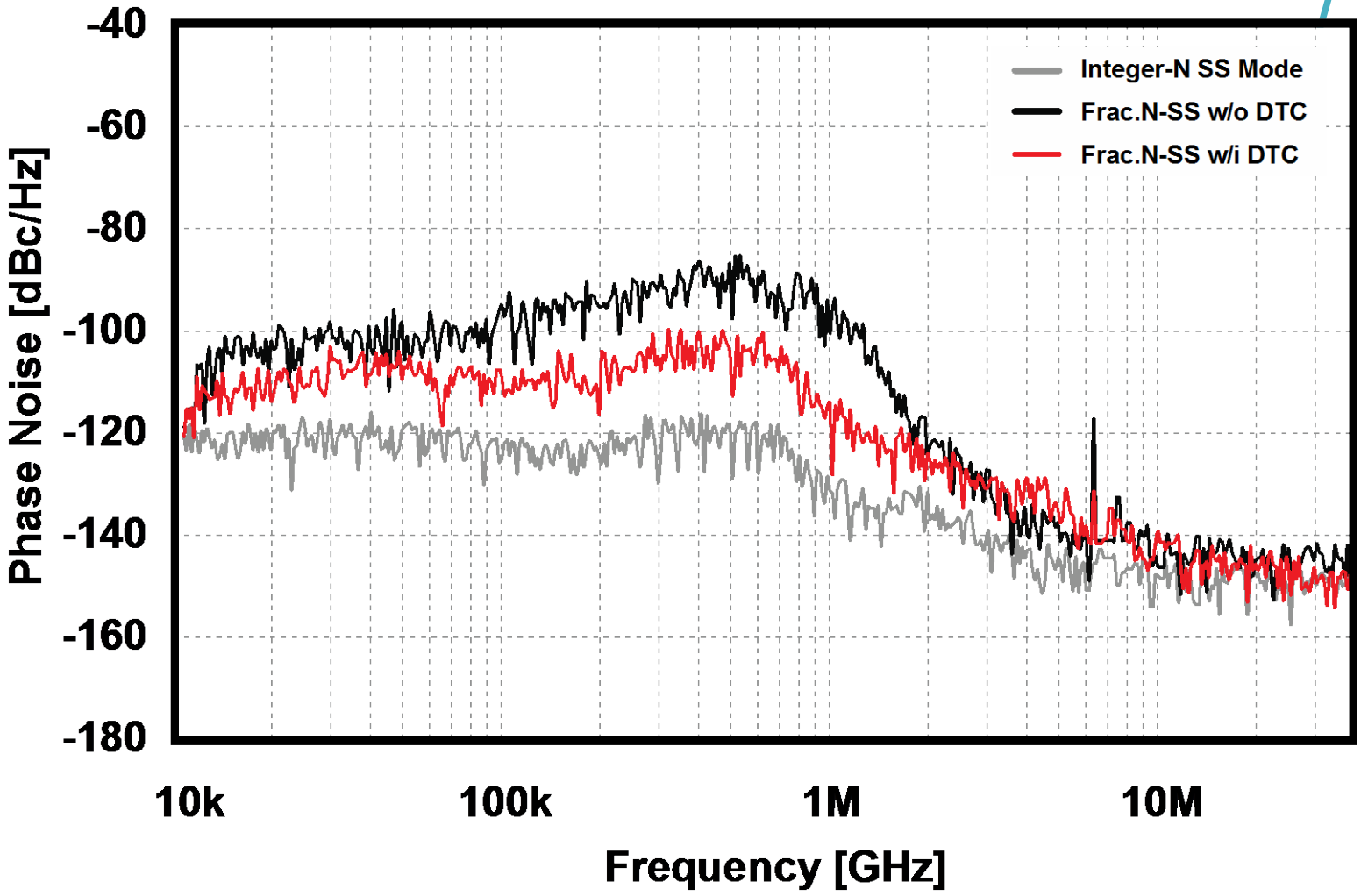
Chip Micrograph



[PSL: Phase Switch Logic] [SSL: Sub-sampling Loop] [PI: Phase Interpolator]

Stacked capacitors are used for area reduction

Measurement Results



Division ratio for fractional-*N*: 50.163

Comparison with SOA

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	This work	[1]	[2]	[3]
Architecture	SSPLL	SSPLL	MDLL	TDC
Freq. [GHz]	4.1-5.1	2.2-2.4	1.6-1.9	2.412-2.484 4.915-5.825
Power [mW]	3.8	17.3	3	9.5
Area [mm^2]	0.2	0.75	0.4	0.3
Phase Noise (in-band)	-112 @400kHz	-112 @50kHz	-112 @100kHz	-106 @100kHz
Integrated Jitter	254.4fs	266fs	1.4ps	173fs
FoM [dB]	-246.1	-239.1	-233.76	-245.5
CMOS Tech.	65nm	180nm	130nm	28nm FDSOI

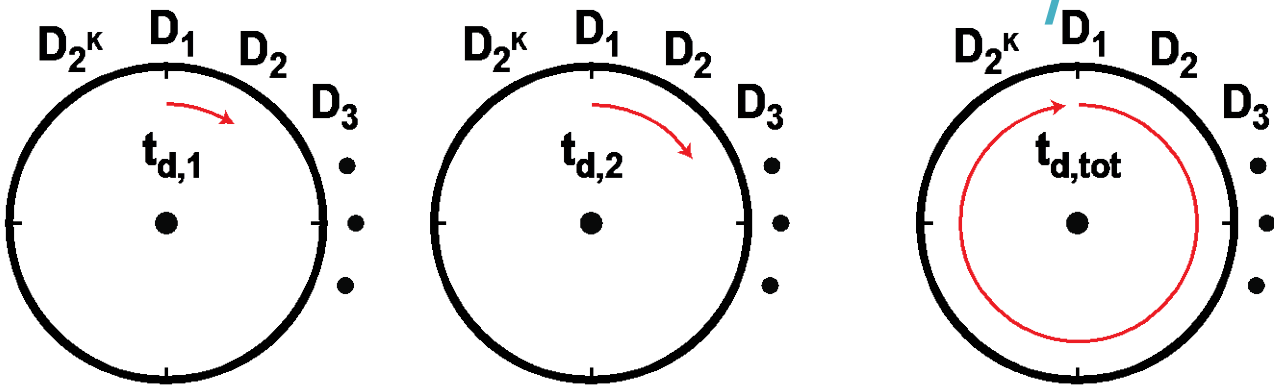
•[1] Po-Chun Huang, ISSCC 2014 [2] G. Marucci, ISSCC 2014 [3] X. Gao, ISSCC 2015

Conclusion

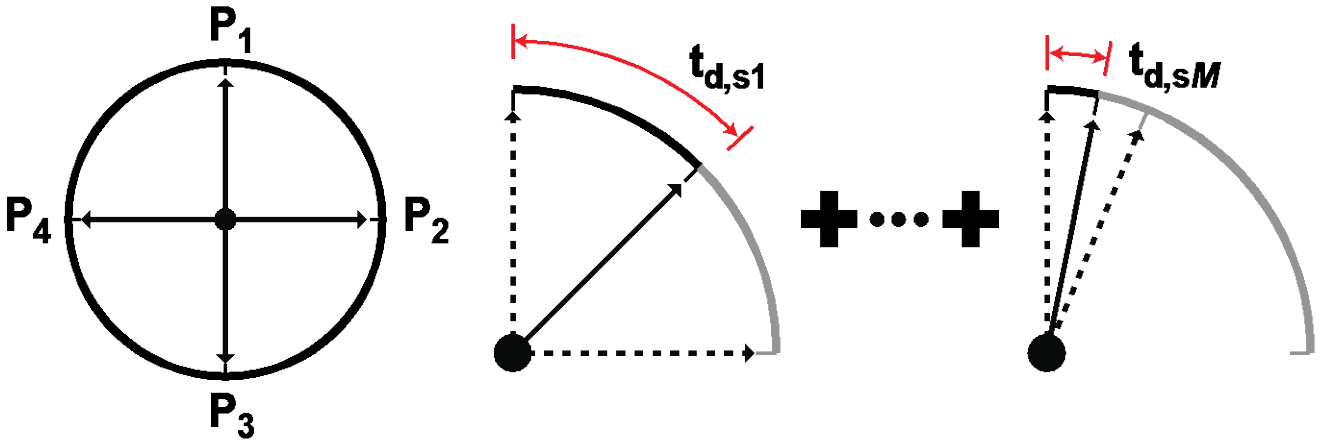
- **A fractional-*N* SSPLL architecture is presented.**
- **The proposed architecture uses a combination of DTC and phase-interpolator**
  - Reduces intrinsic jitter from the multi-phase generator.
  - Power-jitter-resolution tradeoff is mitigated.

Jitter Considerations

Digital-to-Time Converter



Phase Interpolator

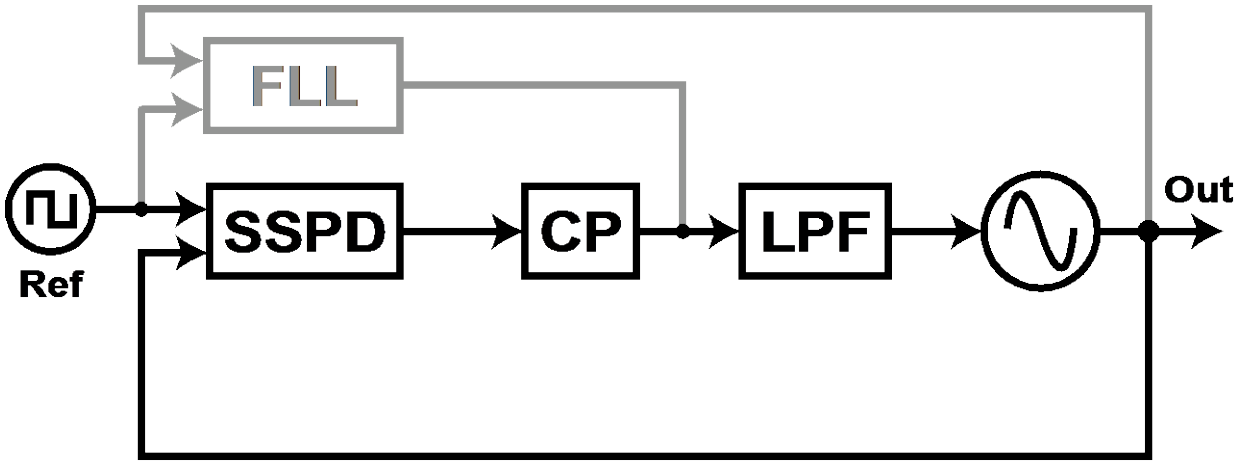


$$\sigma_{\tau_d}^2 = \frac{4kT\gamma\,\tau_d}{I(V_{DD} - V_{th})}$$

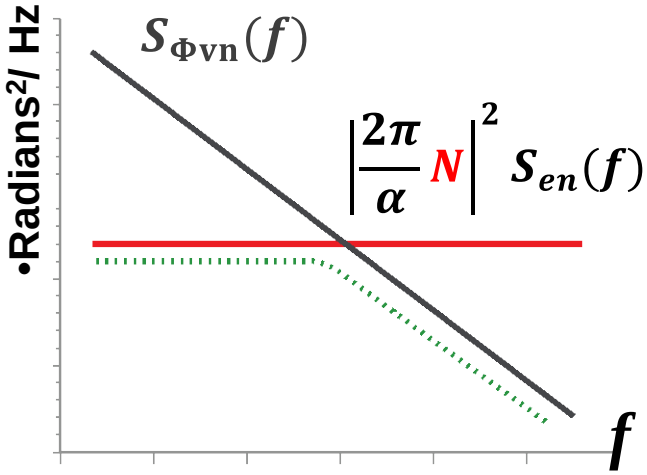
- **Worst case jitter is much smaller in phase-interpolator.**

[A. Abidi, JSSCC 2006]

Sub-Sampling PLL: An Overview



Block Diagram



PLL Noise Shaping

- Lower N implies lower close-in noise.
  - Operation is limited to Integer-*N*.

[X. Gao, ISSCC 2009]