A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator aided DTC

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1 Introduction

Fractional-N PLL is an essential part of modern wireless communication systems. The ever-increasing demand for higher data transfer rates while operating in heavily crowded frequency bands demands top-notch performance from the frequency synthesizers. In order to satisfy the tough requirements put forth by modern communication standards, researchers around the world have examined many innovative technologies in the recent years [4] [5] [6].

2 Proposed Architecture

This work focuses on improving the in-band noise for improving the overall jitter performance of the system. A pipelined phase interpolator is used along with a sub-sampling technique [1] [2] for improving the jitter performance while working with very low power consumption (Fig.1). The multiple phases produced by the phase interpolator and DTC facilitates the fractional operation. The linearity and resolution of DTC influences the spur and in-band phase noise of a fractional-N PLL [3]. Conventional DTCs exhibits highly non-linear behavior and they often requires complex multi-point calibration when used for fractional operation [7]. The introduction of the phase interpolator relaxes the design complexity of the DTC and improves noise performance in comparison with the prior works [4] [5] .

3 Measurement Results

The proposed fractional-N sub-sampling PLL was fabricated in a standard 65nm CMOS process. The core occupies a chip area of 0.2mm^2. While working at a frequency of 4.4716GHz from a reference clock of 40MHz, the system generates an integrated jitter of 273fs with a power consumption of 3.3mW from a 1.1V supply. The comparison of the proposed fractional-N PLL with other state-of-the-art PLLs given in Table1 demonstrates the effectiveness of the proposed topology.

4 Conclusion

This paper proposes a fractional-N PLL using a pipelined phase-interpolator. The pipelined phase-interpolator with low intrinsic jitter and power when combined with the sub-sampling architecture produces a fractional-N PLL with low phase noise, small chip area and low-power.

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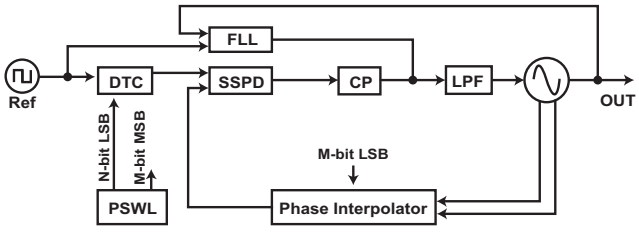

Figure 1: Conceptual block diagram and working principle of proposed fractional-N PLL.

Table 1: Comparison with state-of-the-art fractional-N PLLs.

	[4]	[5]	[6]	This Work
Type	MDLL	SS	TDC	SS
RMS Jitter (fs)	1400	266	173	272.9
Power (mW)	3	17.3	9.5	3.3
Area (mm^2)	0.4	0.75	0.3	0.2
FoM (dB)	-232	-239.1	-245.5	-246.1

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