A 9.35-ENOB, 14.8 fJ/conv.-step Fully-Passive Noise-Shaping SAR ADC

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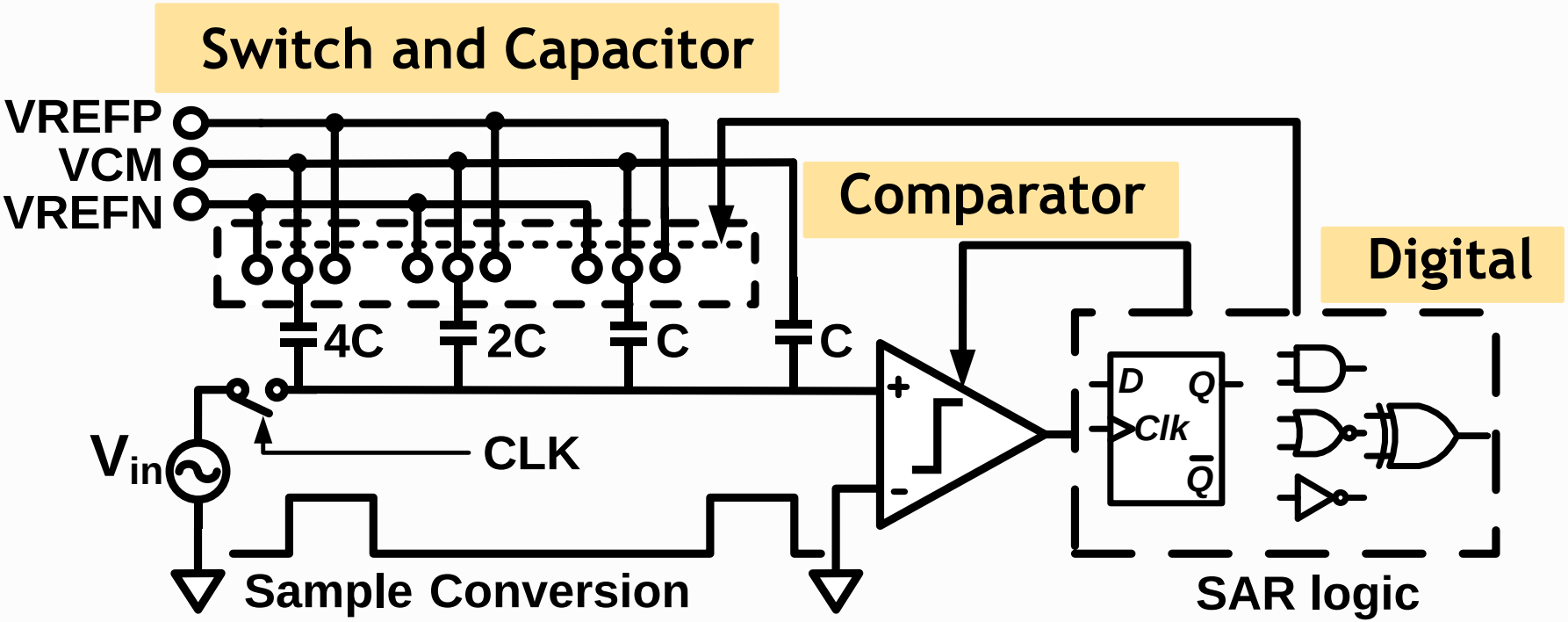
Outline

- Background and motivation
- Conventional Noise shaping technique
- Proposed fully passive noise shaping SAR ADC
- Experimental results
- Conclusion

Background and Motivation

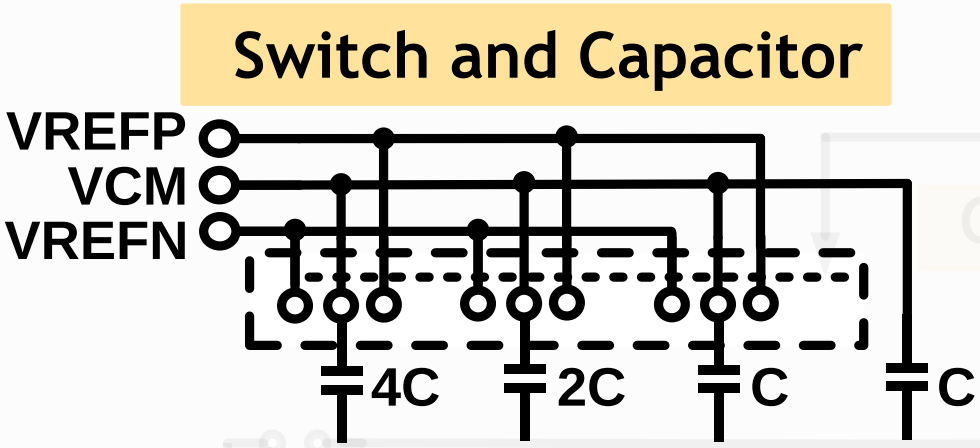
SAR ADC architecture:



- SAR ADC mainly consists of digital circuits
- It can benefit from the technology scaling (like speed)
- Analog components affect the performance

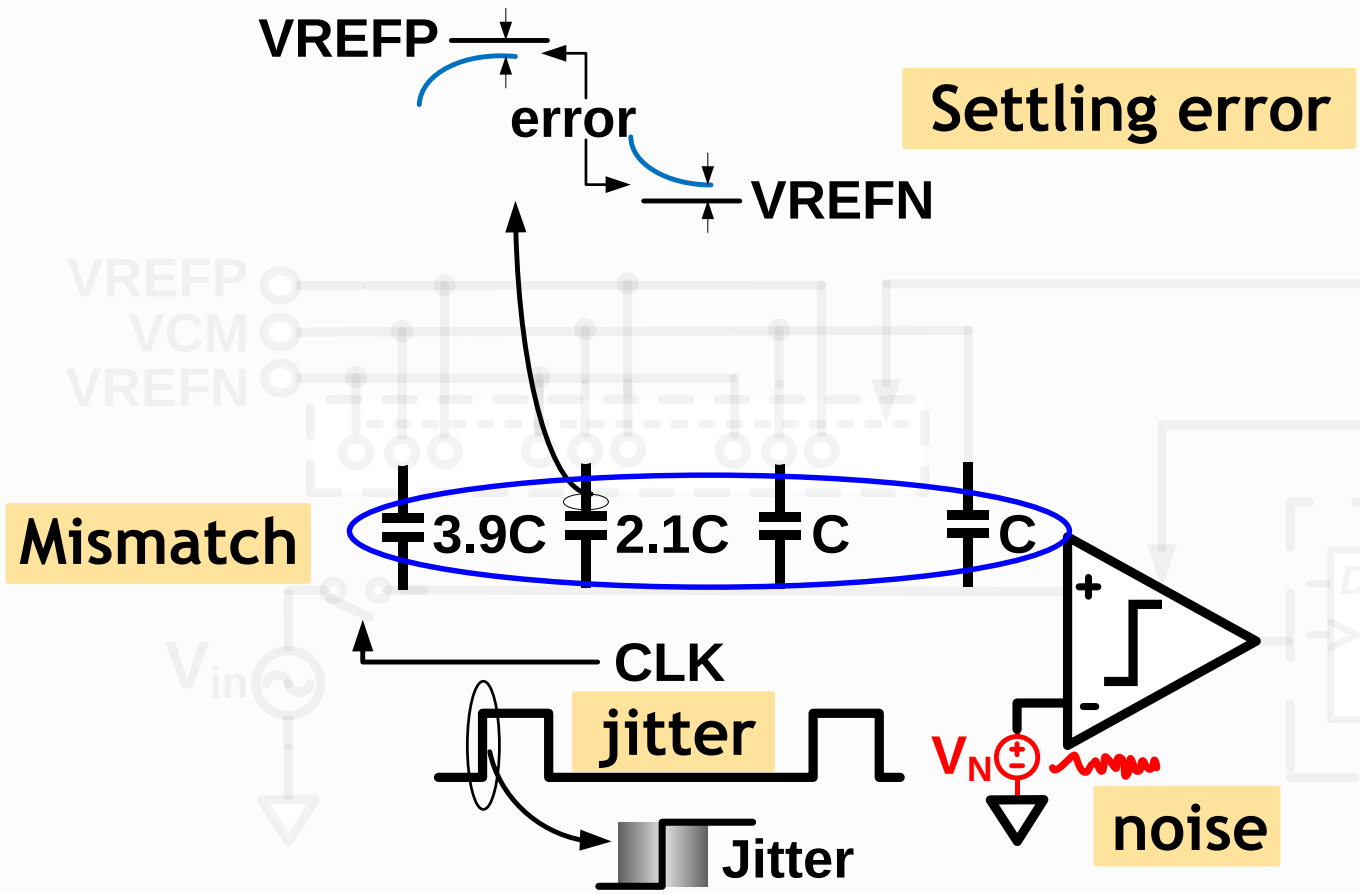
Switch and Capacitor in SAR ADC

Capacitor array affects SAR ADC performance



- Higher resolution → Larger cap → Larger settling time
- Larger cap → Larger chip size → Slower speed

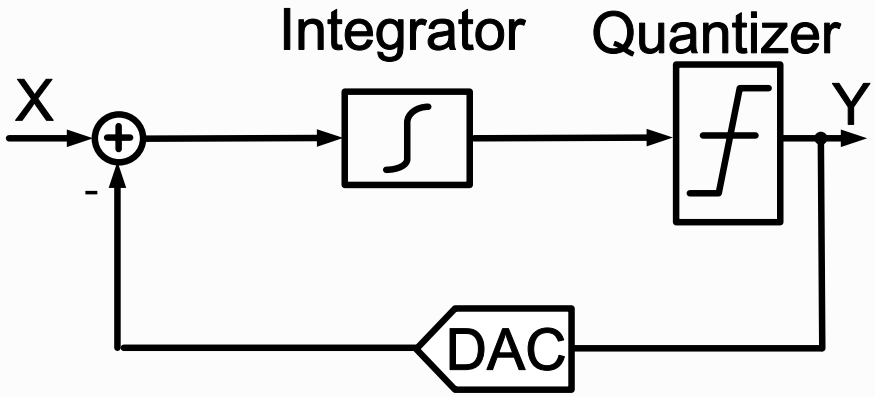
Non-ideal effects

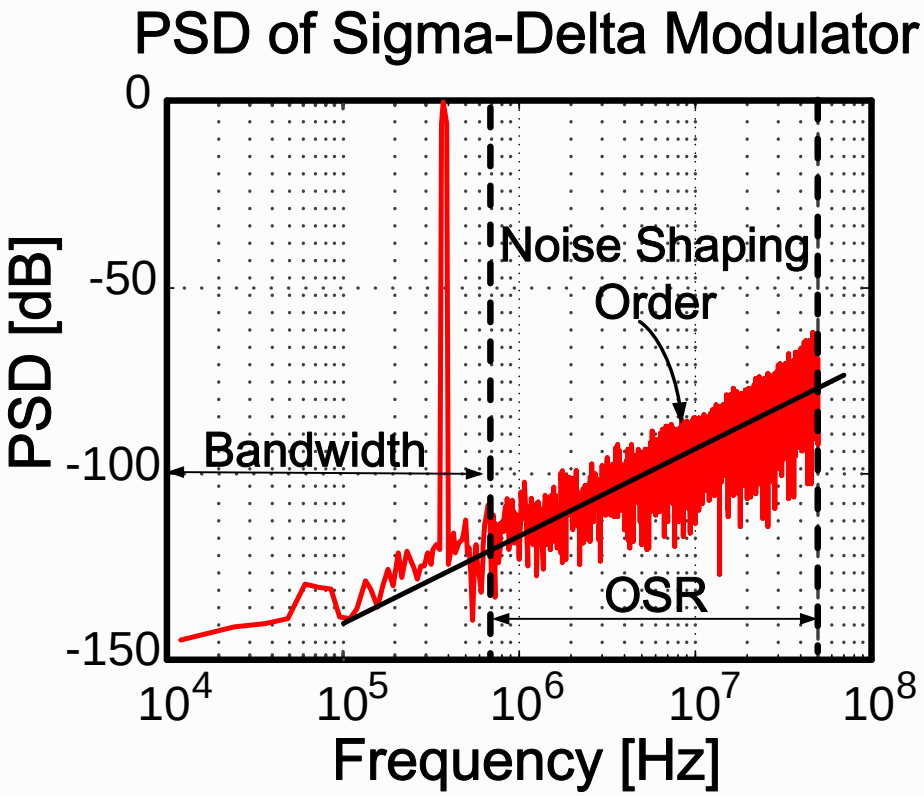


- Non-ideal effects further degrade performance
- How to improve the resolution?

Noise shaping technique

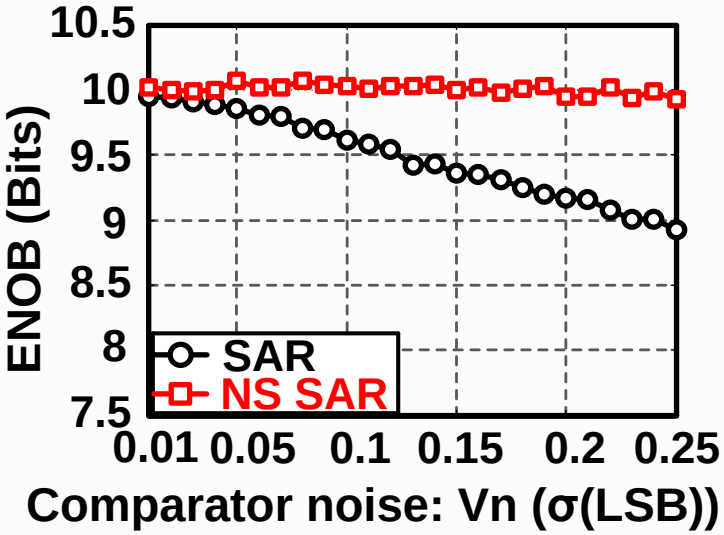
Move noise out of band of interest

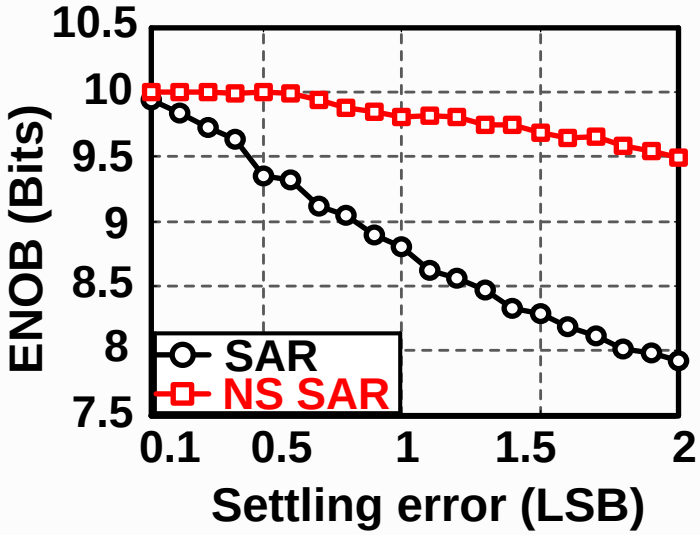


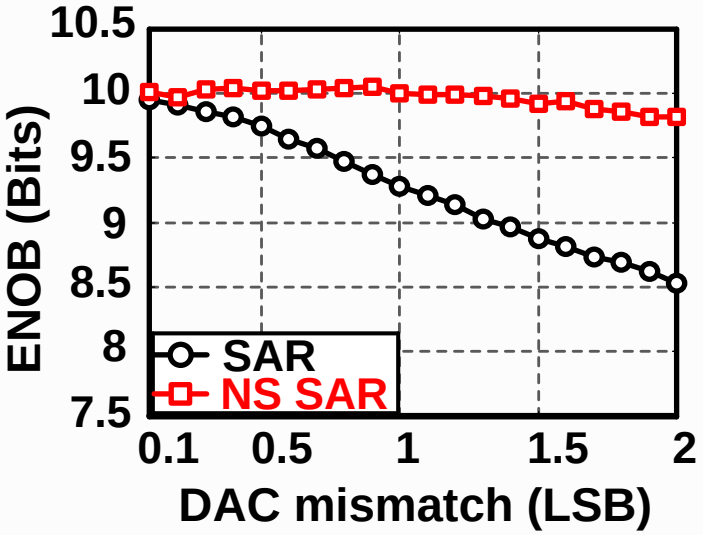


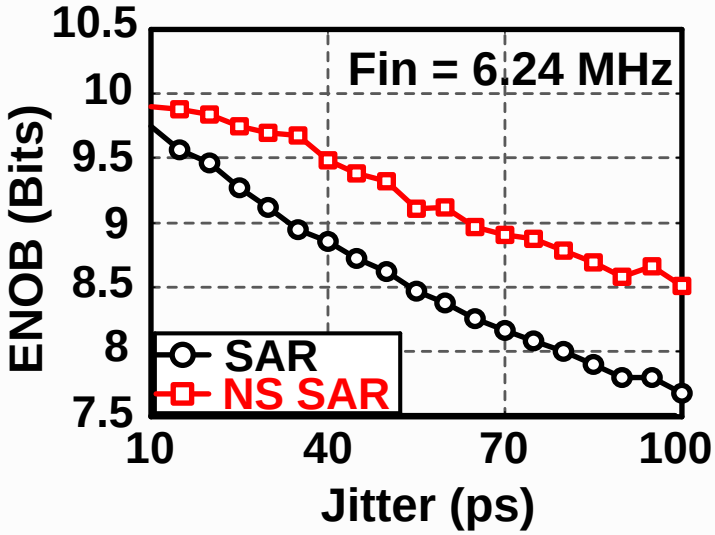
- Sacrifice speed for resolution
- Noise shaping is based on integrator, usually opamp

Simulation results of non-ideal effects









- Noise shaping reduces non-ideal effects

Noise shaping effect on capacitance

- Traditional SAR ADC

Thermal noise = kT/C

- Noise shaping SAR ADC

Thermal noise = $(1-Z^{-1})$ kT/C/OSR

Same SNR, smaller capacitor for noise shaping SAR ADC

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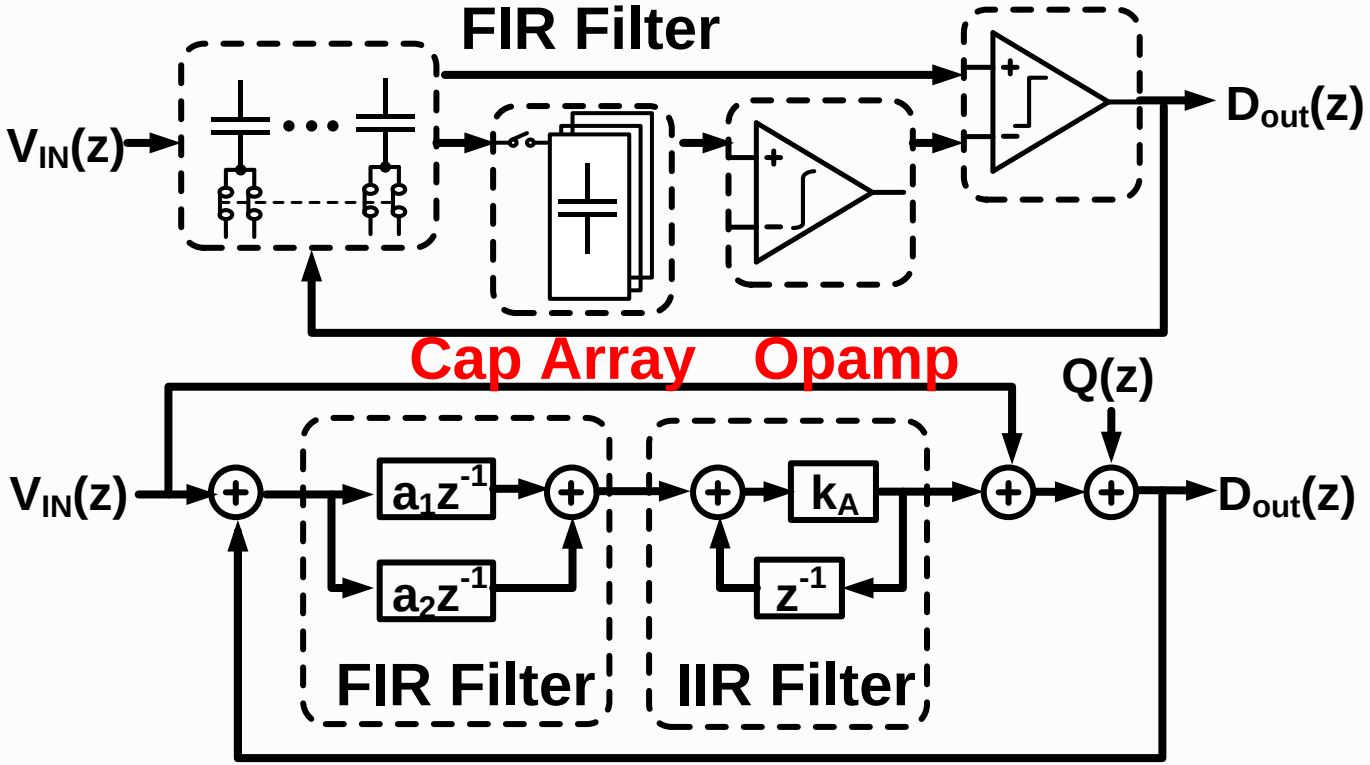
Conventional noise shaping technique



☹ FIR filter introduces extra noise and extra area;

☹ Opamp : extra power and flicker noise

☹ Tech. scaling, difficult to design high performance Opamp

[1] J. Fredenburg, et al., JSSC 2012

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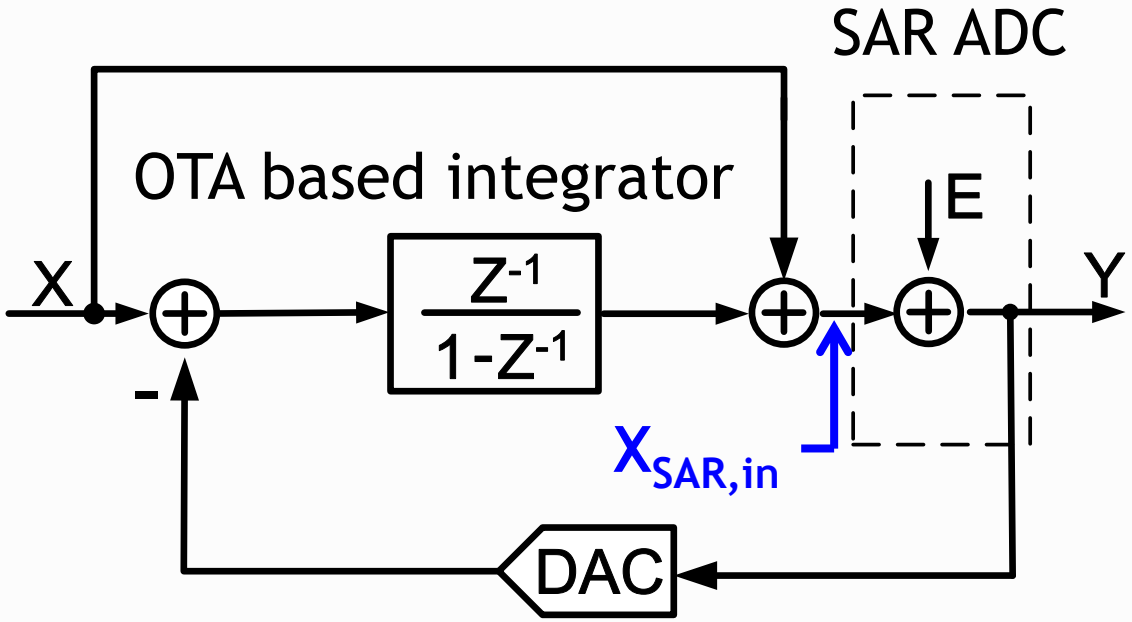
Traditional architecture

Traditional 1st-order noise shaping architecture



E: quantization noise

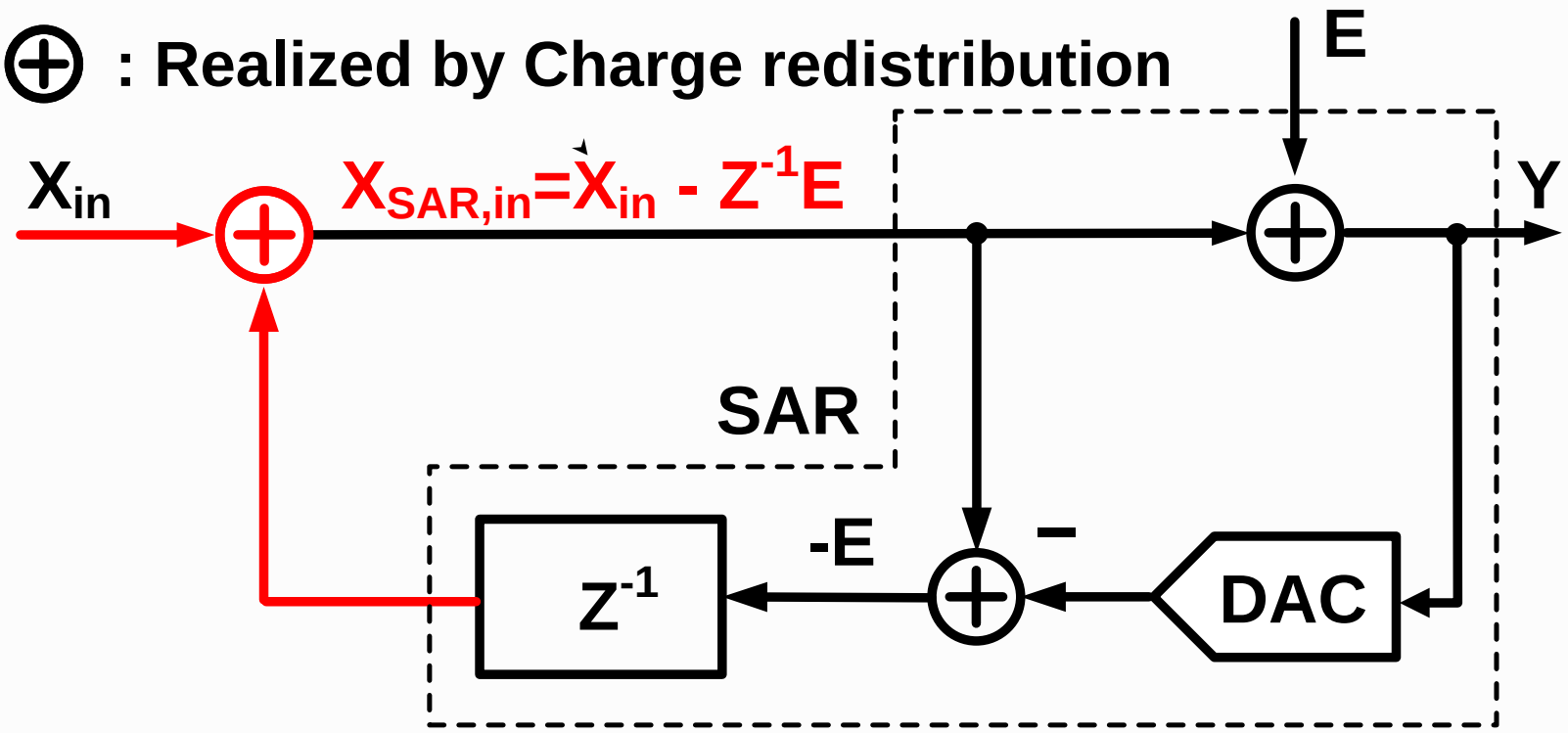
$Y=X+(1-Z^{-1})E$

Previous residue

$Y=(X-Z^{-1}E)+E \longleftrightarrow Y(N)=X(N)+X_{SAR,in}(N-1)-Y(N-1)+E(N)$

Proposed FPNS-SAR ADC architecture

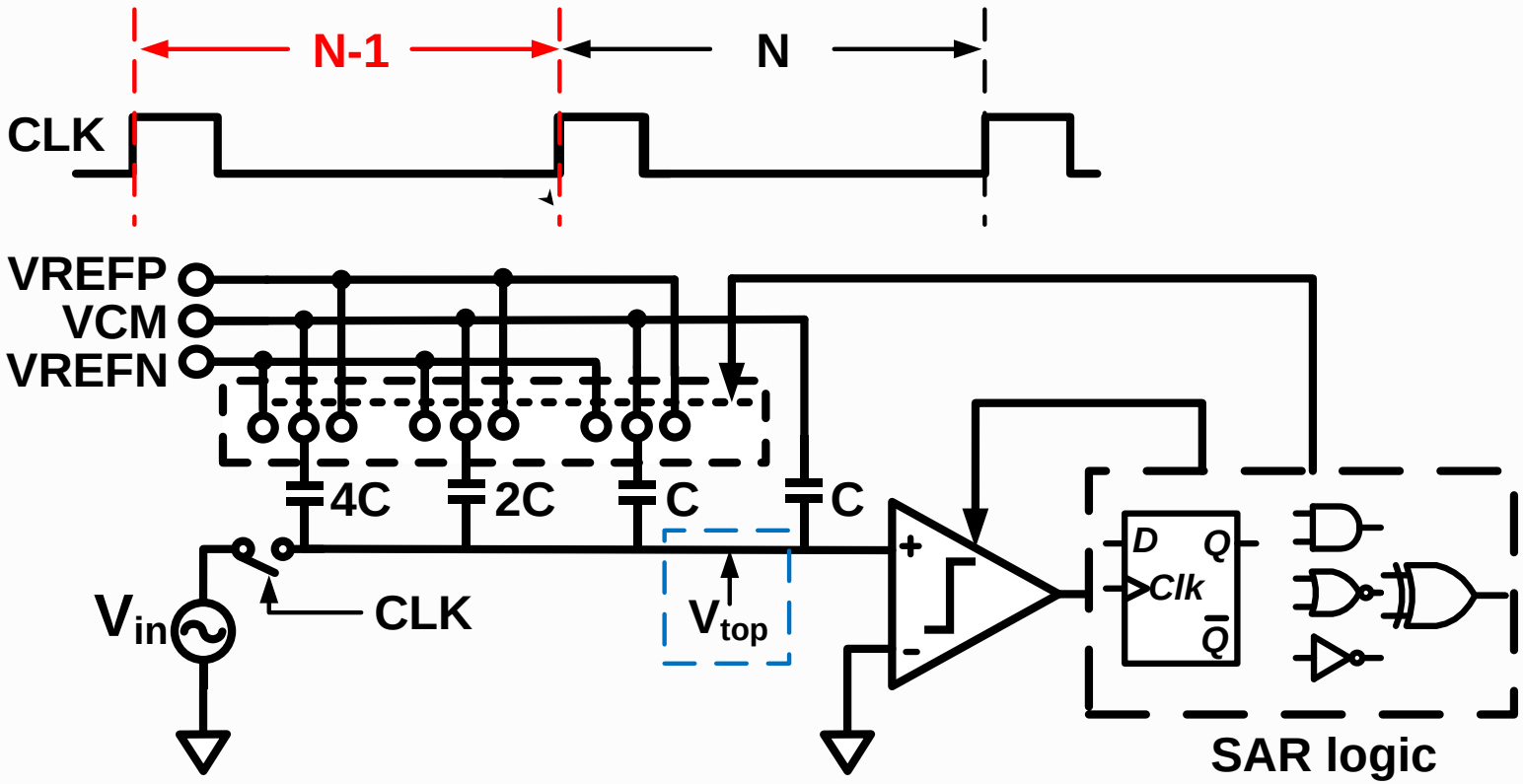
Proposed noise shaping architecture (*FPNS-SAR*)



Step 1: Get previous residue on top-plate of C-DAC;
Step 2: Feed it back to input.

Residue in SAR ADC

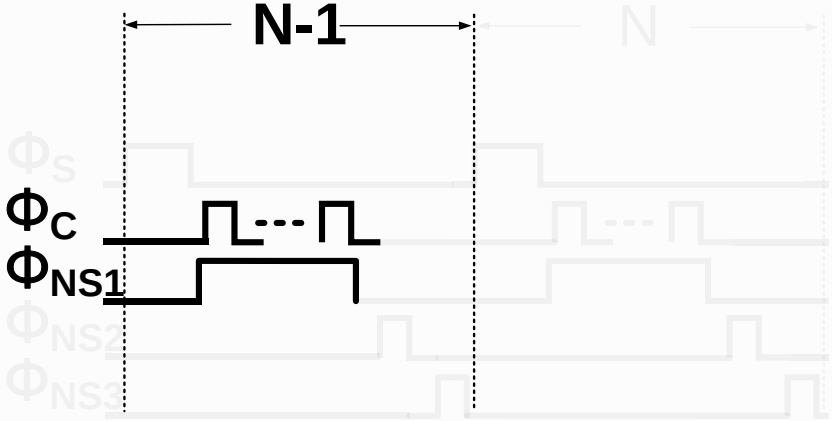
Residue on the top-plate of SAR ADC



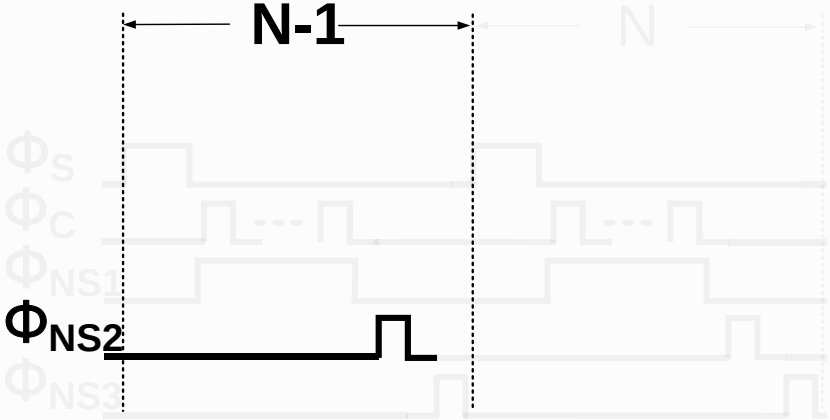
After conversion @ N-1, residue $V_{top}(N-1)=X_{SAR,in}(N-1)-Y(N-1)$

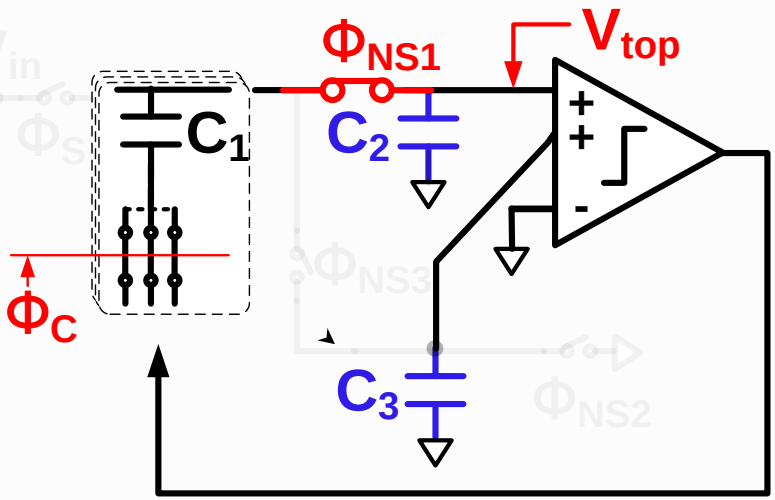
FPNS-SAR ADC implementation

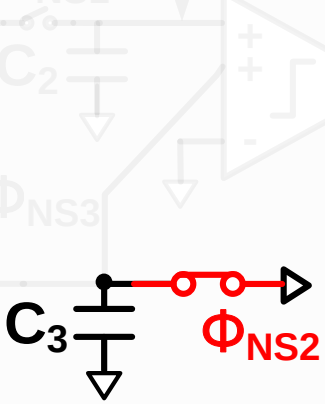
1. Conversion @ N-1



2. Clear Charge@ Φ_{NS2}





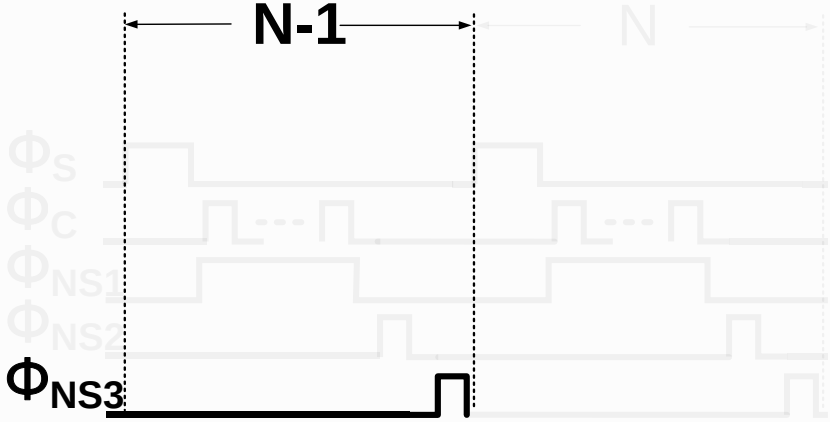


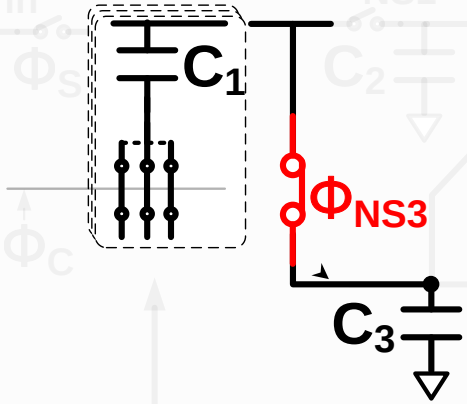
After conversion, V_{top}=-E(n-1)/2;

Clear Charge of C_3, Q_{C3}=0;

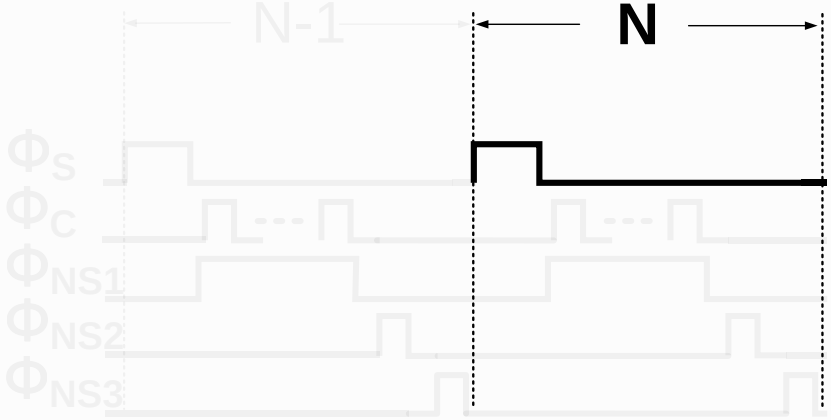
FPNS-SAR ADC implementation

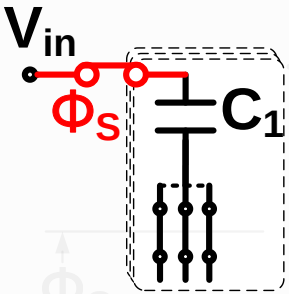
3. Charge share @ Φ_{NS3}





4. Sample @ N

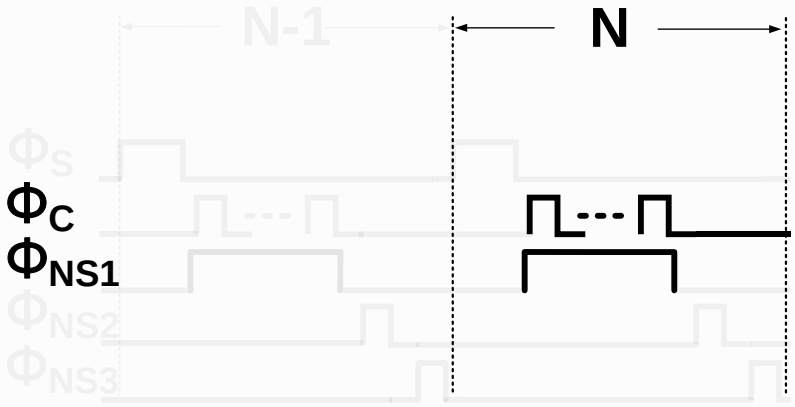




Get half top voltage, $V_{C3}= V_{top}$ (n-1)/2; Sampling input, V_{in}(n);

FPNS-SAR ADC implementation

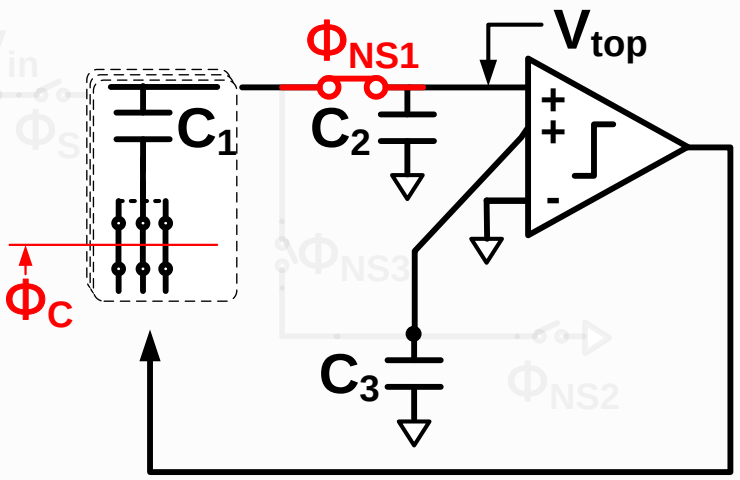
5. Conversion@ N



With the help of C_2 and C_3:

$$V_{DAC}(n) = V_{in}(n)-E(n-1)+E(n)$$

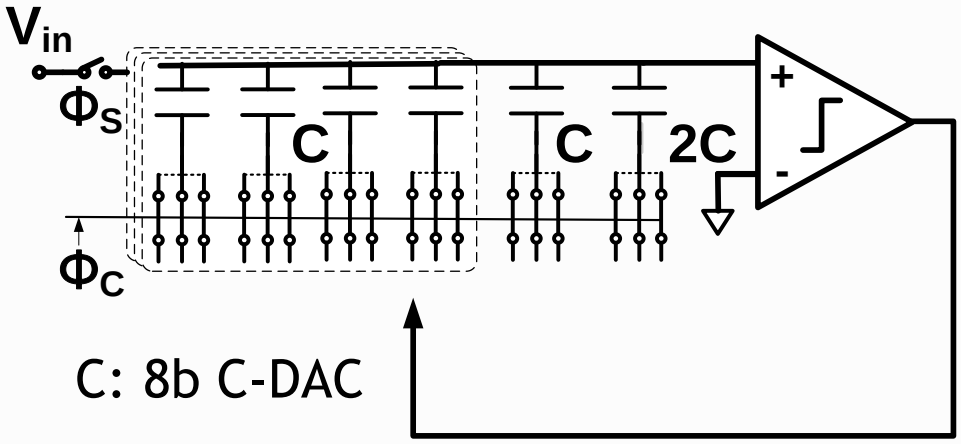
$$V_{DAC}(Z) = V_{in}(Z)+(1-Z^{-1})E(Z)$$



Realize 1st-order NS

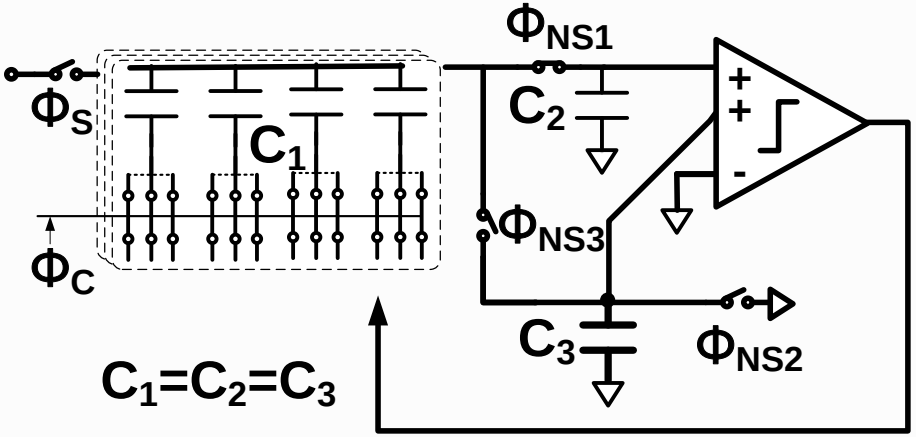
Capacitance comparison

Traditional 10b SAR-ADC



Total: 4 X C

Proposed 10b noise shaping architecture (*FPNS-SAR*)

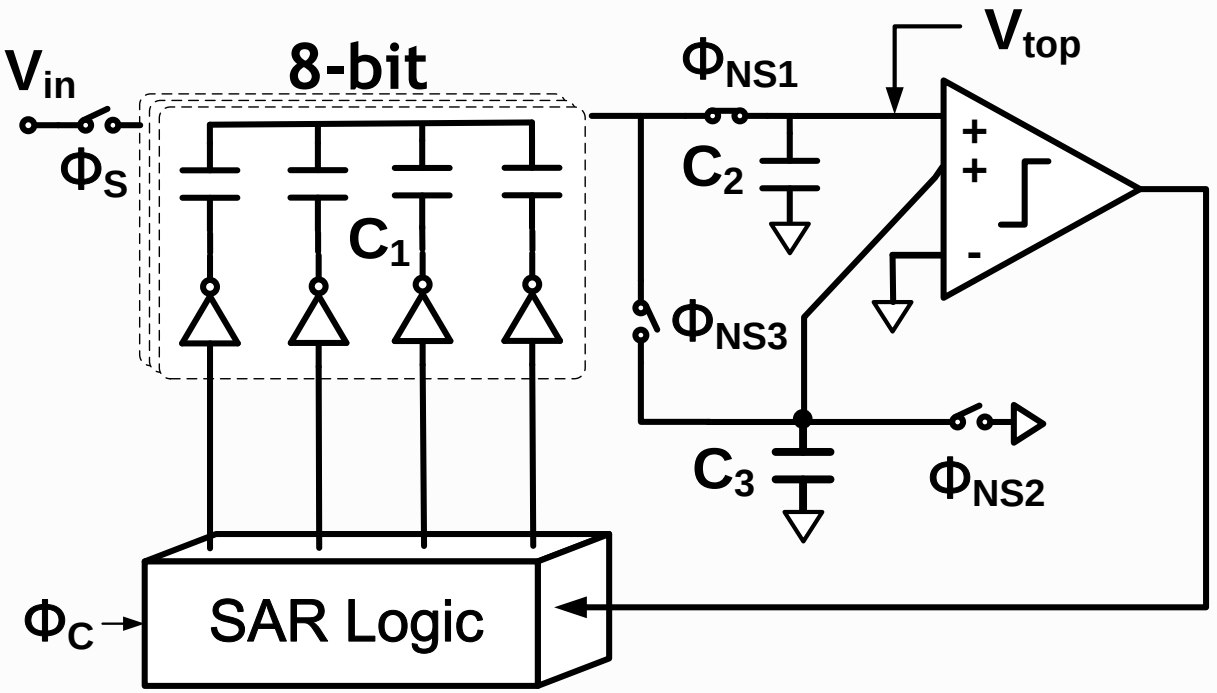


Total: 3 X C_1

☺ C_1<C, hence, proposal saves area

Circuit details

Total Circuit of FPNS-SAR ADC:

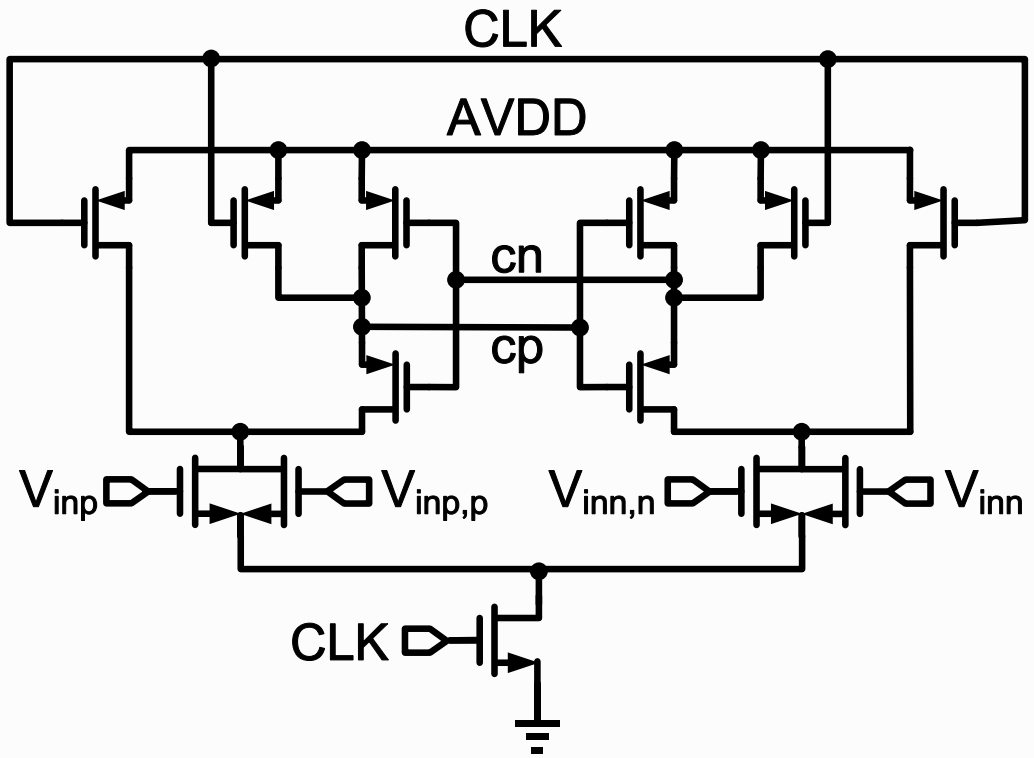


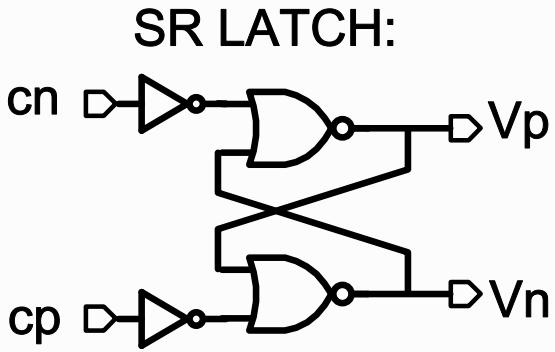
Asynchronous logic; 8-bit C-DAC

Different switches; four inputs comparator

Circuit details

Dynamic comparator [4]





Dynamic comparator, save power

[4] H. Wei, *et al.*, JSSC 2012

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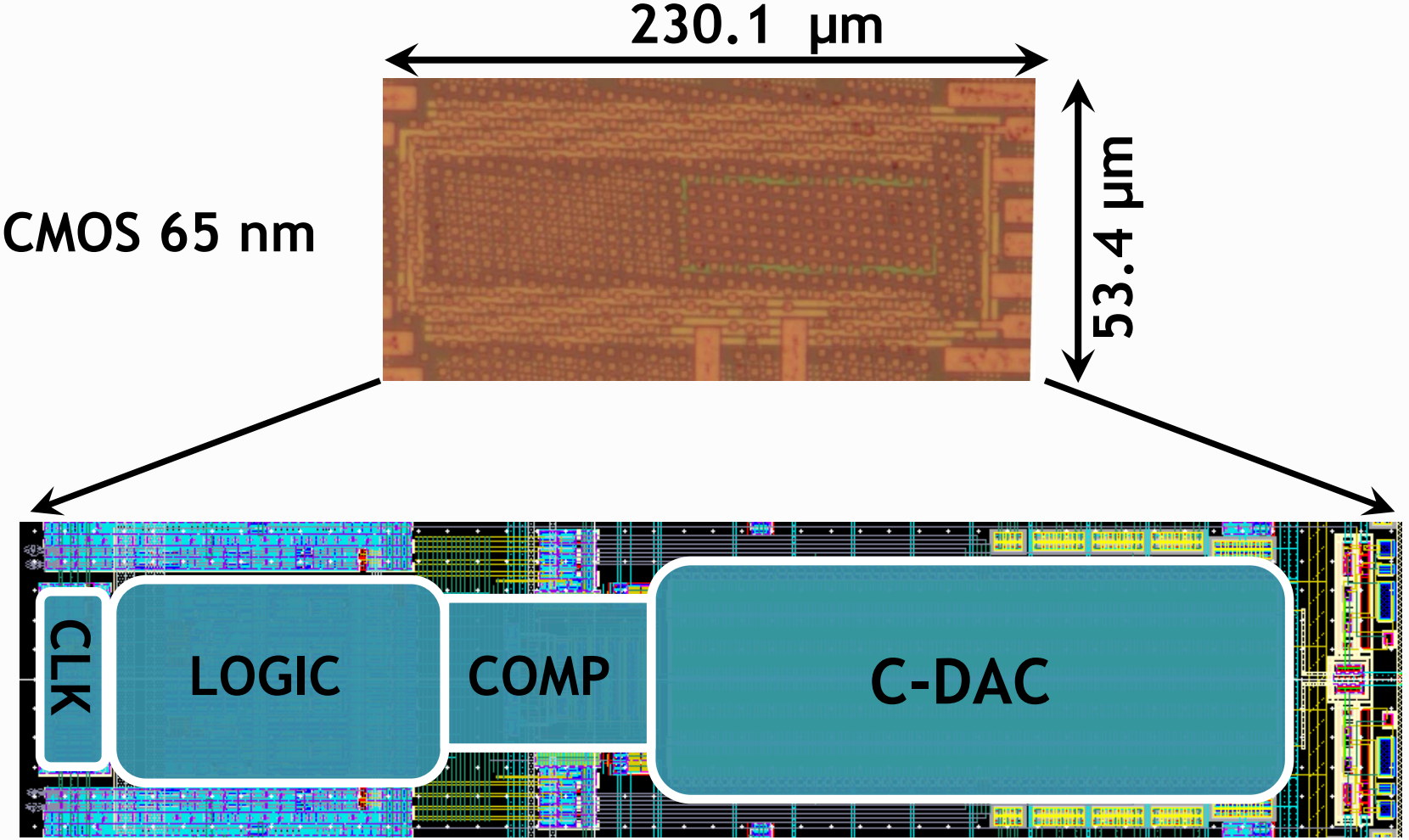
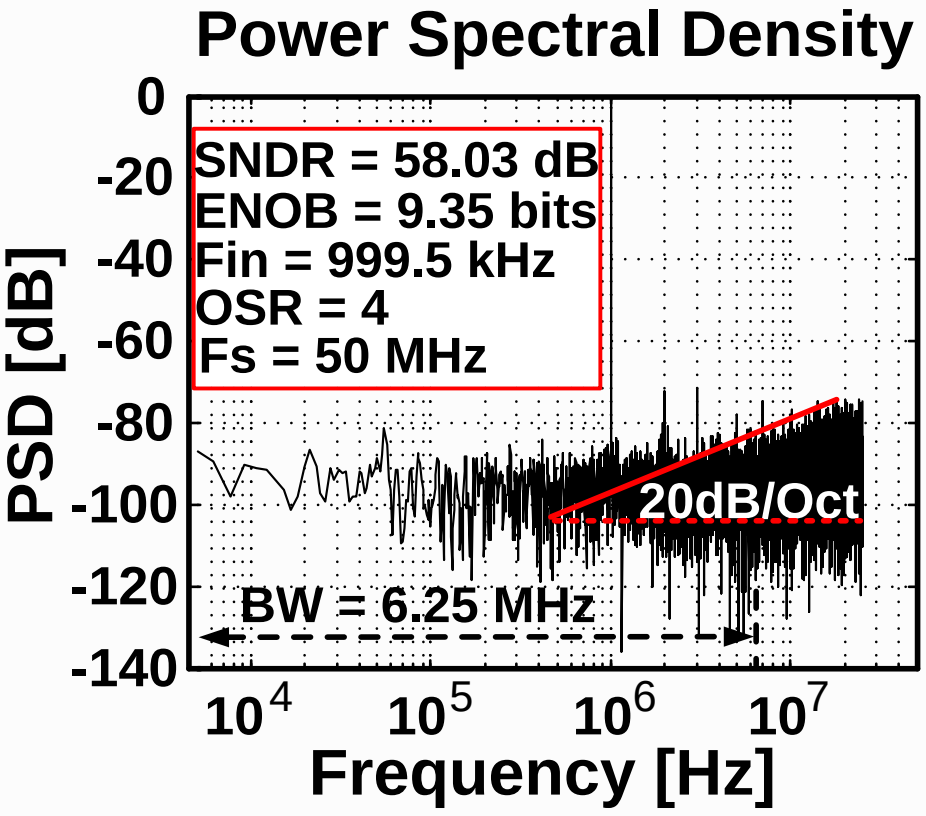
Chip photograph

CMOS 65 nm



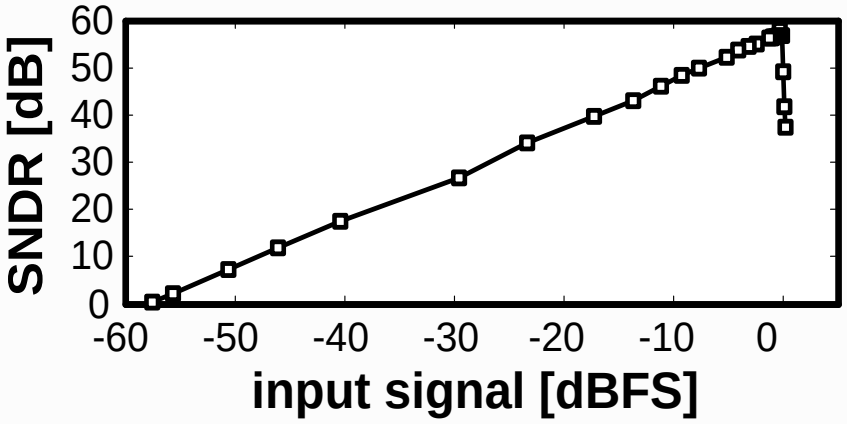
Experimental results

- **Realized 1st-order Noise Shaping**



Power supply: 0.8-V

Power : 120.7-μW



Experimental results-Comparison

	JSSC'10 [2]	JSSC'12 [3]	JSSC'12 [1]	This work
Architecture	SAR	CT-SDM	NS-SAR	FPNS-SAR
Noise Shaping / OTA	No/No	Yes/Yes	Yes/Yes	Yes/ No
Technology (nm)	65	130	65	65
Bandwidth (MHz)	0.5	15.6	11	6.25
Core Area (mm^2)	0.0259	0.27	0.0323	**0.0123**
Supply (V)	1	1.3	1.2	0.8
Power (μW)	1.9	4000	806	120.7
ENOB (bits)	8.75	9.6	10	9.35
FoM^W (fJ/conv.)	4.42	160	35.8	14.8

[1] J. A. Fredenburg , *et al.*, JSSC 2012 [3] A. Jain, *et al.*, JSSC 2012
[2] M. V. Elzakker, *et al.*, JSSC 2010

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Conclusion

- First work that realizes *Passive* noise shaping SAR, save power;
- Maintain basic architecture and operation of SAR-ADC, inherits advantage of SAR-ADC;
- No Opamp, most are digital circuits, robust to future technology and power supply downscaling;
- Relax the requirement of circuit blocks, save area and save power.

Acknowledgements

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