A 9.35-ENOB, 14.8 fJ/conv.-step Fully-Passive Noise-Shaping SAR ADC

Zhijie Chen, Masaya Miyahara, and Akira Matsuzawa

Tokyo Institute of Technology, 2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552, Japan
Tel, Fax: +81-3-5734-3764, E-mail: chen@ssc.pe.titech.ac.jp

Abstract

This paper presents an opamp-free solution to implement noise shaping in a successive approximation register analog-to-digital convertor. The comparator noise, incomplete settling error of digital-to-analog convertor and mismatch are alleviated. Designed in a 65 nm CMOS technology, the prototype realizes 58 dB SNDR at 50 MS/s sampling frequency. It consumes 120.7 μW from a 0.8 V supply and achieves a FoM of 14.8 fJ per conversion step.

Keywords: Charge redistribution, noise shaping, SAR ADC

Introduction

Charge-redistribution successive approximation register (SAR) analog-to-digital convertor (ADC) is a popular architecture for ADCs with moderate resolution and bandwidth [1]. The comparator noise and settling error from C-DACs limit the performance of a SAR ADC [2]. To solve these issues, [1] proposes noise shaping technique by using FIR filter and IIR filter, as shown in Fig. 1. Two capacitor banks based FIR filter is used to sample the residue voltages. Operational amplifier (opamp) based IIR filter acts as an active integrator to realize noise shaping function. However, the FIR filter not only introduces extra noise but also increases the ADC's area. In addition, opamp based integrator is hard to scale and its design becomes difficult with technology and supply voltage scaling.

This paper proposes fully passive noise shaping (FPNS) to solve the issues of comparator noise, digital-to-analog convertor (DAC) mismatch and settling error. This passive implementation has high power efficiency. The proposed design maintains the basic operation and architecture of a traditional SAR ADC, which is based on charge redistribution and consists largely of digital circuits. Therefore, this architecture is robust to low voltage operation and deeply scaled CMOS technologies.

Proposed FPNS-SAR ADC Architecture

Fig. 2 demonstrates the proposed architecture. After the conversion of a charge-redistribution SAR ADC, the residue voltage E on the top-plate of the DAC has all the ADC error information, including quantization noise, comparator noise, DAC mismatch and settling error. The prototype stores residue voltage in the DAC and then feeds the residue back to the input of the SAR ADC. After combining the charge of input and residue together, a new conversion begins. As the equations shown in Fig. 2, this technique can realize 1st order noise shaping. That means 1st order noise shaping has attenuation effect to all ADC errors. As illustrated in Fig. 3 (a) and (b), the traditional SAR ADC architecture suffers from comparator noise, DAC mismatch and settling error while the proposed FPNS-SAR suppresses such non-ideal effect by noise shaping.

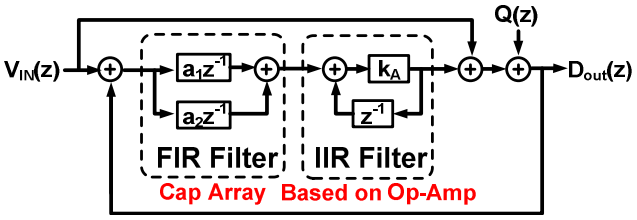

Fig. 1 Conventional noise shaping SAR architecture.

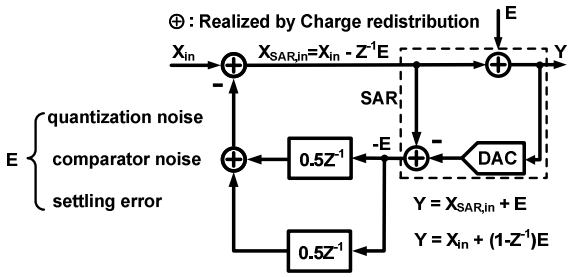

Fig. 2 Proposed FPNS-SAR ADC architecture

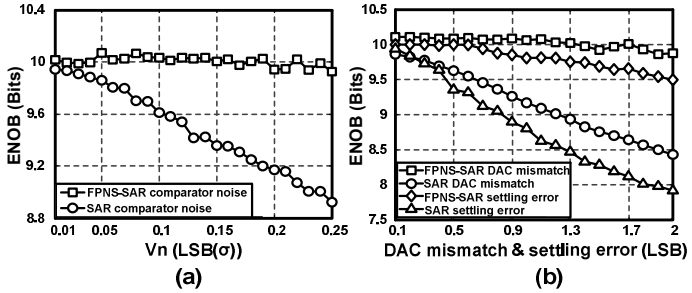

Fig. 3 Simulated (a) comparator noise effect and (b) DAC mismatch and settling error effect.

Circuit Implementation

In Fig. 4 (a)-(e), it explains the detail circuit operation sequence and shows how to realize 1st order noise shaping using charge redistribution. A differential scheme is implemented and a single-ended schematic is shown for simplicity.

The most important step is to obtain the entire residue voltage and then feed the residue back to the input of the SAR ADC before the next conversion begins. C_2 and C_3 are used to obtain the residue. As shown in Fig. 4, there are two positive inputs in the comparator. C_1 and C_2 are connected to one of the positive inputs while C_3 is connected to the other one. After a conversion (cycle N-1), the residue E is left on the top-plate of C-DAC (C_1 and C_2). The top-plate of C_2 is used to keep half of the residue voltage, where $V_{top}(N\text{-}1)=-E(N\text{-}1)/2$. In order to compensate for the loss of half of the residue on C_2, C_3 is introduced to the architecture. C_3 obtains half of the top-plate voltage ($V_{C3}=V_{top}(N\text{-}1)/2$) from C_1 due to charge sharing. After the next cycle (cycle N) finishes sampling and before the conversion begins, the input and the half residue on the top-plate of C_2 are combined together. Then, the positive inputs of comparator become $V_{in}(N)/2+V_{top}(N\text{-}1)/2+V_{C3}$. As the equations in Fig. 4 (e) explain, the $V_{DAC}(N)$, which represents digital output of SAR ADC at cycle N, equals to $V_{in}(N)+E(N)-E(N\text{-}1)$. Therefore, with the help of C_2 and C_3, a full residue of previous cycle (cycle N-1) is fed back to the current cycle (cycle N). In another word, 1st order passive noise shaping is realized with such technique.

The proposal uses capacitor $C_1=C_2=C_3$. With the help of noise shaping, the resolution can be improved by 2-b when over sampling ratio (OSR) is 4 and noise shaping order is 1.

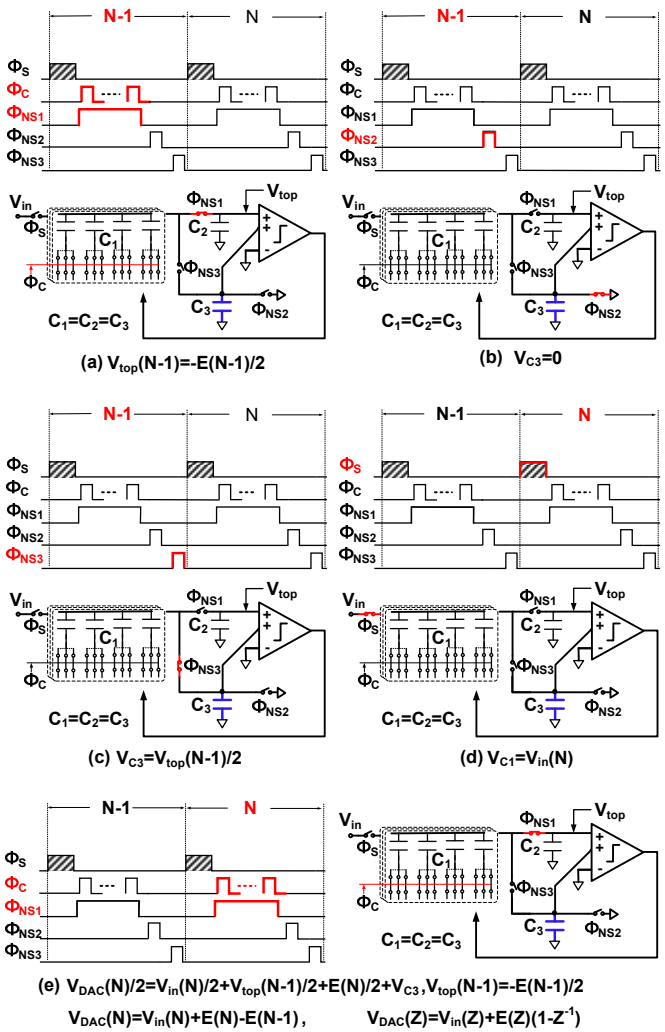

Fig. 4 Circuit operation (a) half noise left in the top plate of C_2; (b) Clear the charge of C_3; (c) Sharing charge between C_1 and C_3; (d) Sample the next input; (e) Begin the next conversion.

For instance, for an 8-b C-DAC architecture, the 10-b resolution can be achieved when OSR is 4 and noise shaping order is 1. Therefore, for a 10-b FPNS-SAR ADC architecture, it only uses $3\times C_1$ (C_1 is the value of 8-b C-DAC). However, for a traditional SAR ADC architecture, it needs $4\times C_1$ to implement 10-b ADC. In other words, the FPNS-SAR uses a smaller capacitance to realize a higher resolution ADC. Since capacitors dominate the area in a SAR ADC, the area can be reduced when compared with the traditional SAR ADC architecture. Moreover, with the smaller capacitance and its higher tolerance to settling error, this architecture has the potential to achieve higher operation speed.

Experimental Results

The prototype FPNS-SAR ADC is designed with 8-b C-DAC and an OSR of 4. It is fabricated in a 65 nm CMOS technology with a core area of 0.012 mm^2. With 50 MS/s and 0.8 V supply, Fig. 5 shows the measured spectrum with 1st order noise shaping, giving an SNDR of 58 dB. The die photograph is shown in Fig. 6.

The performance comparison with state-of-the-art results are shown in Table I.

Conclusion

The proposed fully passive technique can realize 1st order noise shaping. This technique suppresses quantization noise, comparator noise, DAC mismatch and settling error. This passive implementation enhances power efficiency. Moreover, since it maintains the basic operation of a traditional SAR ADC, it inherits the merits of a SAR ADC which is robust to low voltage operation and technology scaling.

Acknowledgements

This work was partially supported by HUAWEI, Berkeley Design Automation for the use of the Analog Fast SPICE (AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

References

[1] J. Fredenburg, *et al.*, *JSSC* 2012, pp. 2898-2904.
[2] V. Giannini, *et al.*, *ISSCC* 2008, pp. 238-239.
[3] M. V. Elzakker, *et al.*, *JSSC* 2010, pp. 1007-1015.
[4] M. Yip., *et al.*, *ISSCC* 2011, pp. 190-192.
[5] A. Jain., *et al.*, *JSSC* 2012, pp. 1615-1625.

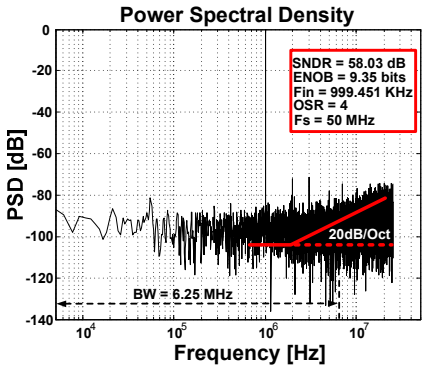

Fig. 5 Measured PSD.

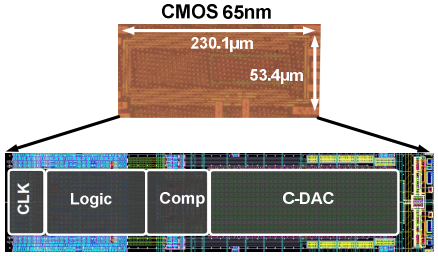

Fig. 6 Die photograph.

Table I Performance comparison

	JSSC'10 [3]	ISSCC'11 [4]	JSSC'12 [5]	JSSC'12 [1]	This work
Architecture	SAR	SAR	CT-SDM	NS-SAR	FPNS-SAR
OTA	No	No	OTA	OTA	No
Noise Shaping	No	No	Yes	Yes	Yes
Technology (nm)	65	65	130	65	65
Resolution (bit)	10	10	10	10	10
Bandwidth (MHz)	0.5	0.01	15.6	11	6.25
Core Area (mm^2)	0.0259	0.353	0.27	0.0323	**0.0123**
Supply (V)	1	1	1.3	1.2	0.8
Power (μW)	1.9	0.206	4000	806	120.7
ENOB (bit)	8.75	8.84	9.6	10	9.35
FoM^W (fJ/conv.)	4.42	22.4	160	35.8	14.8