Delta-Sigma Time to Digital Converter Using Charge Pump and SAR ADC

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Outline

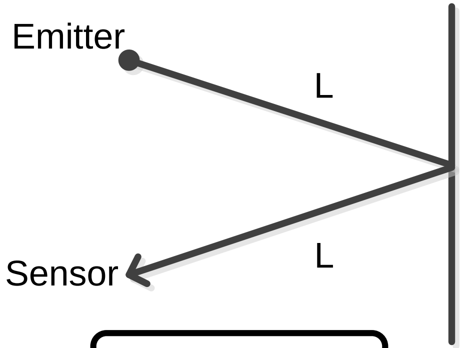
- **Background**
- **Basic concept**
- **Circuit design**
- **Simulation results**
- **Conclusion**

Background

- **TDC Application**
  - **3D camera**
  - **Laser range finder**
  - **Time-of-flight (TOF) particle detector**
  - **On chip jitter measurement**
  - **PLL and frequency synthesizer**

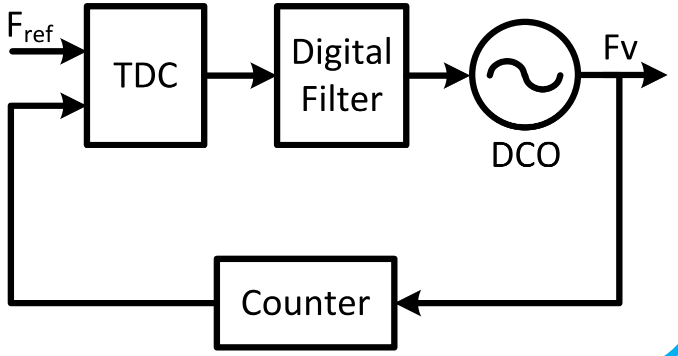
- **Contradictory requirements**
  - **High resolution (~1ps)**
  - **Wide input range (several ns)**

Distance measurement



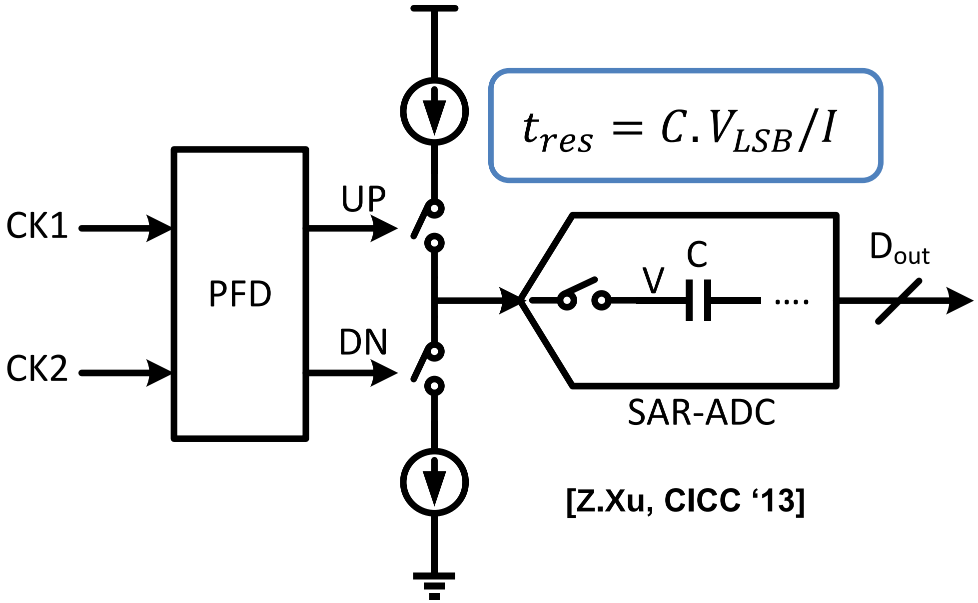
$$L = c.t/2$$

ADPLL



Previous Work

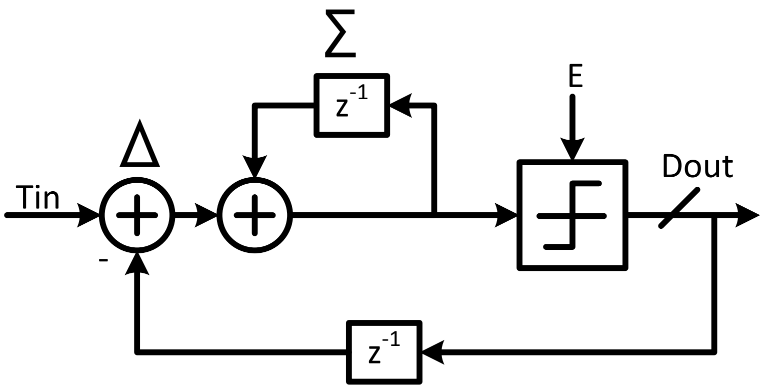
- **Charge pump and SAR ADC**
- **Time-to-charge conversion with SAR ADC → high resolution**
- **SAR-ADC: compact, sufficient range, and moderate speed**
- **Challenge: high order SAR ADC is required**
  - **High design complexity**
  - **Limited speed**
  - **Large area**

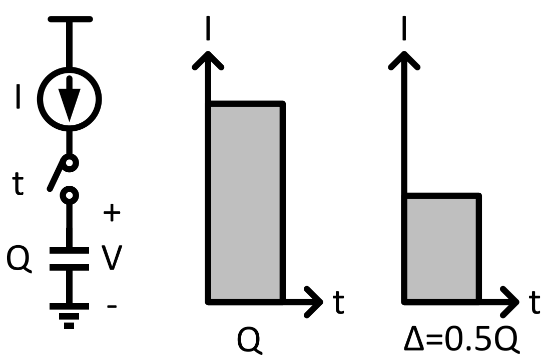


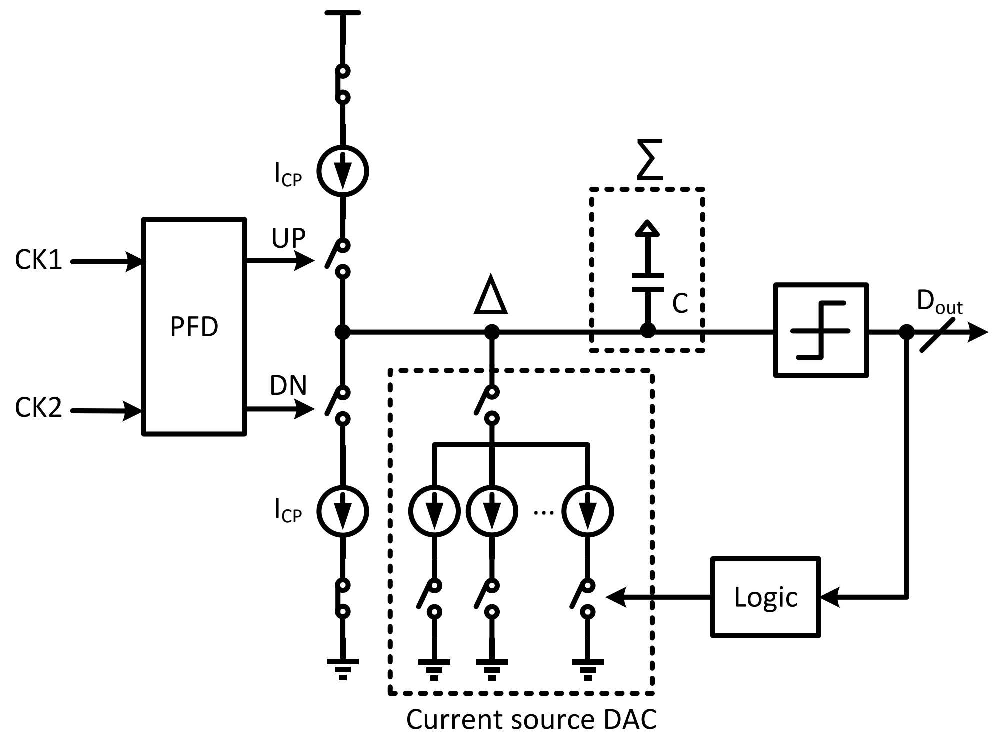
[Z.Xu, CICC '13]

Proposal: ΔΣ TDC

- Σ is realized by charging capacitor C and never reset it
- Δ is realized by discharging/charging C through array of current source DAC at constant time for positive/negative output

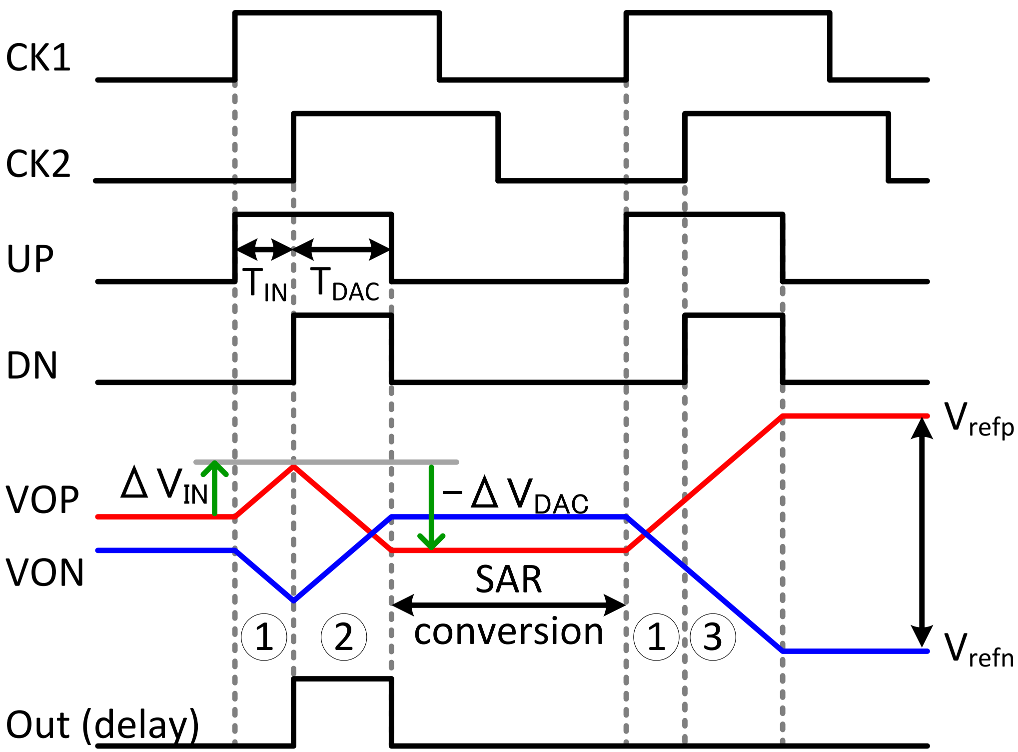






Timing Diagram

- $\Delta V_{max} = \Delta V_{IN,max} + \Delta V_{DAC,max}$
- $\frac{1}{2}\left(V_{refp} - V_{refn}\right) = \frac{I_{CP} \cdot T_{IN,max}}{C_{DAC}} + \frac{\Sigma I_{DAC} \cdot T_{DAC}}{C_{DAC}}$



ΔΣ thumb rule:

$$\left|\Delta V_{IN,max}\right| = \left|\Delta V_{DAC,max}\right|$$

For VOP:

1. **Charging input**
2. **HIGH output → discharge**
3. **LOW output → charge**

Multibit Quantizer Effect

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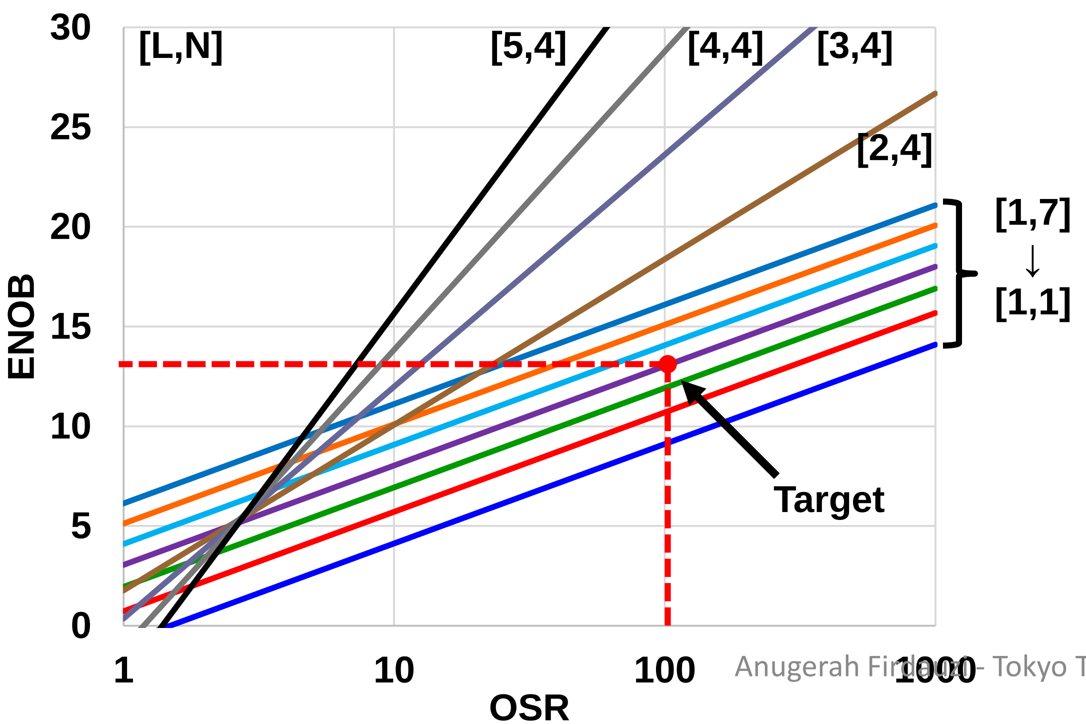
- For L^{th} order ΔΣ ADC with N bit quantizer:
  - $SNR_{dB} = 10\ \log\left(\frac{3\pi}{2}\left(2^N - 1\right)^2 (2L+1)\left(\frac{OSR}{\pi}\right)^{2L+1}\right)$
  - $ENOB = (SNR_{dB} - 1.76)/6.02$
- Increasing quantizer size by one can improve ENOB 1-1.5 bit



Target:

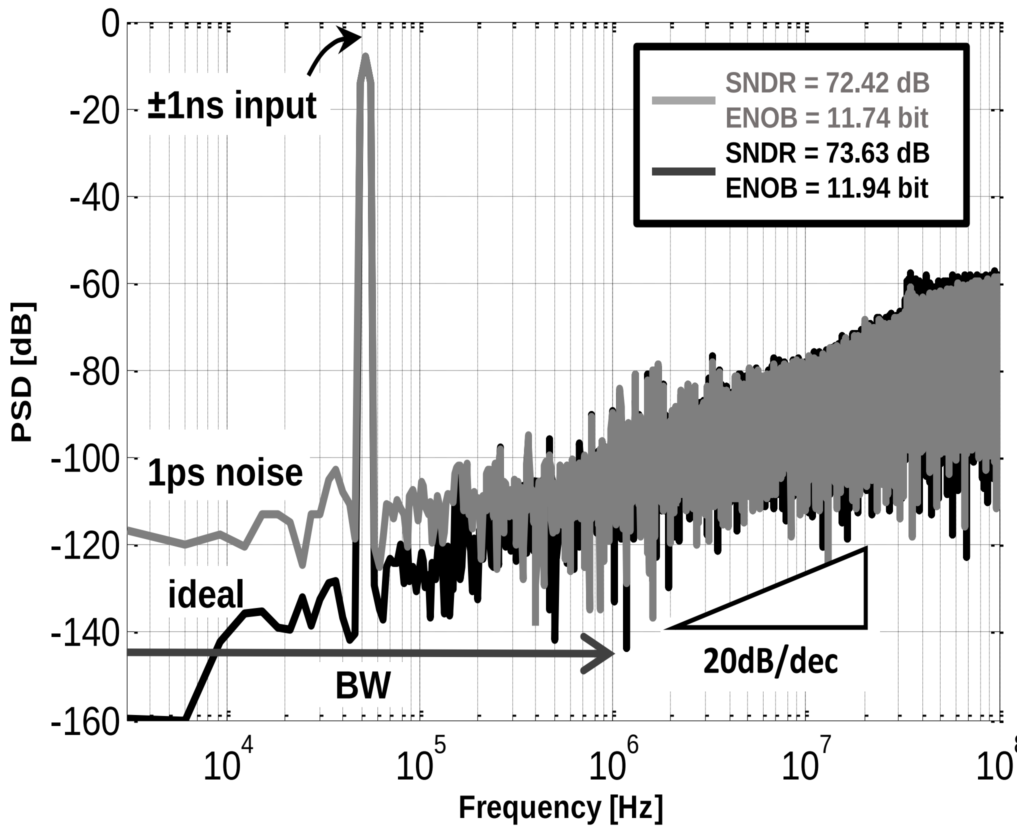
- 1st order ΔΣ TDC
- Quantizer 4 bit
- OSR = 100
- ENOB = 13 bit

Matsuzawa & Okada Lab.

Simulation Result

- **Ideal model using MATLAB**
- **4 bit quantizer**
- **Input = ±1ns at 52kHz**
- **BW = 1MHz**
- **OSR = 100**

- **Result:**
  - **ENOB > 11bit**
  - **Effective resolution < 0.9ps**



Conclusion

- **A new approach for TDC by using ΔΣ architecture is proposed.**
- **ΔΣ TDC implemented by using CP SAR ADC, and current source DAC gives first order noise shaping and high resolution for moderate bandwidth while keeping the input range large and power consumption low**