Delta-Sigma Time to Digital Converter Using Charge Pump and SAR ADC

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1. Introduction

One of the straightforward methods for time to digital conversion is using time to charge conversion by using charge pump which is then connected to a SAR ADC for digital conversion [1]. The SAR ADC, while it is convenient for providing both charge storage and conversion, also provides high challenges for more than 10 bits resolution design while maintaining its speed high.

In this paper, lower-bit SAR ADC is used to obtain smaller area and lower power consumption. To overcome the resolution drop, delta-sigma (ΔΣ) structure using oversampling is used. Furthermore, the noise-shaping can also significantly reduce in-band quantization noise from SAR ADC.

2. Circuit Design

The architecture of the proposed ΔΣ TDC is presented in Fig.1. In this architecture, a charge-pump is used to convert the time difference input, T_{IN}, into charge which is then stored in the SAR CDAC. Between each conversion, ideally the charge stored in SAR CDAC is constant, thus by never resetting the SAR, the charge stored on each conversion cycle is accumulated and an integrator (Σ) can be obtained.

To implement the Δ, SAR ADC quantization output is used as selector for the current source DAC to discharge/charge SAR CDAC in a constant time interval, T_{DAC}, for positive/negative output in the next conversion cycle. In this way, a first order ΔΣ TDC with SAR ADC as quantizer can be implemented.

In ΔΣ system, integrator input needs to be kept close to zero by making feedback DAC in the same level with the input. For the case of this TDC, maximum charge from the input must be equal with total charge from the feedback, or $\max(T_{IN}).I_{CP} = T_{DAC}.\Sigma I_{DAC}$, where I_{CP} is the charge pump current and ΣI_{DAC} is the total current from current source DAC.

Multibit quantization using 4 bit SAR ADC is used in this structure to improve the first order ΔΣ TDC's resolution by 1-1.5 bit for every quantization bit increase. Higher resolution SAR ADC is not required since the resolution in ΔΣ modulator is determined mostly by the oversampling rate (OSR) and filter/integrator order. In this way, the design of SAR ADC can be kept simple, fast, and low power. Faster SAR ADC will allow the use of higher OSR and doubling the OSR can improve the resolution by 1.5 bit.

3. Simulation Results

The proposed structure was simulated by using MATLAB with ±1ns full-scale input difference at 52 kHz, 1 MHz bandwidth, OSR=100, for ideal condition and with 1 ps charge-pump noise.

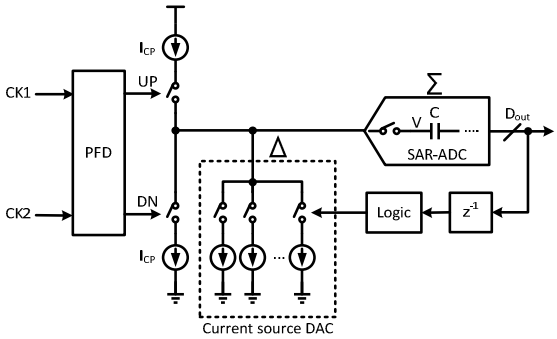

Fig. 1. Delta-sigma TDC architecture

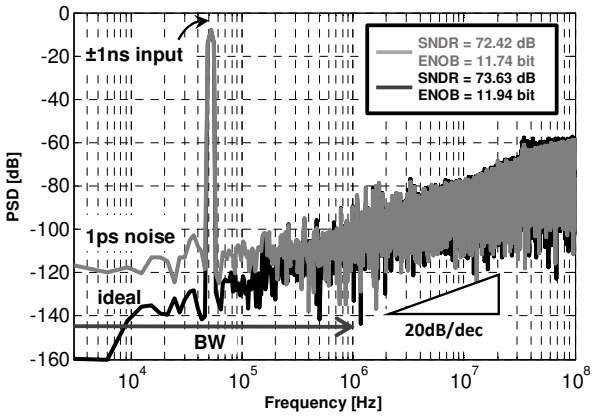

Fig. 2. Simulation result

As presented in Fig.2, the simulation results shows 20 dB/dec noise shaping, and the noise floor became higher when the noise is applied. Both simulation results give SNDR higher than 72 dB, and ENOB more than 11 bit, or less than 0.9 ps effective resolution.

4. Conclusion

A new approach for TDC by using ΔΣ architecture with charge domain analysis is proposed. The ΔΣ TDC implemented by using charge-pump, SAR ADC, and current source DAC gives first order noise shaping and high resolution for moderate bandwidth while keeping the input range large and power consumption low.

Acknowledgment

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References

[1] Z. Xu, S. Lee, M. Miyahara, and A. Matsuzawa, "A 0.84ps-LSB 2.47mW time-to-digital converter using charge pump and SAR-ADC", IEEE Custom Integrated Circuits Conference (CICC) 2013