19.5 An HCI-Healing 60GHz CMOS Transceiver

Rui Wu, Seitaro Kawai, Yuuki Seo, Kento Kimura, Shinji Sato, Satoshi Kondo, Tomohiro Ueno, Nurul Fajri, Shoutarou Maki, Noriaki Nagashima, Yasuaki Takeuchi, Tatsuya Yamaguchi, Ahmed Musa, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Tokyo, Japan

The research of 60GHz CMOS transceivers has bloomed due to their capability of achieving low-cost multi-Gb/s short-range wireless communications [1]. Considering practical use of the 60GHz CMOS transceivers, longer operation lifetime with high output power is preferred to provide reliable products. Unfortunately, as indicated in [2], the output power capability of the transmitter will gradually degrade due to the hot-carrier-injection (HCI) effects in the standard CMOS transistors at large-signal operation (*e.g.* power amplifiers). It is because the inherently large voltage swing at the output of the power amplifiers (PAs) is the main source of the HCI damage. Unfortunately, a thick-oxide transistor, a common solution for reliability issues at lower frequencies, cannot be utilized for 60GHz CMOS PA design due to its limited maximum oscillation frequency (f_{max}).

Conventional solutions are demonstrated to be very effective to solve the HCI issues for the 60GHz CMOS PAs. Lowering the supply voltage [2,3] and using cascode topology [4] can greatly reduce the HCI damage at the cost of low output power, linearity, and efficiency. Power combining [5] and beamforming [6] techniques can be used to compensate the degraded output power and linearity. However, the deteriorated efficiency remains unimproved. This paper presents a 60GHz CMOS transceiver with HCI damage healing function, which can detect the HCI damage to the transistor used in the PA and heal it afterwards. The proposed HCI-healing technique relieves the trade-off between the HCI reliability and the system performance, which guarantees longer operation lifetime with high output power. The proposed transceiver demonstrates an EVM of -27.9dB in 16QAM and can transmit 7Gb/s within 2.16GHz bandwidth. The transmitter, receiver, and PLL consume 174mW, 144mW, and 44mW from a 1.2V supply, respectively.

A non-volatile memory using a standard CMOS transistor has been reported with 100-times program/erase endurance [7], where the charge trap and ejection mechanism in gate oxide is applied to control the threshold voltage. The HCI effects have the same damaging mechanism as the charge trap, which degrade the threshold voltage (V_t), channel carrier mobility (μ), unit-area gate oxide capacitance (C_{ox}), and therefore drain current [2]. In this work, a charge-ejection technique is applied to a mm-Wave power amplifier as shown in Fig. 19.5.1. The proposed HCI-healing transistor module is composed of a core NMOSFET with deep n-well, a tail-switching transistor, an MIM transmission line (MIM TL) with a MIM capacitor array attached alongside, and a high-density decoupling capacitor. The body terminal of the core NMOSFET (V_B) is connected to the HCI-healing bias (V_H) through a current-limiting resistor. When the module is in HCI-healing status, the tail transistor is switched off, which creates a high impedance (high Z) terminal for the source of the core NMOSFET. A high voltage is applied to V_H generating a strong vertical electric field between substrate and gate to eject and neutralize the trapped electrons [7]. Meanwhile, the drain side is forward biased for assisting the HCI-healing procedure. In this work, an external 10V voltage source is used for V_H. The measured peak current is 3.9mA corresponding to a V_B of 2.2V. On the other hand, in order to maintain the transistor performance for the 60GHz operation, the MIM TL and high-density capacitor are connected to the source of the core NMOSFET forming an RF ground.

Figure 19.5.2 demonstrates the HCI-healing capability of the proposed technique when applied to a transistor and a 60GHz CMOS power amplifier. The I_D-V_G curves of the stand-alone HCI-healing transistor TEG are measured at V_D=1.2V. An accelerated DC stress of V_D=2.4V is applied, causing the HCI damage. Then the proposed HCI-healing technique is used to recover the drain current (I_D). The HCI damage is mainly observed as a V_t shift. Although adaptively increasing gate bias voltage (V_G) also can compensate I_D, the HCI effects are strengthened by the increased V_G, shortening the lifetime of the transistor. The measured P_{in}-P_{out} performance of the stand-alone PA TEG at 60GHz is shown in Fig. 19.5.2. The solid gray line is for an undamaged fresh PA showing a 1dB compression power (P_{1dB}) of 7dBm. The accelerated DC stress (V_{DD6}=2.4V) is applied to the last stage, which causes more than 1dB degradation of P_{1dB}. After the HCI-healing function is enabled, a full recovery of the P_{1dB} can be observed. It also can be seen that the small-signal gain of the PA is not fully recovered because of small degradation in μC_{ox}.

Figure 19.5.3 shows the detailed 60GHz CMOS PA with the proposed HCI-healing function. The proposed technique is utilized for the last stage of the PA which suffers the most from the HCI effects. The switches (M_p, M_c, M_n, and S_{G6}) are used to realize the proposed HCI-healing technique, in which M_p and M_c are designed to be large and small sizes, respectively, for HCI damage detection. The lifetime measurement results of the power amplifier are depicted in Fig. 19.5.3 with the drain current of the last stage (I_{D6}) measured under V_{G6}=0.7V and V_{D6}=1.2V. It can be observed that a lifetime of 81.2 years is achieved for the PA after the HCI-healing function is activated, which keeps outputting a 7dBm continuous-wave signal. In a practical use, due to the large peak-to-average power ratio of the modulation signal, the HCI damage is smaller than that of the continuous-wave signal at 1dB compression [4]. Therefore, one healing event is adequate during the lifetime of the device.

Figure 19.5.4 shows the 60GHz HCI-healing transceiver design using direct-conversion topology. The carrier signal is generated through a 20GHz PLL with a 40MHz reference and quadrature injection-locked oscillators (QILOs). The on-chip logic is integrated to achieve the gain control, power management, and HCI-healing function. The measured saturated output power (P_{sat}) of the transmitter is 11.3dBm at the center frequency of 63.72GHz excluding the PCB loss, and the P_{1dB} is 6.3dBm. The PCB loss is estimated by calculating the measured P_{sat} difference between a stand-alone PA and a transceiver chip integrated on a PCB.

Figure 19.5.5 shows the measured EVM performance of the transmitter at different output power. The carrier frequency of the modulated signal is 63.72GHz. The symbol rate is 1.76GS/s in 16QAM with a roll-off factor of 25%. The same PCB configured for TX mode is used in three different TX damaging statuses. It is shown that for the undamaged TX, the output power is 9.3dBm when a TX EVM of -21dB is achieved. After the HCI damage occurred, the output power of the TX is reduced to 5.3dBm for the same value of TX EVM. Finally the output power of the TX are recovered to 7.8dBm at TX EVM = -21dB by activating the HCI-healing function.

Figure 19.5.6 shows a comparison table for 60GHz CMOS transceivers. This paper presents a 60GHz transceiver with HCI-healing function, which guarantees over 81-year lifetime without sacrificing the output power and efficiency.

Figure 19.5.7 shows the die micrograph. The transceiver is fabricated in a 65nm CMOS technology. The core area of the transceiver is 2.3 mm^2.

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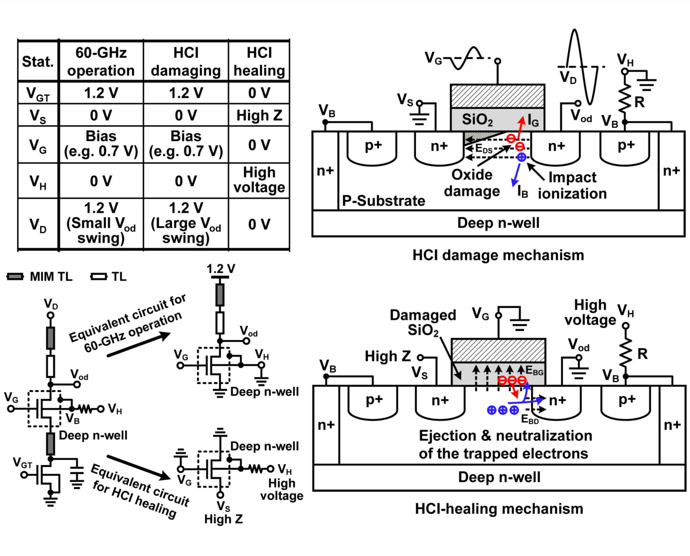
References:
[1] K. Okada, *et al.*, "A 64-QAM 60GHz CMOS Transceiver with 4-Channel Bonding," *ISSCC Dig. Tech. Papers*, pp. 346-347, Feb. 2014.
[2] M. Tanomura, *et al.*, "TX and RX Front-Ends for 60GHz Band in 90nm Standard Bulk CMOS," *ISSCC Dig. Tech. Papers*, pp. 558-559, Feb. 2008.
[3] T. Tsukizawa, *et al.*, "A PVT-variation tolerant fully integrated 60GHz transceiver for IEEE 802.11ad," *IEEE Symp. VLSI Circuits*, pp.123-124, June 2014.
[4] A. Siligaris, *et al.*, "A 60GHz power amplifier with 14.5dBm saturation power and 25% peak PAE in CMOS 65 nm SOI," *IEEE J. Solid-State Circuits*, vol.45, no. 7, pp.1286-1294, July 2010.
[5] J. Chen, *et al.*, "A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 432-433, Feb. 2011.
[6] M. Boers, *et al.*, "A 16TX/16RX 60GHz 802.11ad Chipset with Single Coaxial Interface and Polarization Diversity," *ISSCC Dig. Tech. Papers*, pp. 344-345, Feb. 2014.
[7] K. Miyaji, *et al.*, "Zero additional process, local charge trap, embedded flash memory with drain-side assisted erase scheme using minimum channel length/width standard CMOS single transistor cell," *Japanese J. Appl. Phys.*, vol. 51, pp. 04DD02-1-04DD02-7, Apr. 2012.
[8] T. Mitomo, *et al.*, "A 2Gb/s-Throughput CMOS Transceiver Chipset with In-Package Antenna for 60GHz Short-Range Wireless Communication," *ISSCC Dig. Tech. Papers*, pp. 266-267, Feb. 2012.
[9] T. Tsukizawa, *et al.*, "A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications," *ISSCC Dig. Tech. Papers*, pp. 230-231, Feb. 2013.



Stat.	60-GHz operation	HCI damaging	HCI healing
V_{GT}	1.2 V	1.2 V	0 V
V_S	0 V	0 V	High Z
V_G	Bias (e.g. 0.7 V)	Bias (e.g. 0.7 V)	0 V
V_H	0 V	0 V	High voltage
V_D	1.2 V (Small V_{od} swing)	1.2 V (Large V_{od} swing)	0 V

Figure 19.5.1: Proposed HCI damage healing technique for PA.

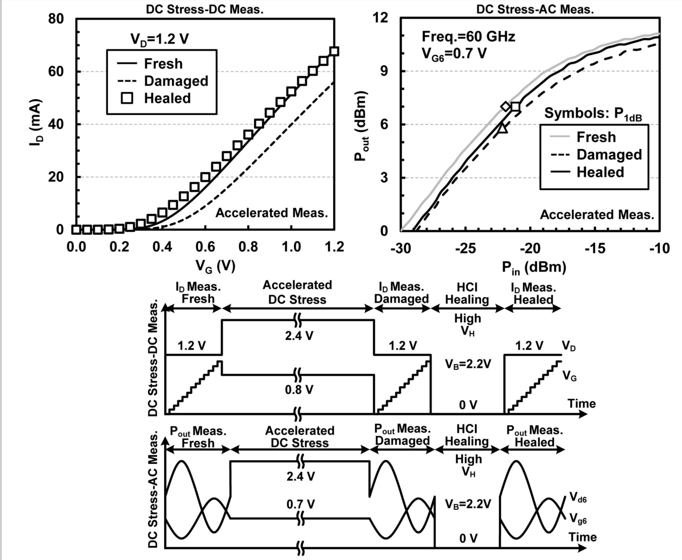


Figure 19.5.2: Measured I -V curve and P_{in}-P_{out} of stand-alone TEGs.

Stat. \ Pin	S_{6a}	S_{6b}	S_{6c}	EN_{CMP}	EN_C	EN_{DAC}	V_{G6}
60GHz Operation	On	On	Off	Dis.	Dis.	En.	DAC_{out}
HCI Detection	Off	On	Off	En.	Dis.	En.	DAC_{out}
HCI Healing	Off	Off	On	Dis.	Dis.	Dis.	Gnd

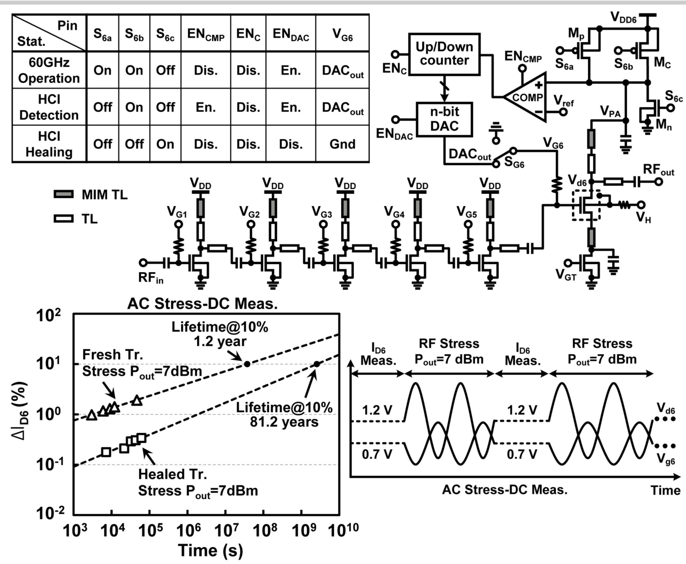


Figure 19.5.3: 60GHz CMOS PA with HCI-healing function.

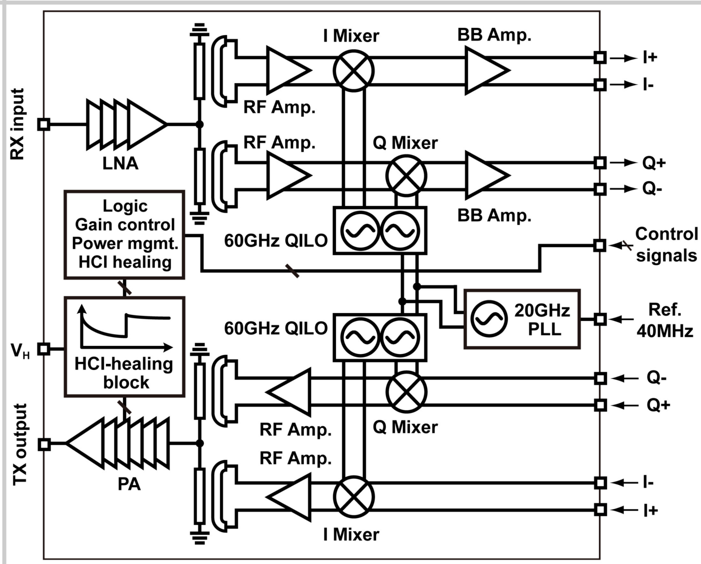


Figure 19.5.4: Block diagram of 60GHz HCI-healing transceiver.

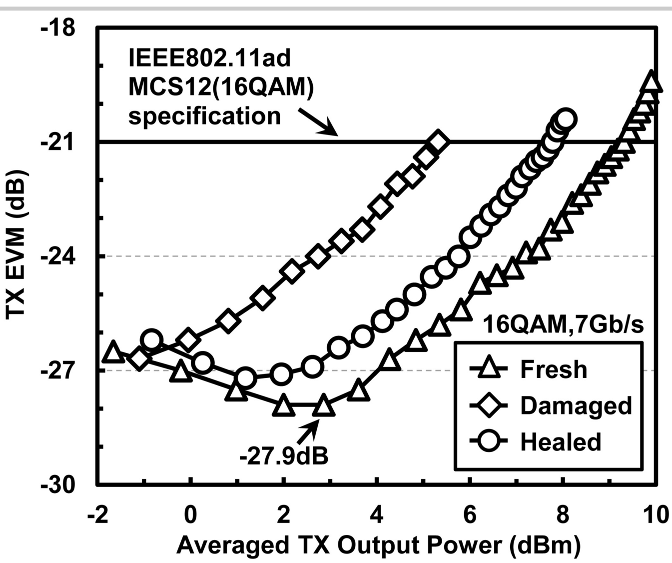
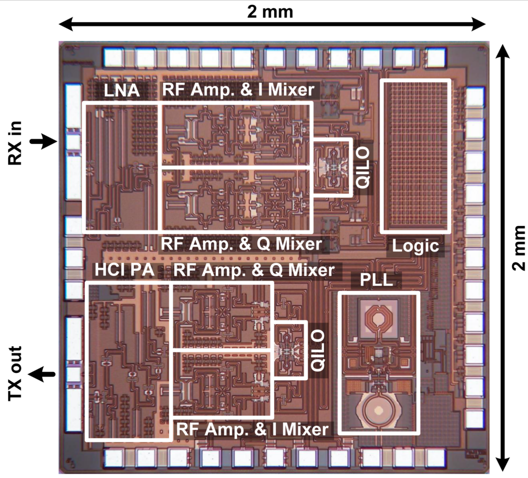


Figure 19.5.5: Measured TX EVM performance at different TX P_{out}.

	Data rate (Modulation)	P_{out} /each PA (dBm)	TX efficiency P_{out}/P_{DC} (%)	Life-time (year)	HCI healing	Core area (mm²)	Power Consumption
Tokyo Tech [1]	10.56Gb/s (64QAM) 28.16Gb/s (16QAM)	8.5* @TX EVM = -21dB	2.8	N/A	NO	3.9	TX: 251mW RX: 220mW
NEC [2]	2.6Gb/s (QPSK)	6	3.0 w/o PLL	11415	NO	3.4	TX: 133mW RX: 206mW w/o PLL
Panasonic [3]	2.5Gb/s (QPSK)	1.9 @TX EVM = -19.6dB	0.4	N/A	NO	5.7	TX: 361mW RX: 260mW
Broadcom [6]	4.6Gb/s (16QAM)	-4* @TX EVM = -23dB	0.5	N/A	NO	26.3**	TX: 1190mW RX: 960mW 16x16 array
Toshiba [8]	2.6Gb/s (QPSK)	N/A	N/A	N/A	NO	2.9	TX: 160mW RX: 233mW
Panasonic [9]	2.5Gb/s (QPSK)	2 @TX EVM = -22dB	0.5	N/A	NO	13.5**	TX: 347mW RX: 274mW
This work	7Gb/s (16QAM)	9.3 @TX EVM = -21dB	3.9	81	YES	2.3	TX: 218mW RX: 188mW

*Estimated from literature **Chip area

Figure 19.5.6: Performance comparison of 60GHz CMOS transceivers.



	TX	RX	PLL	Logic
Area (mm^2)	0.79	1.01	0.27	0.21

Figure 19.5.7: Die micrograph.