

An HCI-Healing 60GHz CMOS Transceiver

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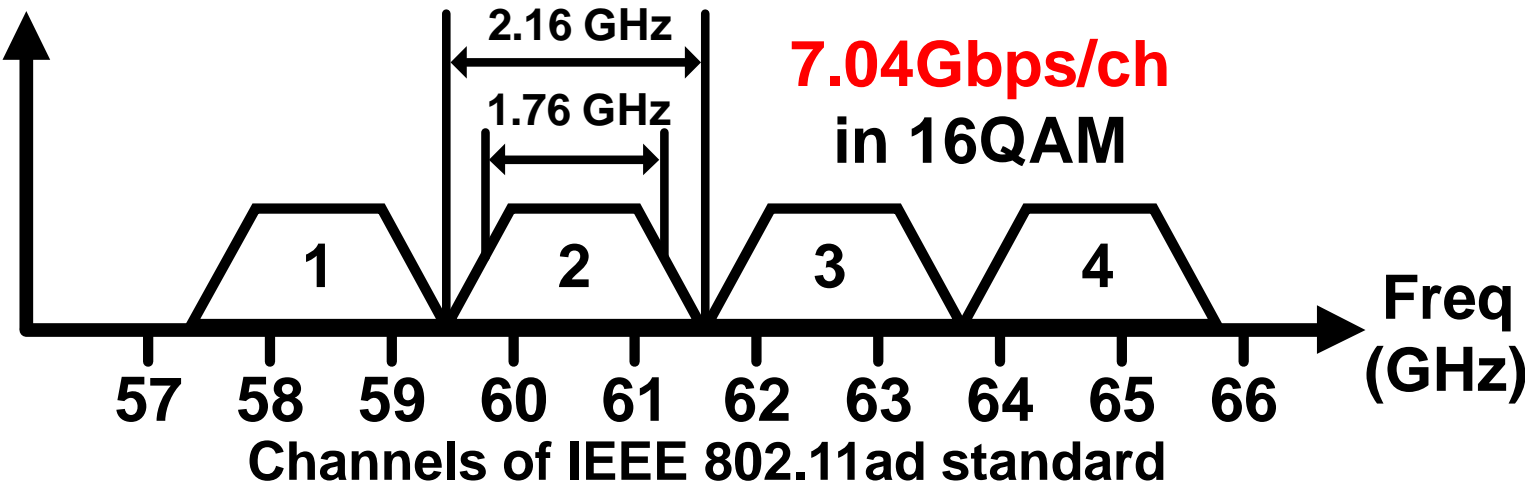
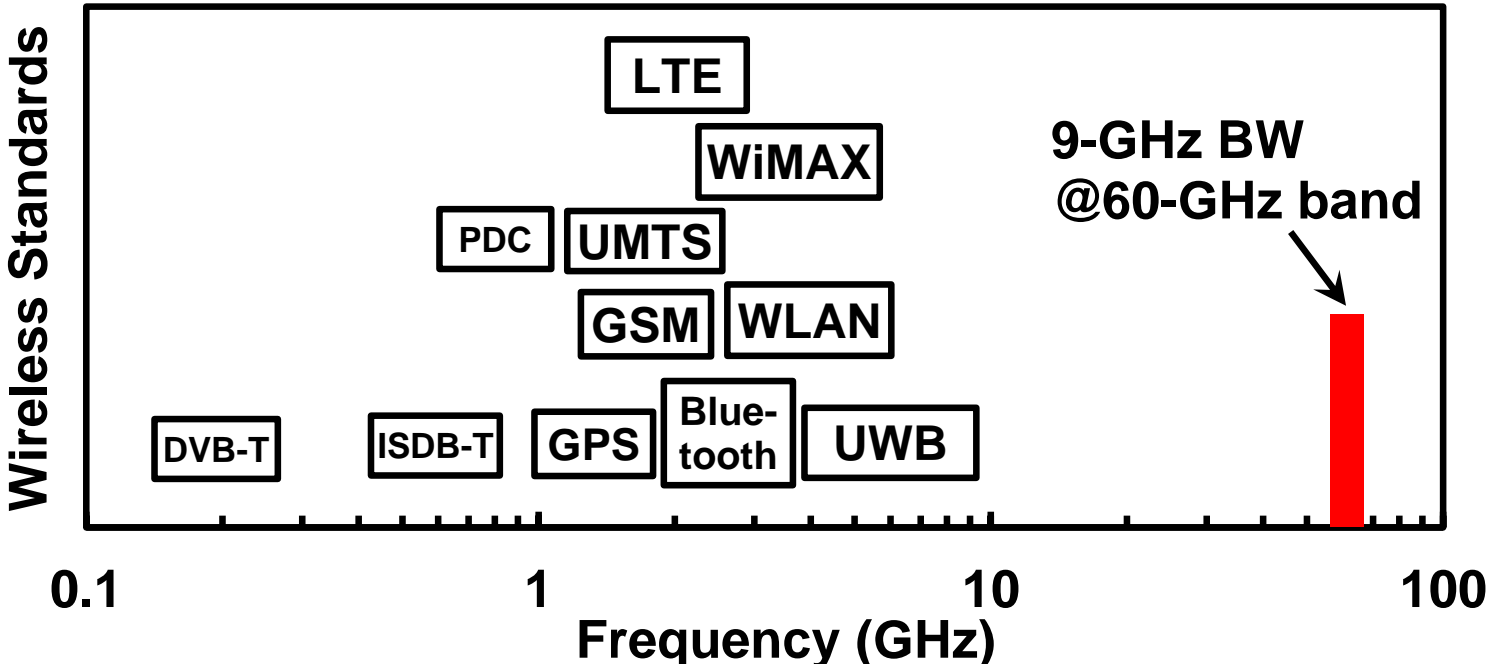
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Outline

- **Motivation**
- **Hot-Carrier-Injection Issues,
Prior Arts and Proposed Solution**
- **Proposed HCI-Healing 60GHz TRX**
 - **Detailed circuit implementation**
- **Measurement and Comparison**
- **Conclusion**

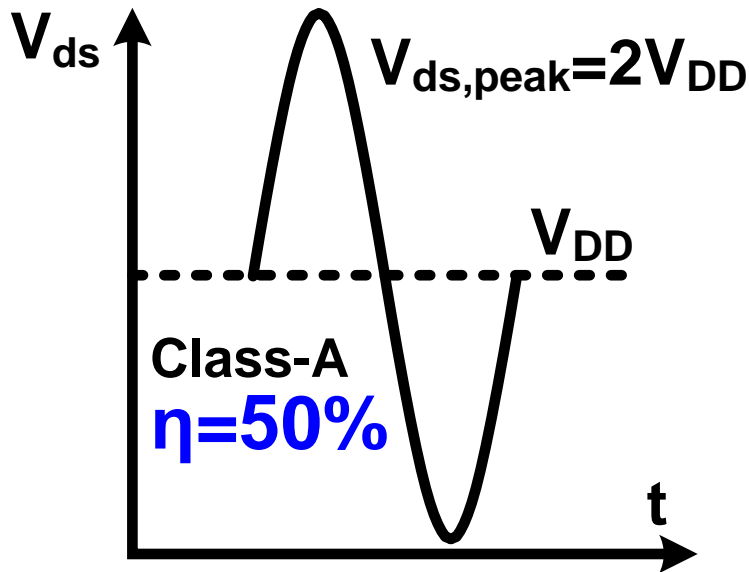
60GHz-Band Capability



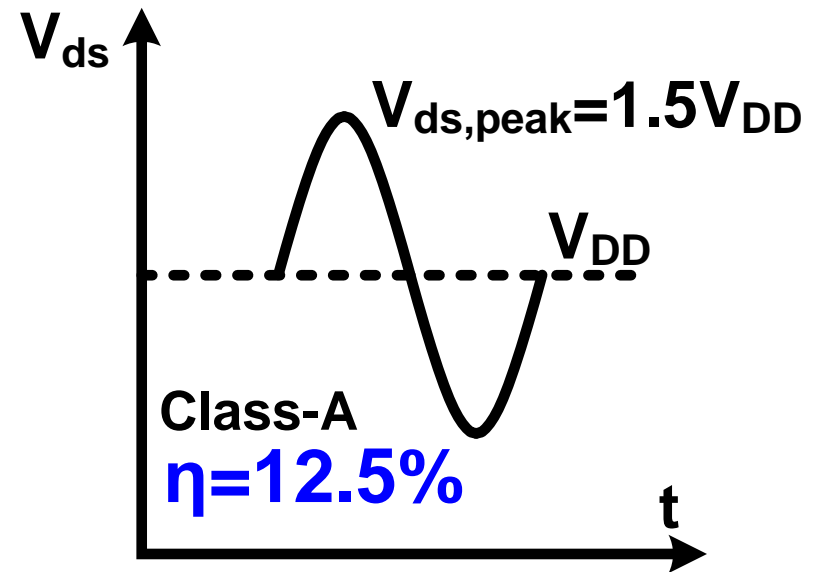
Hot-Carrier-Injection Issue in CMOS (1/2)

CMOS power amplifier

Drain efficiency: $\eta = P_{\text{out}}/P_{\text{DC}}$

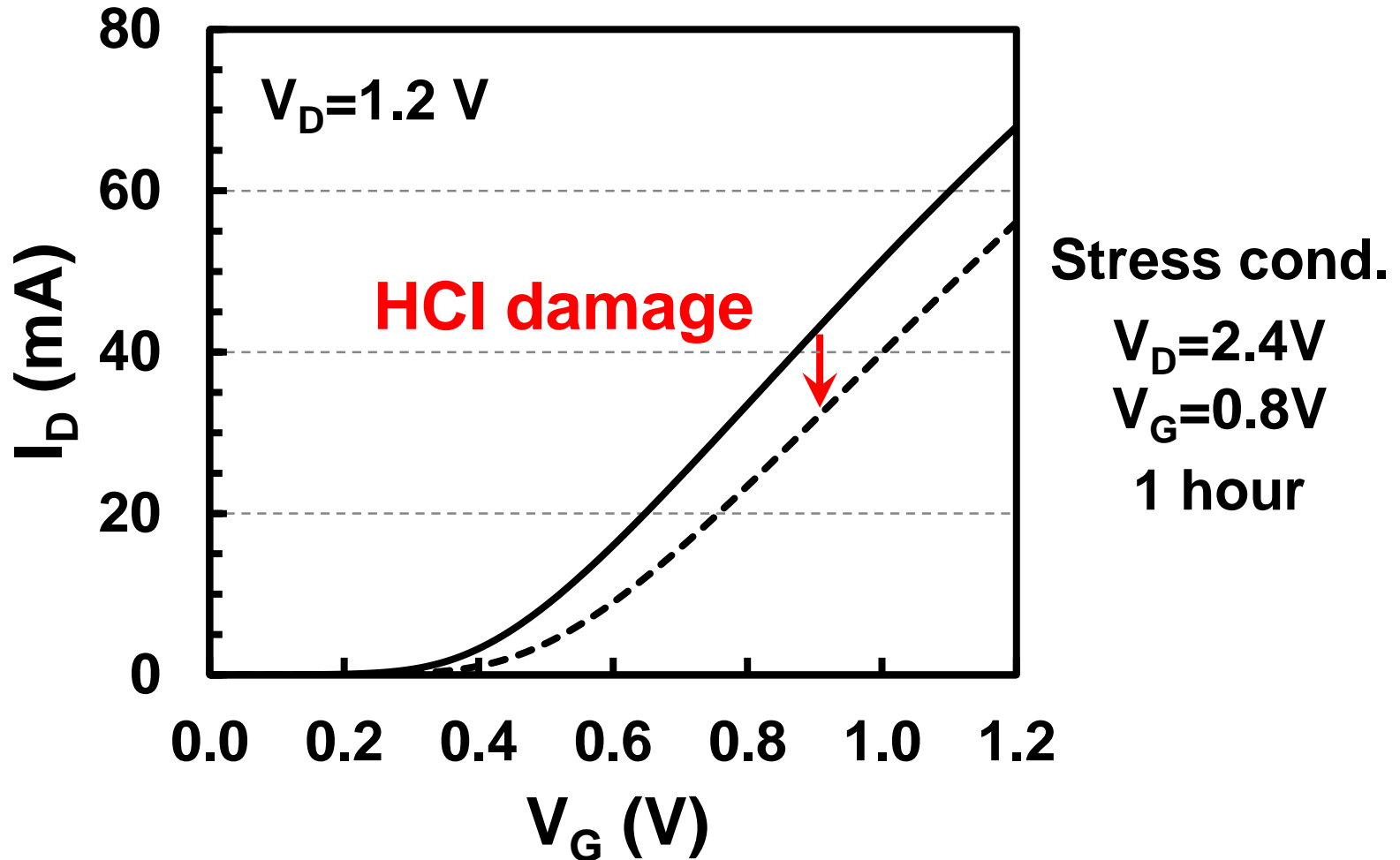


Large $V_{ds,peak}$
HCI damage



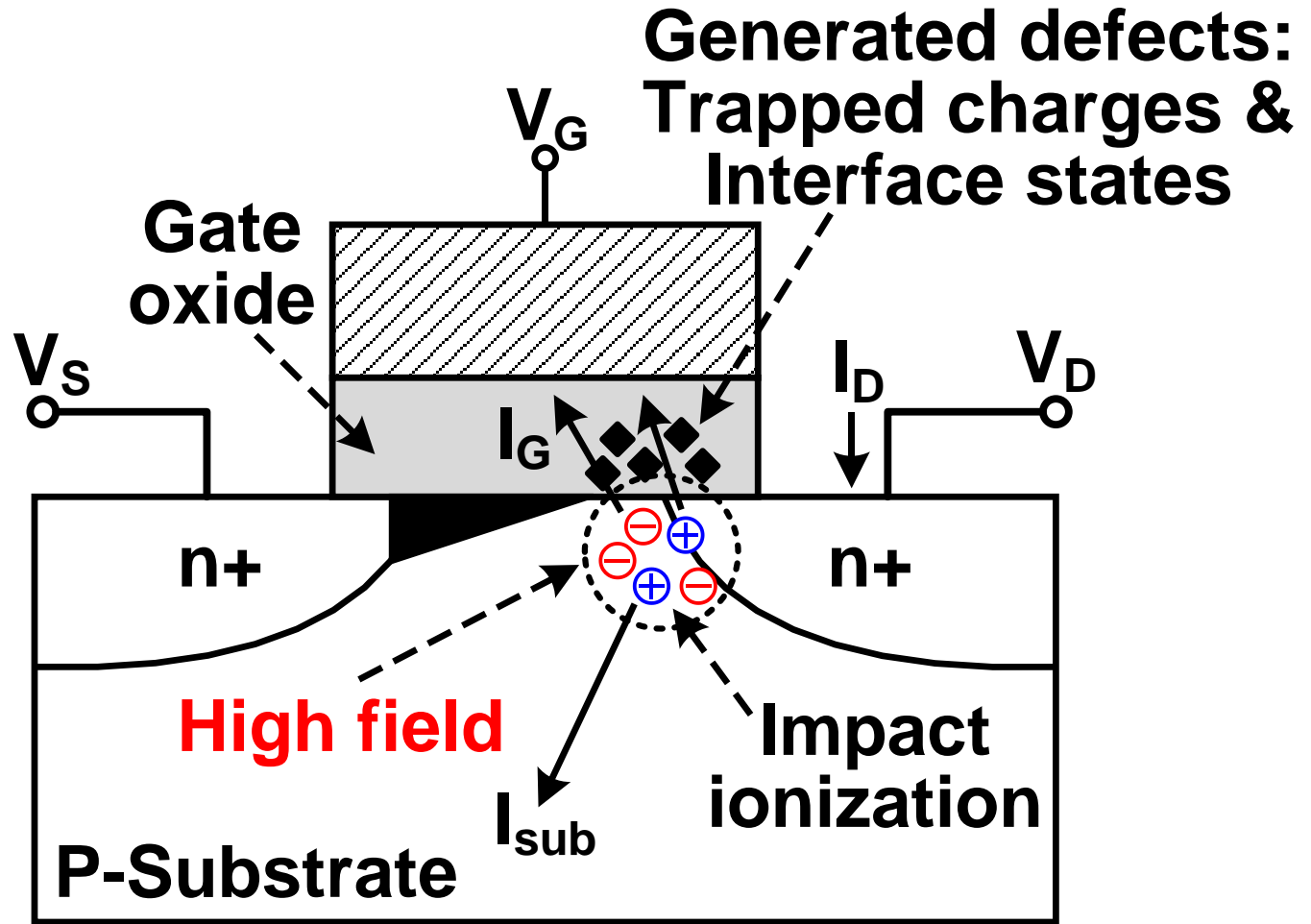
Small $V_{ds,peak}$
Low efficiency

Hot-Carrier-Injection Issue in CMOS (2/2)



Lifetime: the time when $\Delta I_{DS} = 10\%$ @ saturation

Hot-Carrier-Injection Mechanism

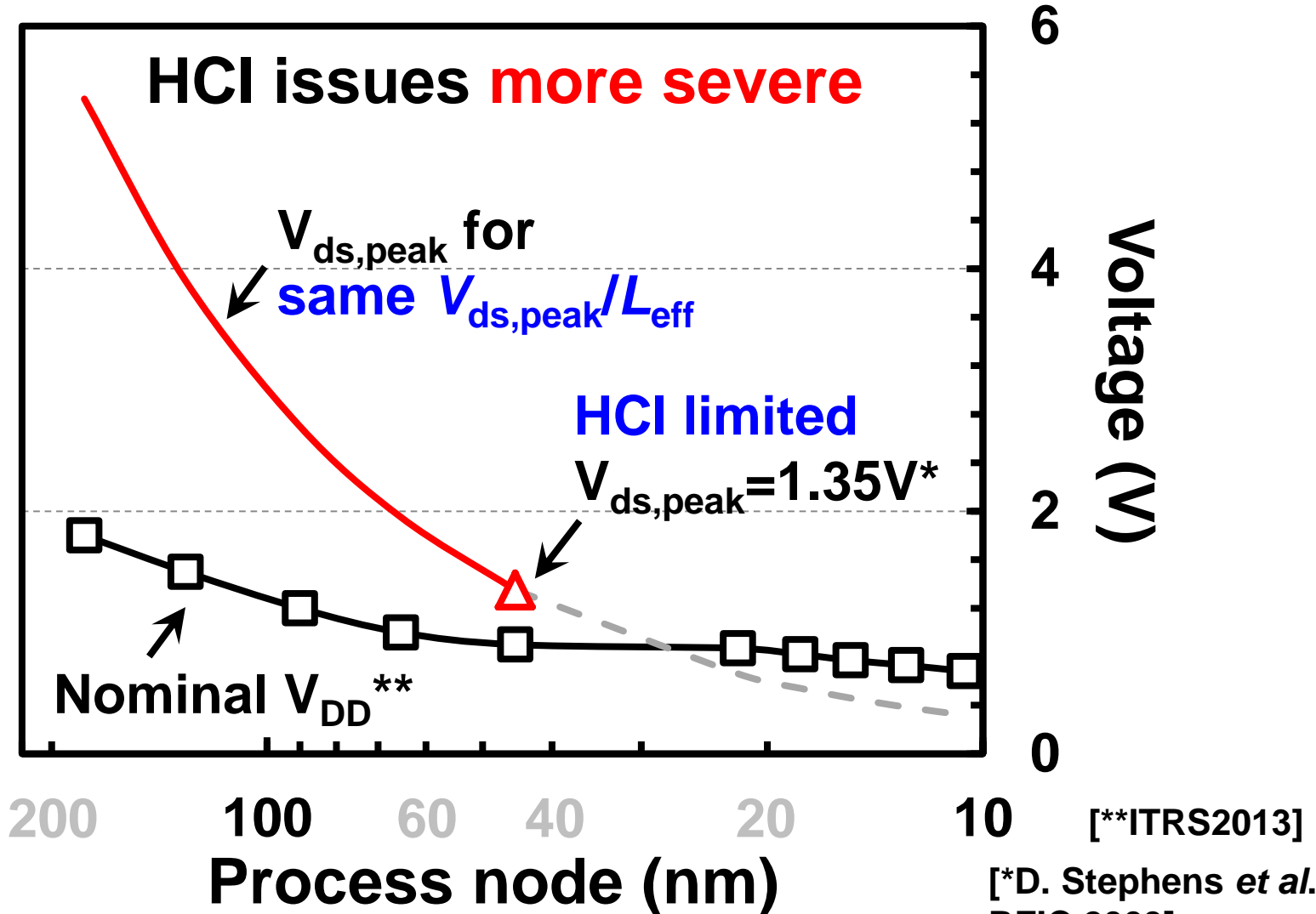


[*Y. Leblebici *et al.*,
JSSC 1993]

Degrade V_t , μ_n , g_m , I_D , and lifetime

HCI Issue in Advanced CMOS

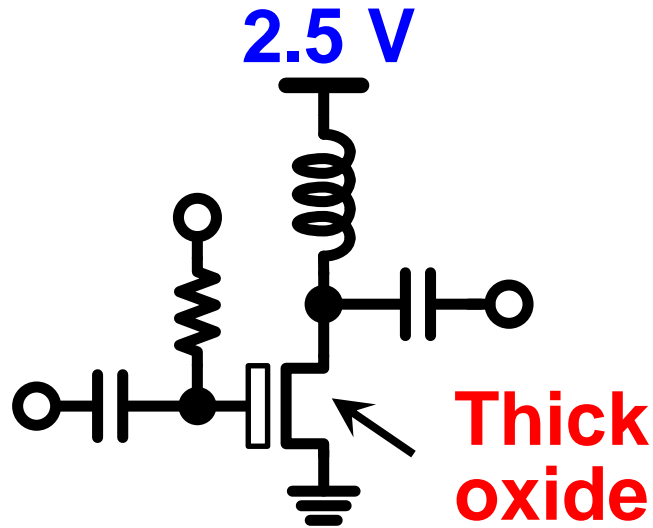
$$\text{HCI aging} \propto E_{\text{lateral}} \propto V_{\text{ds}}/L_{\text{eff}}$$



[*D. Stephens *et al.*,
RFIC 2009]

HCI Issues for 60-GHz Applications

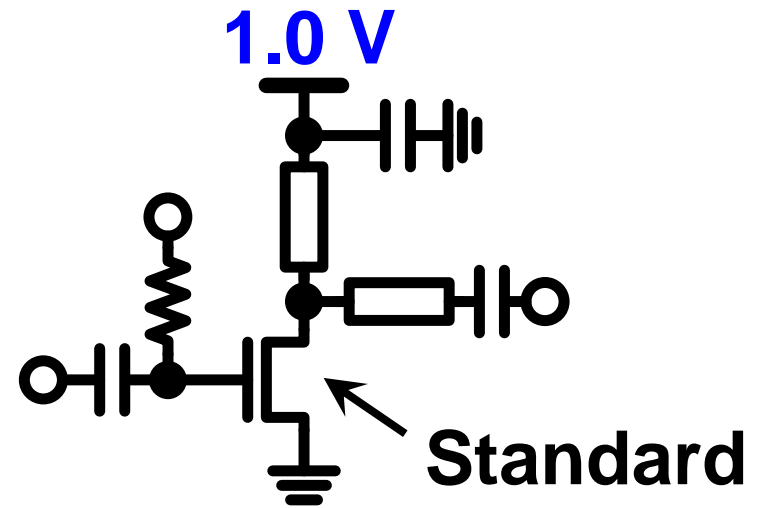
2.4-GHz power amplifier



$L=250$ nm (I/O Tr.)

$f_{\max}=40$ GHz

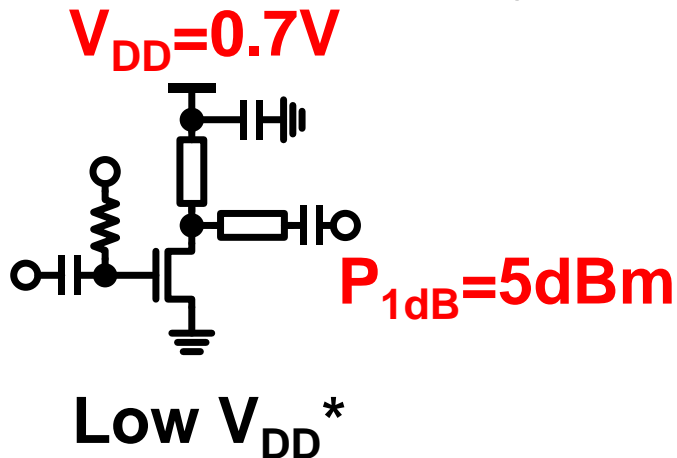
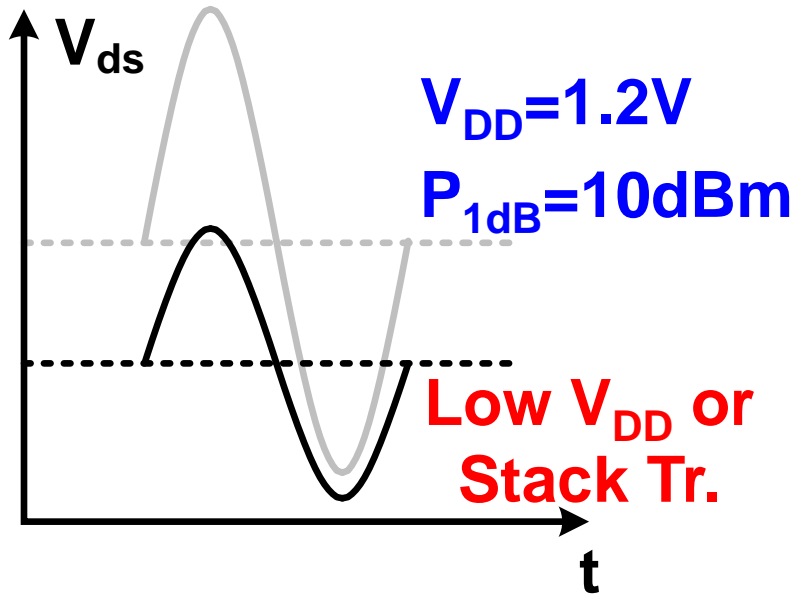
60-GHz power amplifier



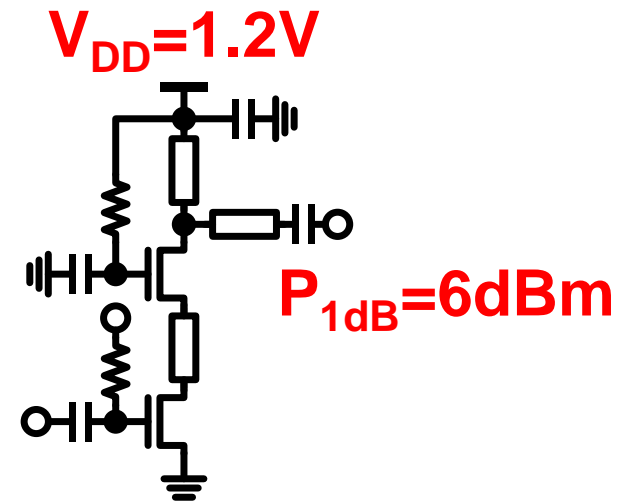
$L=65$ nm (core Tr.)

$f_{\max}=220$ GHz

Summary of Prior HCl Solutions @60GHz



- ☺ Better lifetime
- ☹ Degraded output power, linearity and efficiency

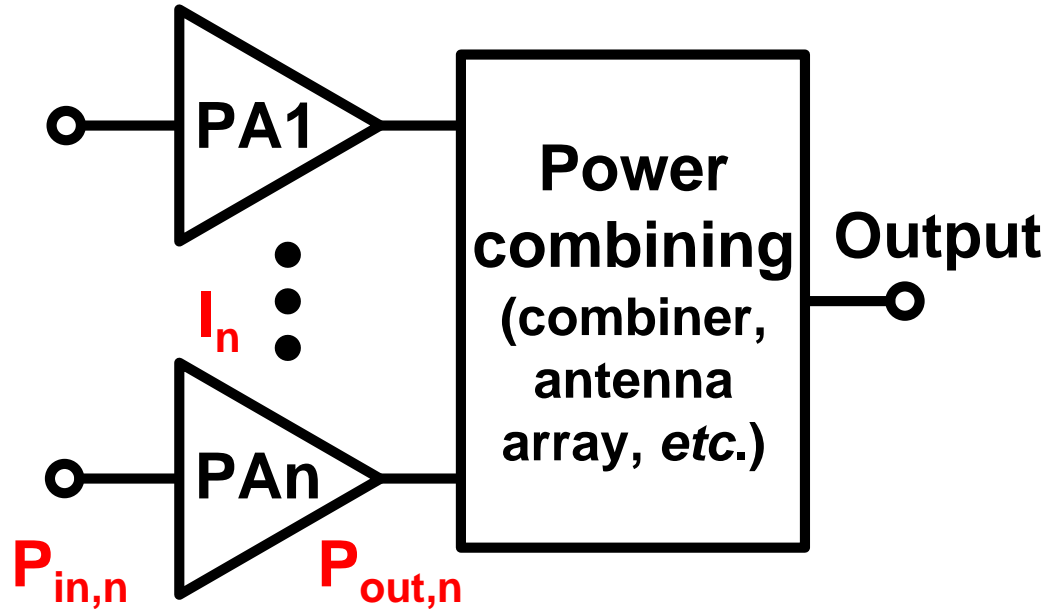


Stack Transistor**

[*M. Tanomura *et al.*, ISSCC 2008]

[**A. Siligaris *et al.*, JSSC 2010]

Power Combining Techniques

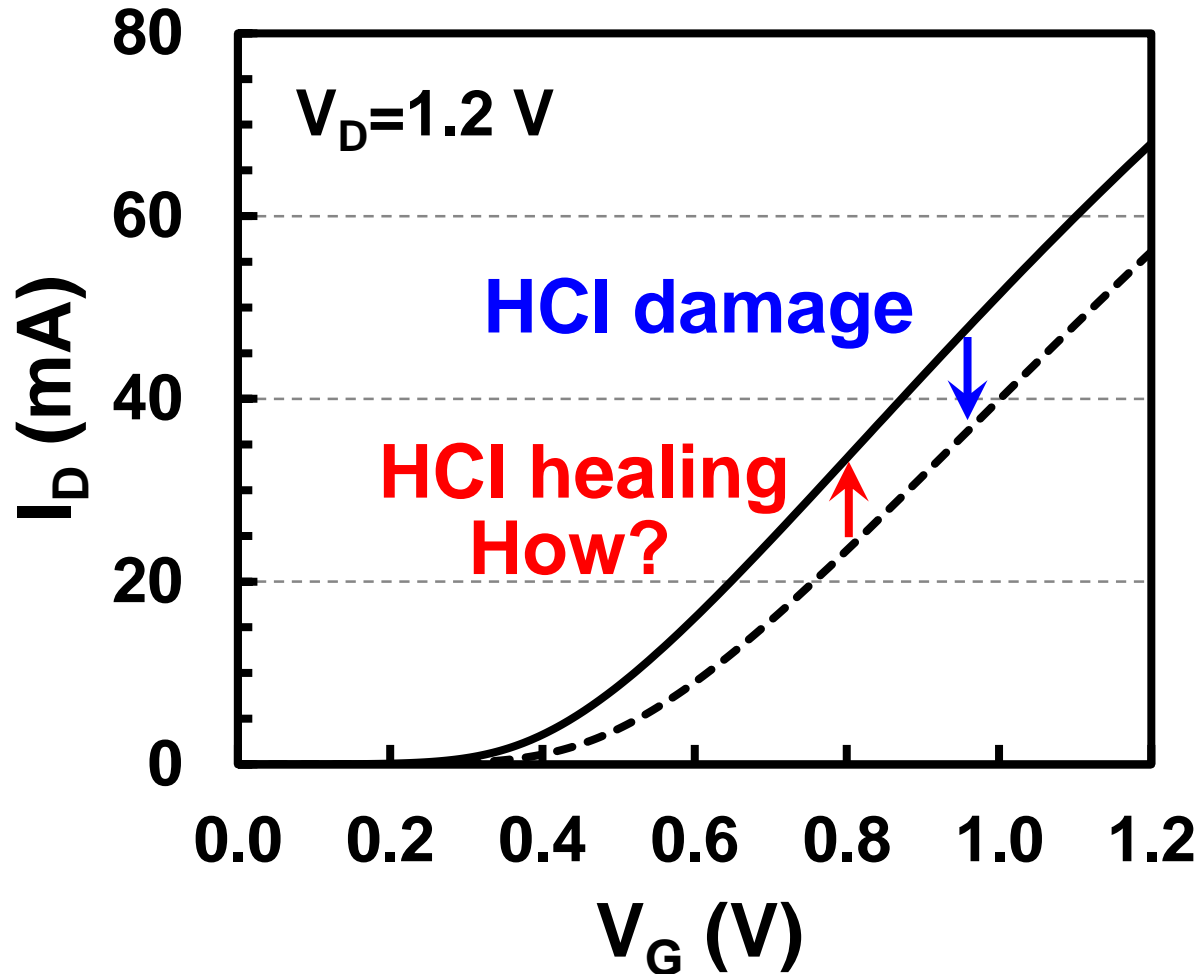


[*J. Chen *et al.*,
ISSCC 2011]

$$\text{Individual: PAE} = \frac{P_{out,n} - P_{in,n}}{I_n V_{DD}} \approx \text{Combined: PAE} = \frac{n \times (P_{out,n} - P_{in,n})}{n \times I_n V_{DD}}$$

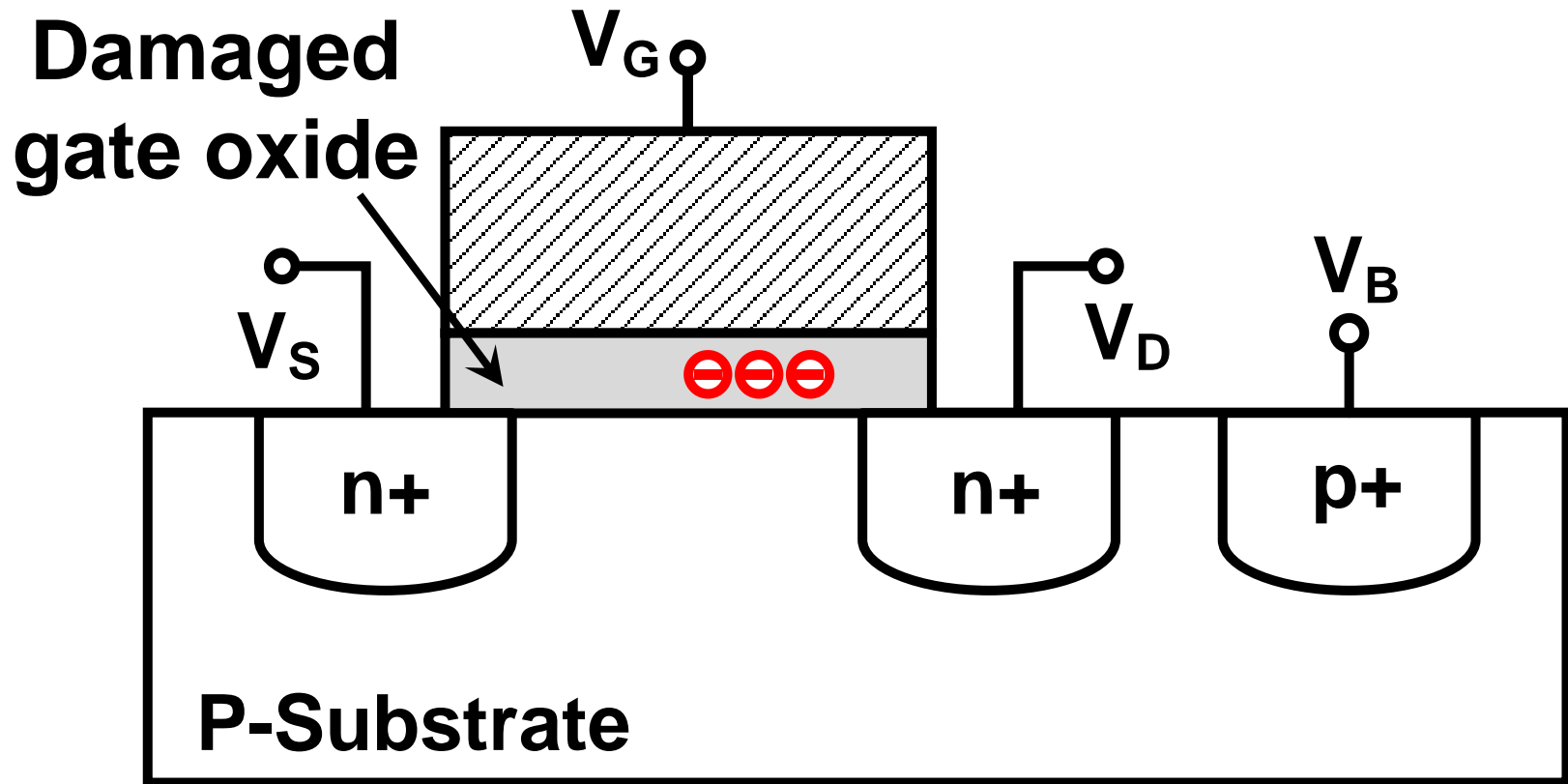
- ☺ Compensate output power and linearity
- ☹ Deteriorated efficiency can not be improved

Proposed HCl-Healing Technique



Ultimate solution: Physically heal HCl damage

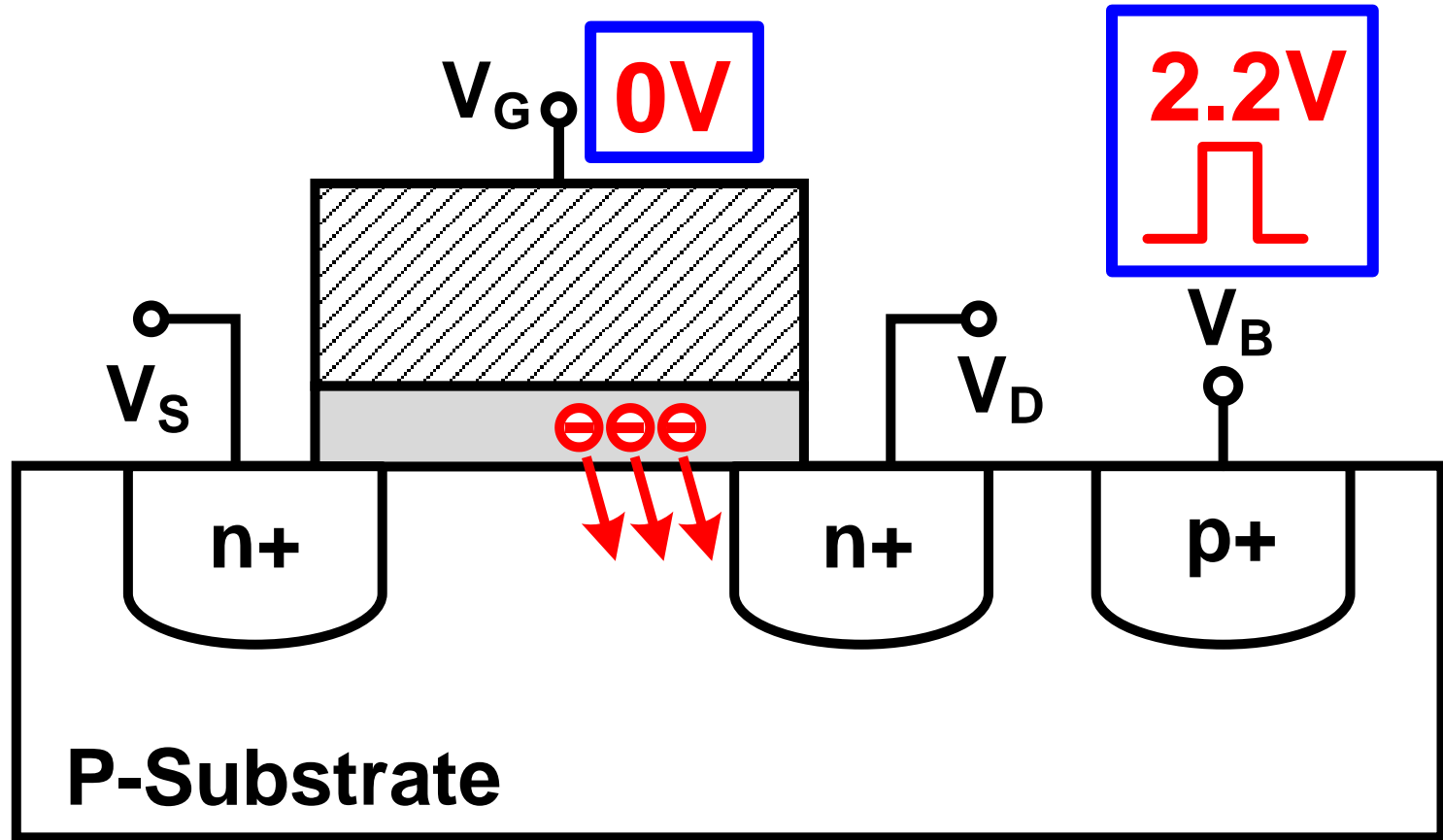
Proposed HCl Healing Mechanism (1/2)



Damage mechanism: **trapped electrons**

[Y. Leblebici *et al.*, JSSC 1993]

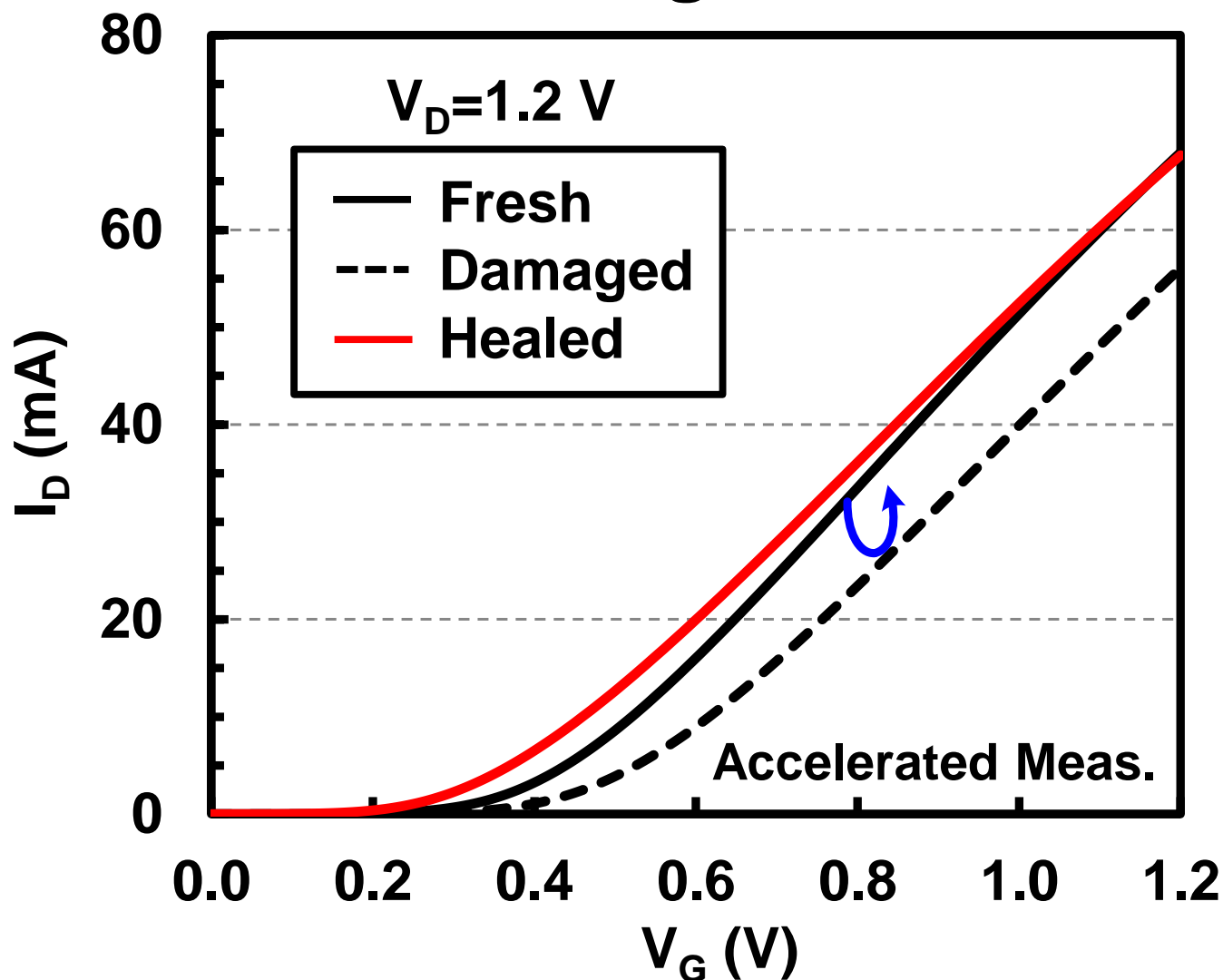
Proposed HCl Healing Mechanism (2/2)



Possible solution: **charge ejection**

Measured HCl-Healing I_D - V_G Curves

First HCl healing demonstration



Stress cond.

$V_D = 2.4$ V

$V_G = 0.8$ V

1 hour

Heal cond.

$V_B = 2.2$ V

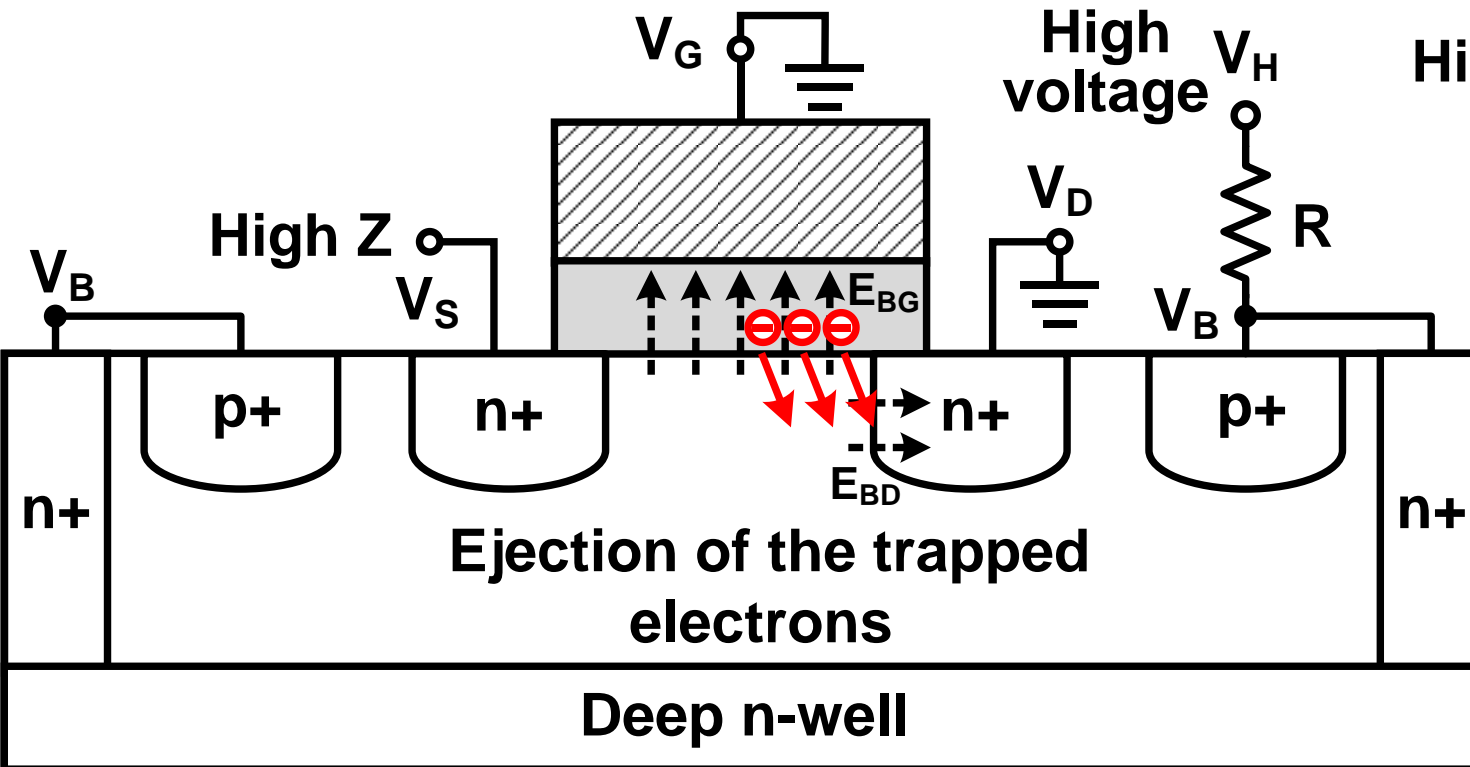
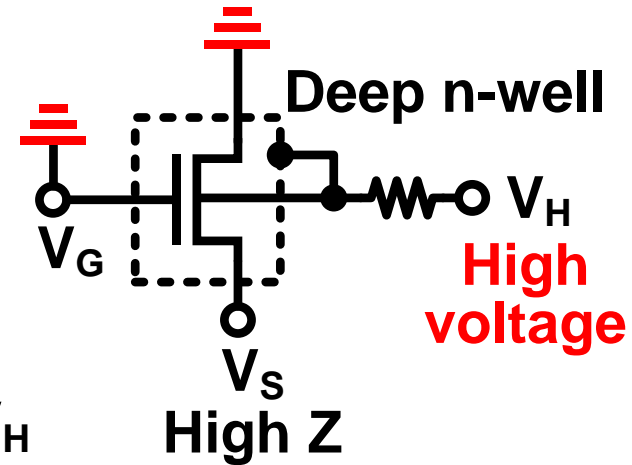
$V_G = V_D = 0$ V

1 second

HCI-Healing Function in Transistor

First HCI healing transistor

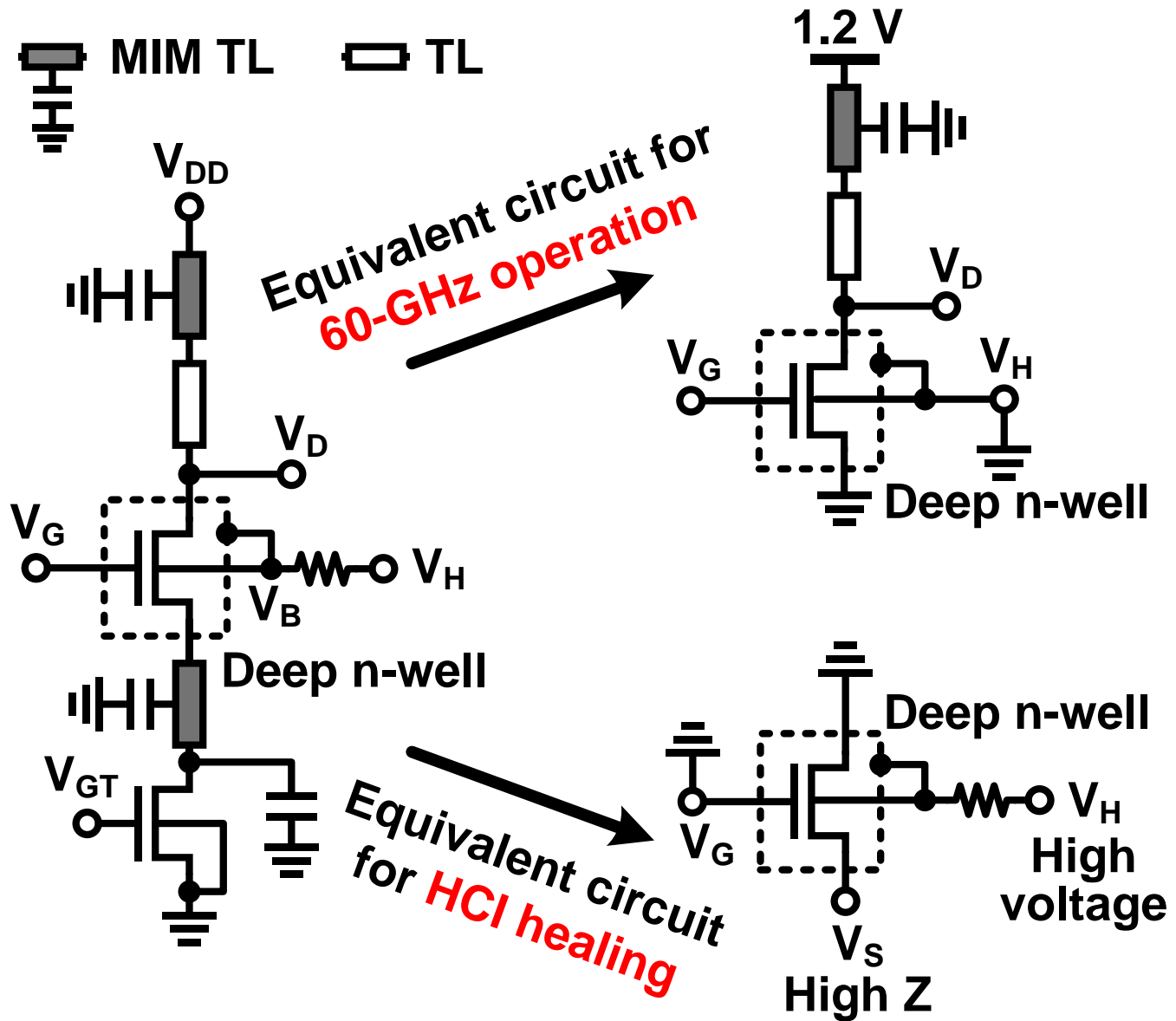
Floating source* & low drain bias** assisting ejection (memory cells)



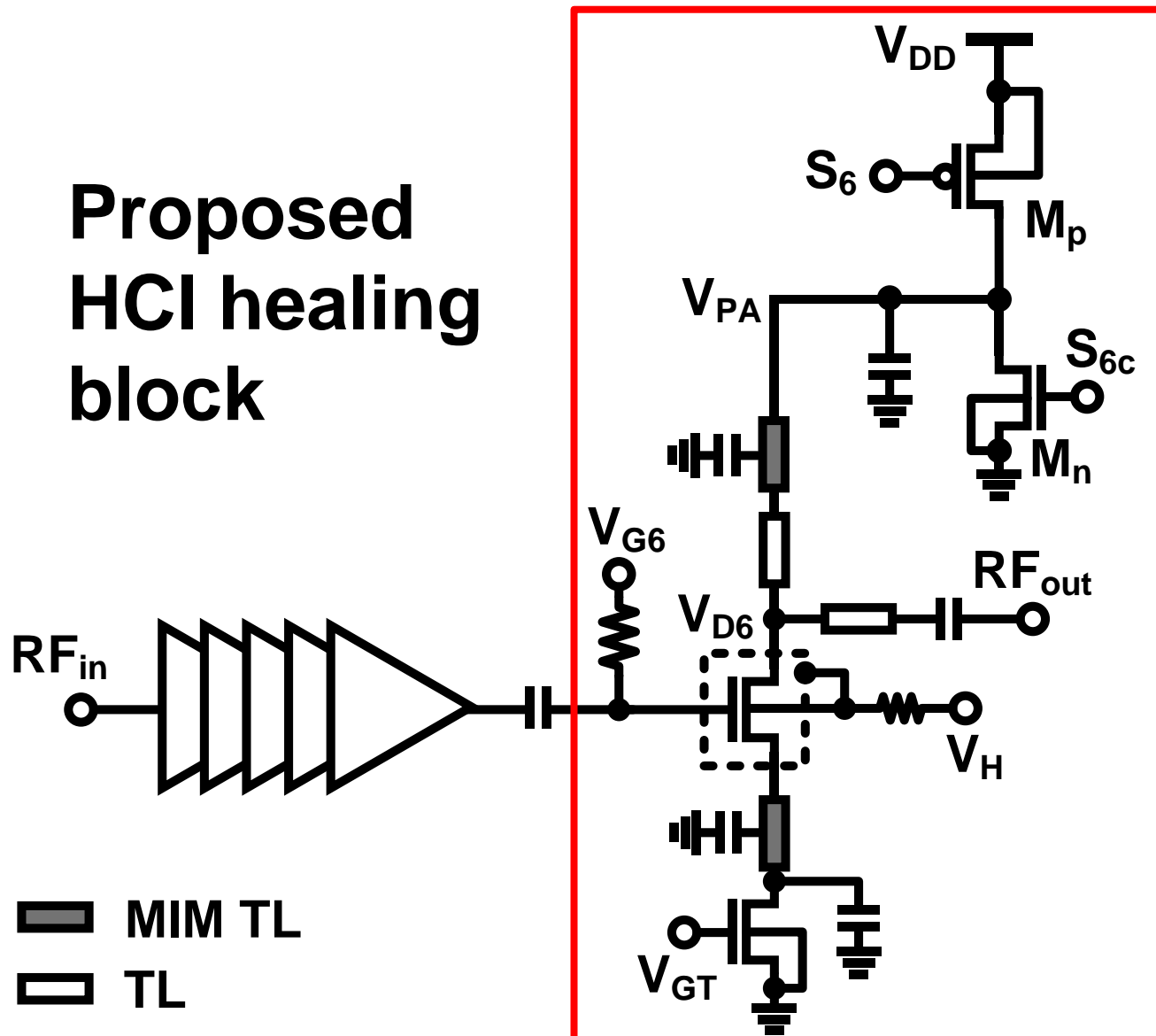
[*T. Endoh *et al.*, IEDM 1989]

[**K. Miyaji *et al.*, JJAP 2012]

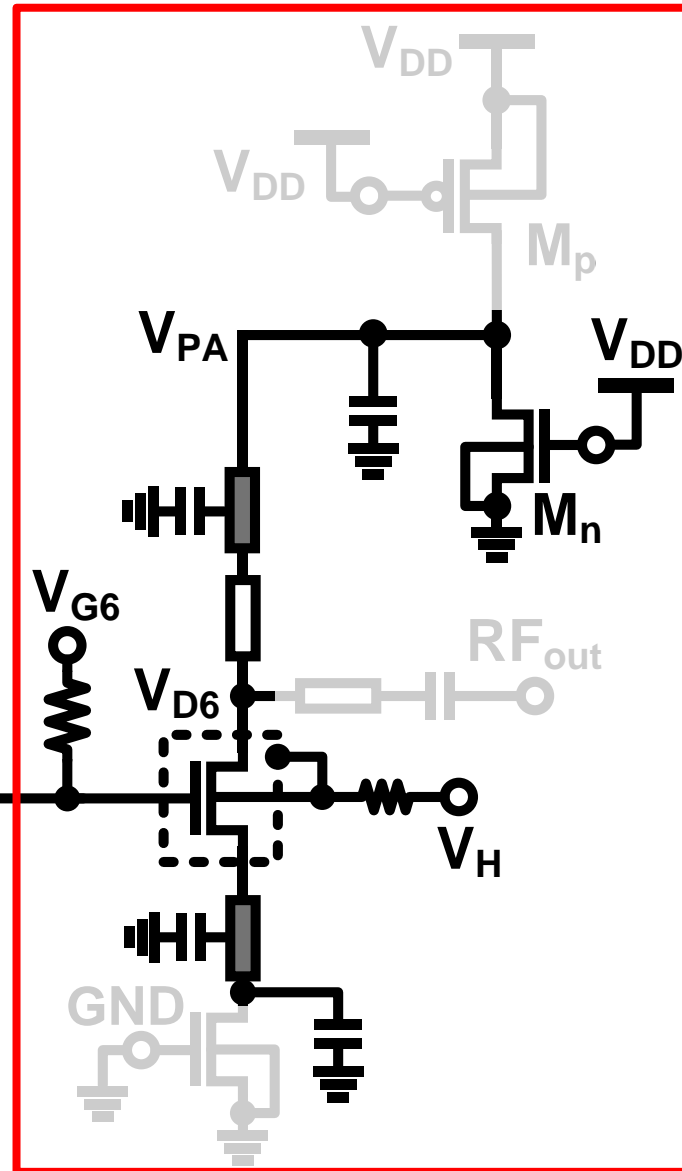
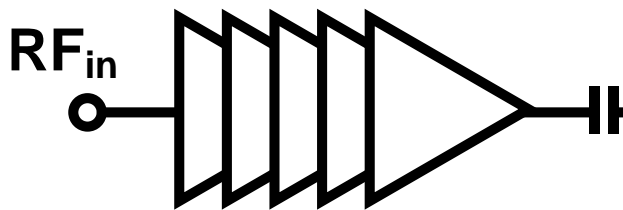
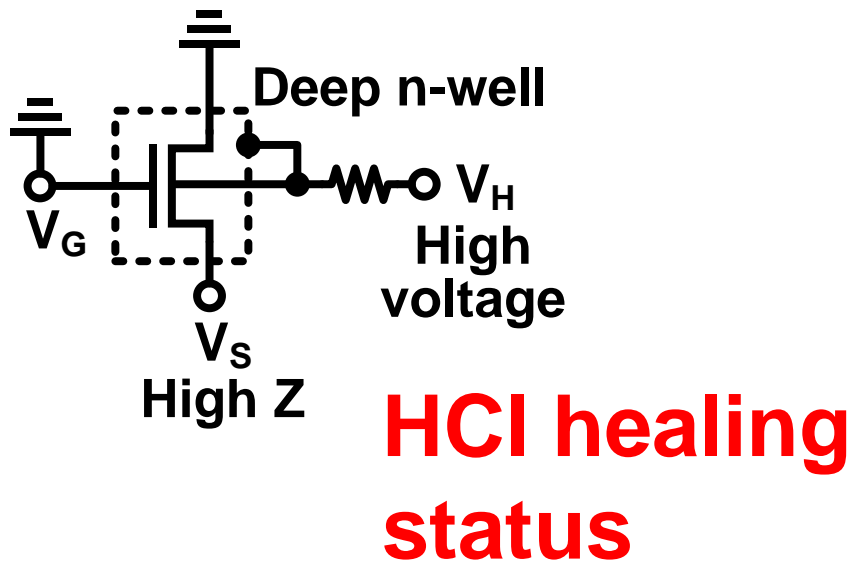
HCI-Healing Transistor Module



HCI-Healing Power Amplifier (1/3)

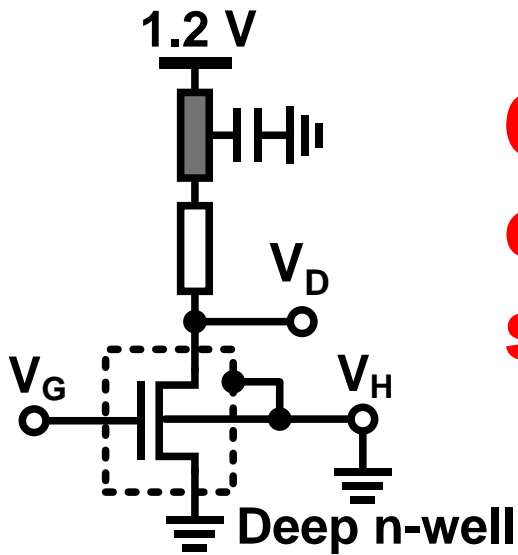


HCI-Healing Power Amplifier (2/3)



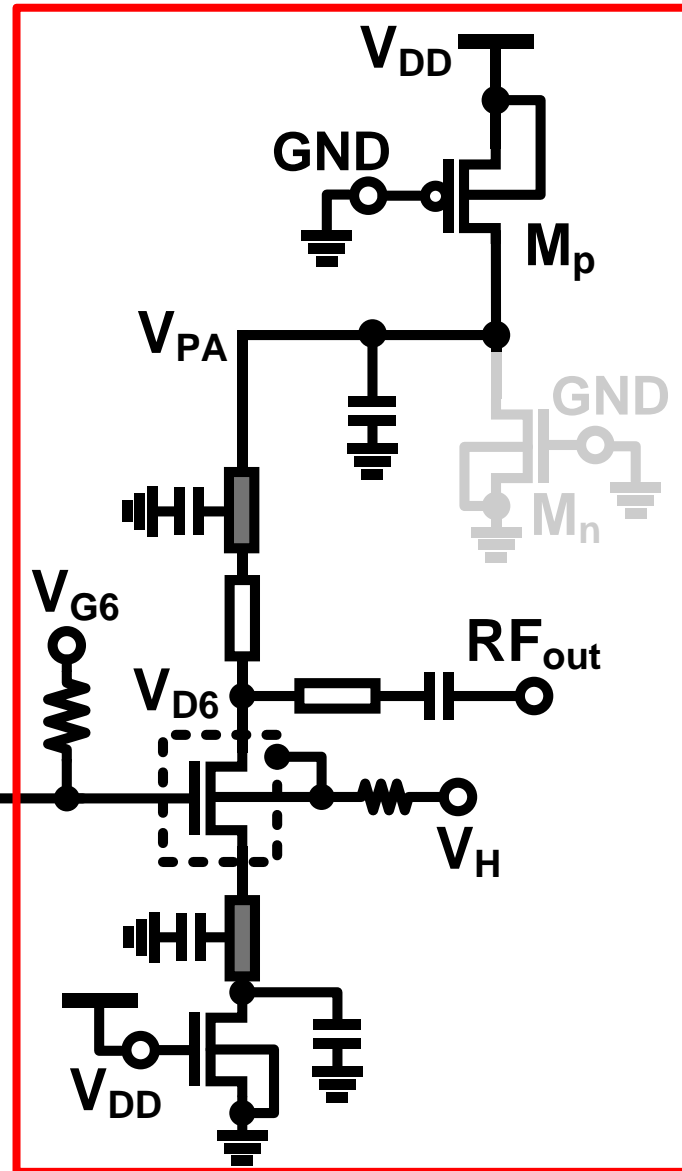
HCI-Healing Power Amplifier (3/3)

**60GHz
operation
status**



RF_{in}

■ MIM TL
 □ TL

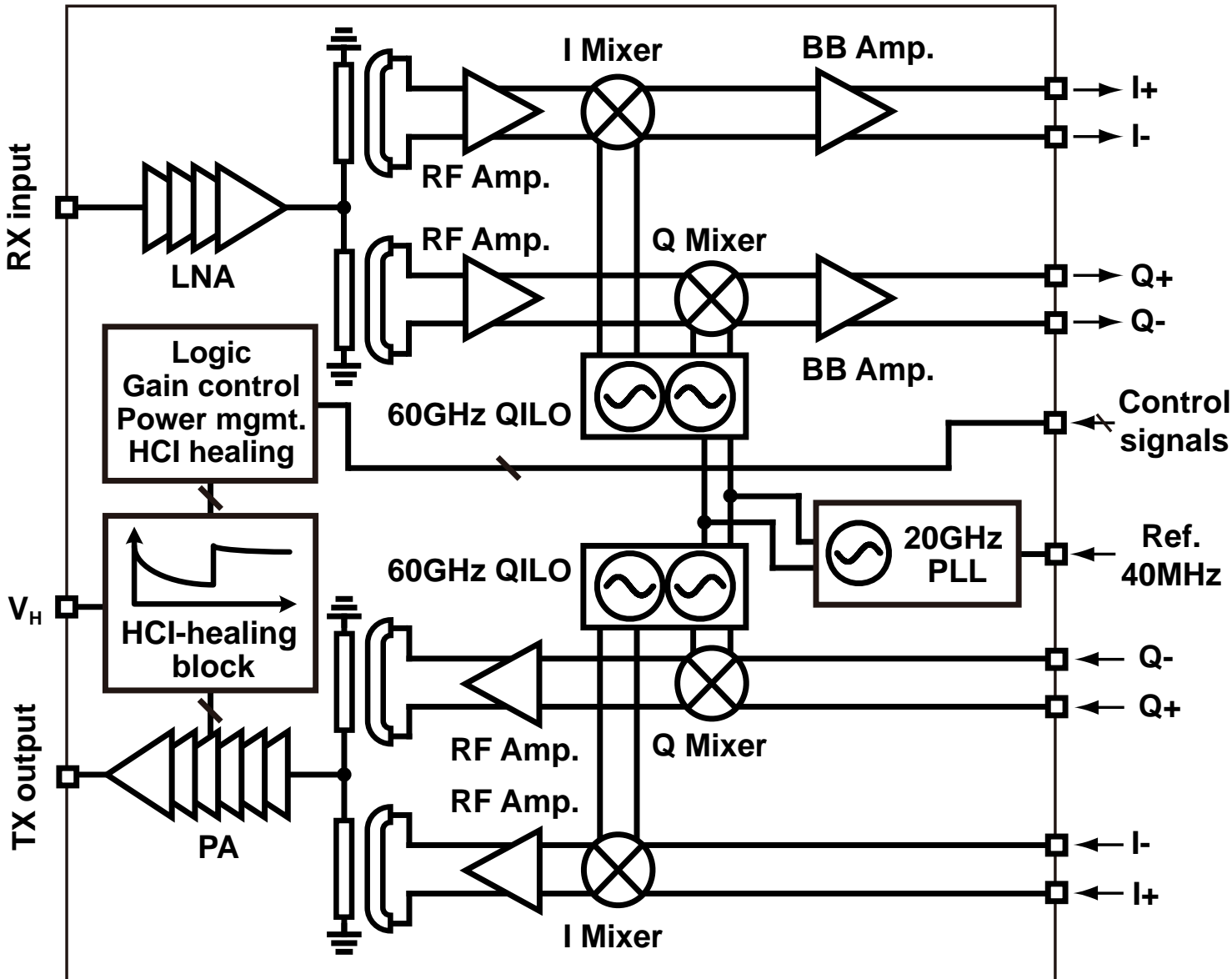


HCI-Healing TRX Block Diagram

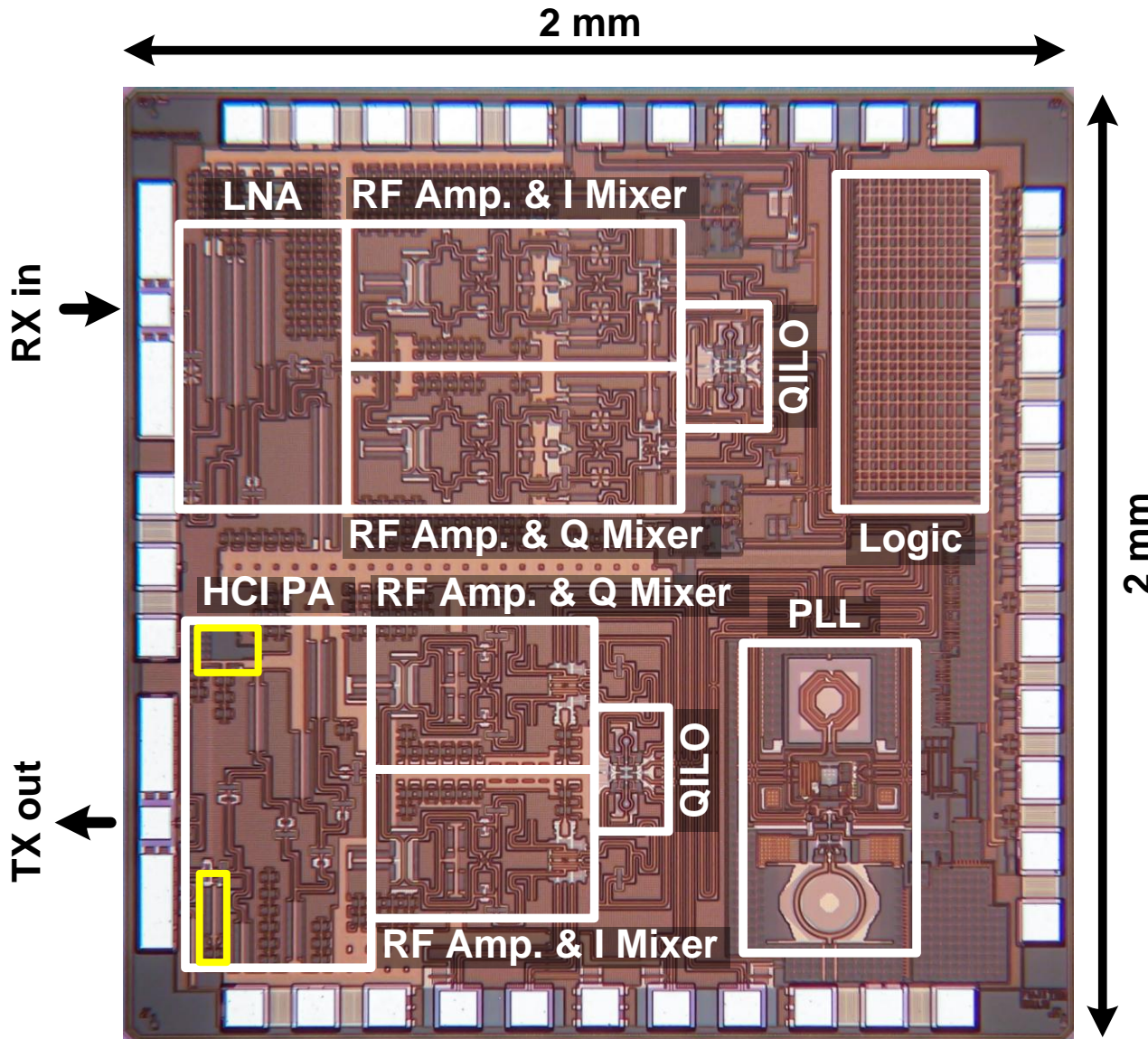
Direct Conversion

**20GHz PLL+
60GHz QILO**

**Integrated
HCI-healing
function**



Die Micrograph



**Standard
65 nm CMOS**

Block	Area (mm ²)
TX	0.79
RX	1.01
PLL	0.27
Logic	0.21

2 mm

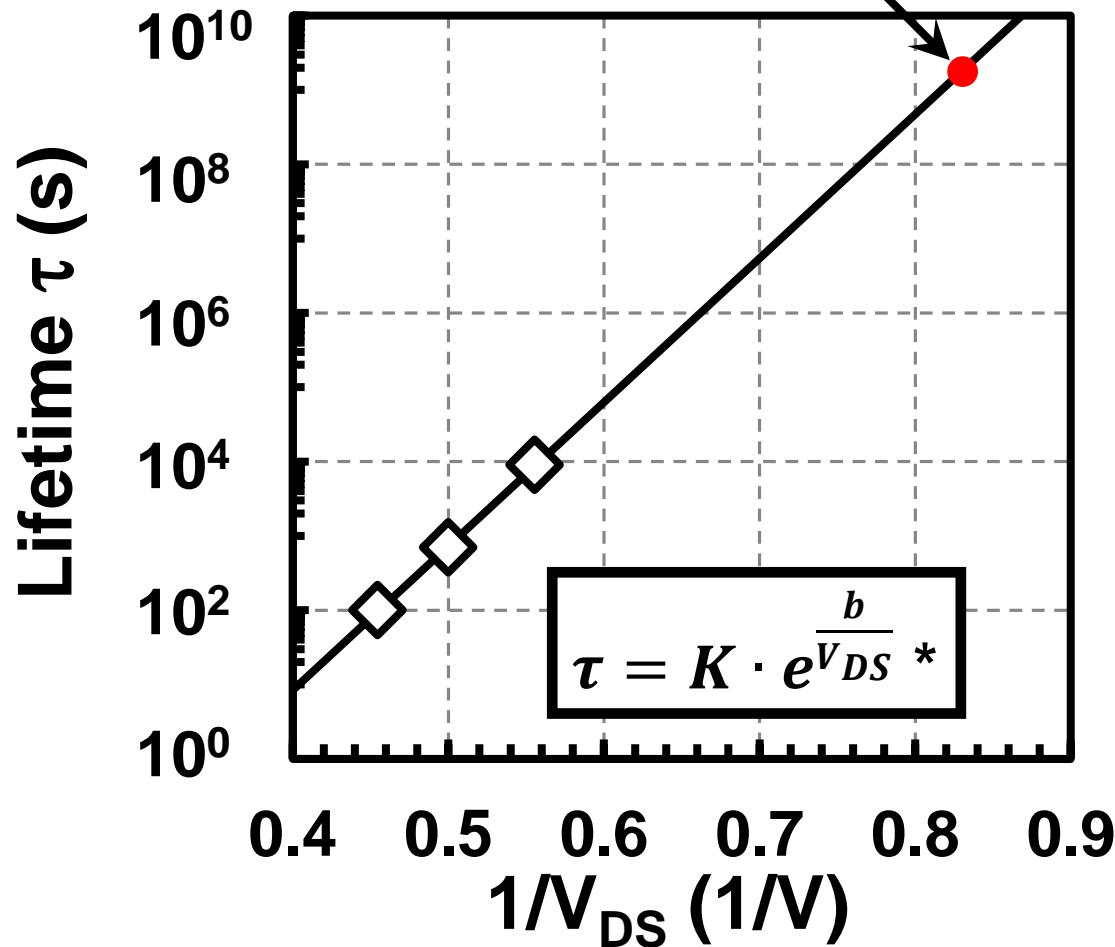
Measurements

- **Transistor TEG**
 - DC stress lifetime
 - AC stress lifetime
- **Stand-alone PA TEG**
 - P_{in} - P_{out} with healing
 - AC stress lifetime with healing
- **TRX Board**
 - EVM versus P_{out} with healing

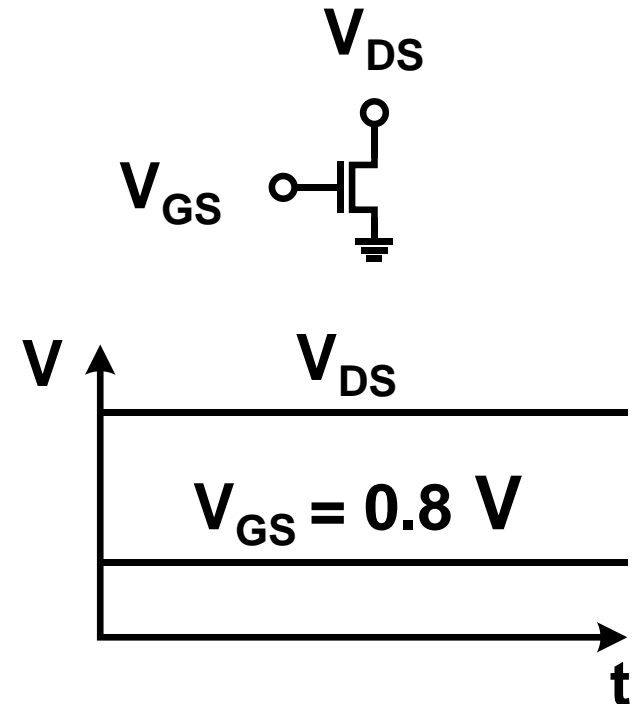
65 nm NMOSFET DC Stress Lifetime

Lifetime = **63 years**

@ $V_{DS}=1.2V$



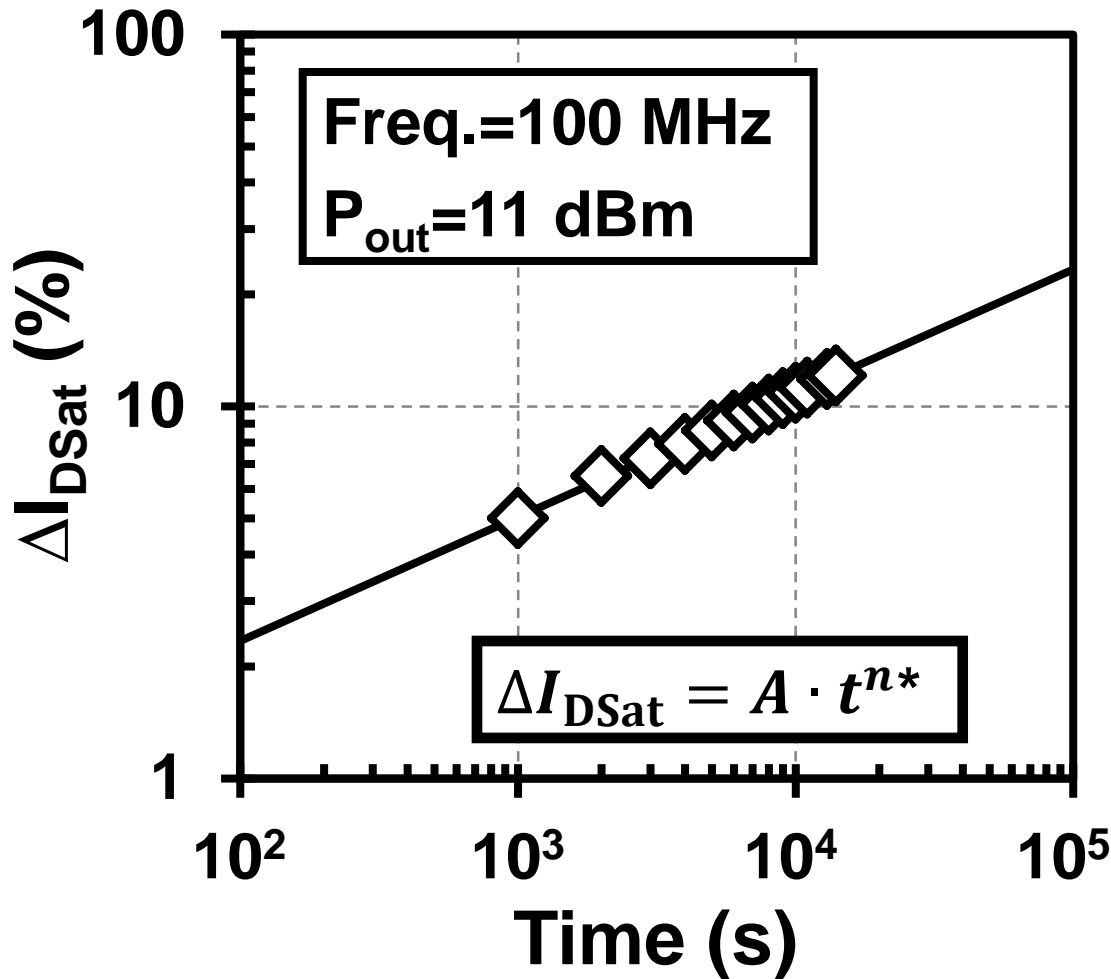
Stress condition



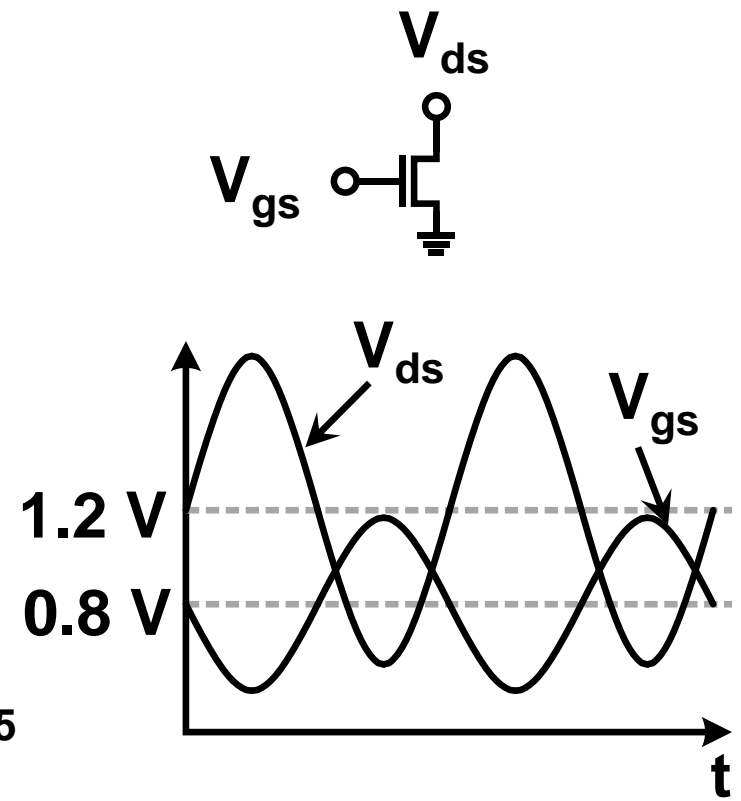
[*E. Takeda *et al.*, EDL 1983]

65 nm NMOSFET RF Stress Lifetime

Lifetime = **2 hours**

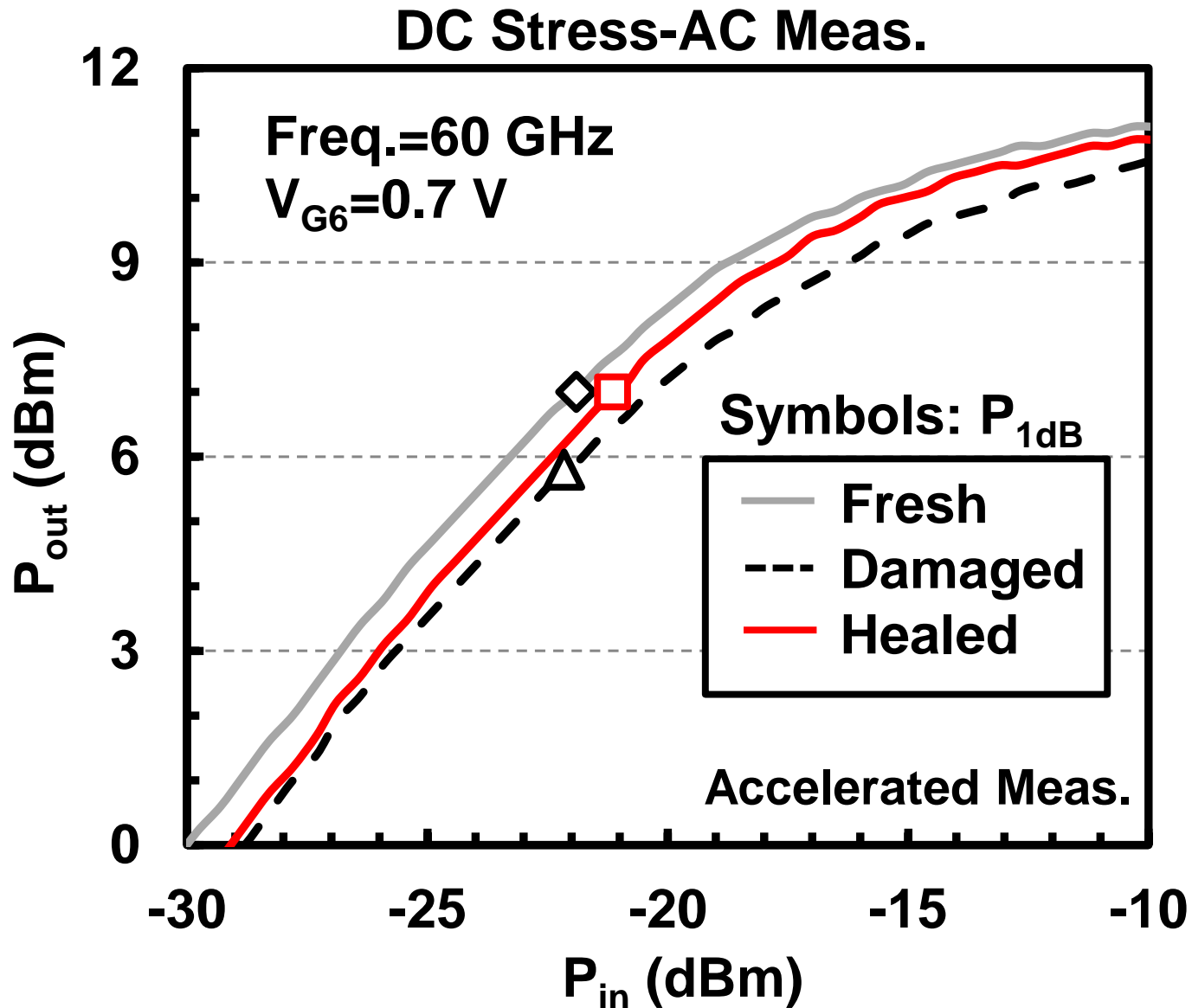


Stress condition

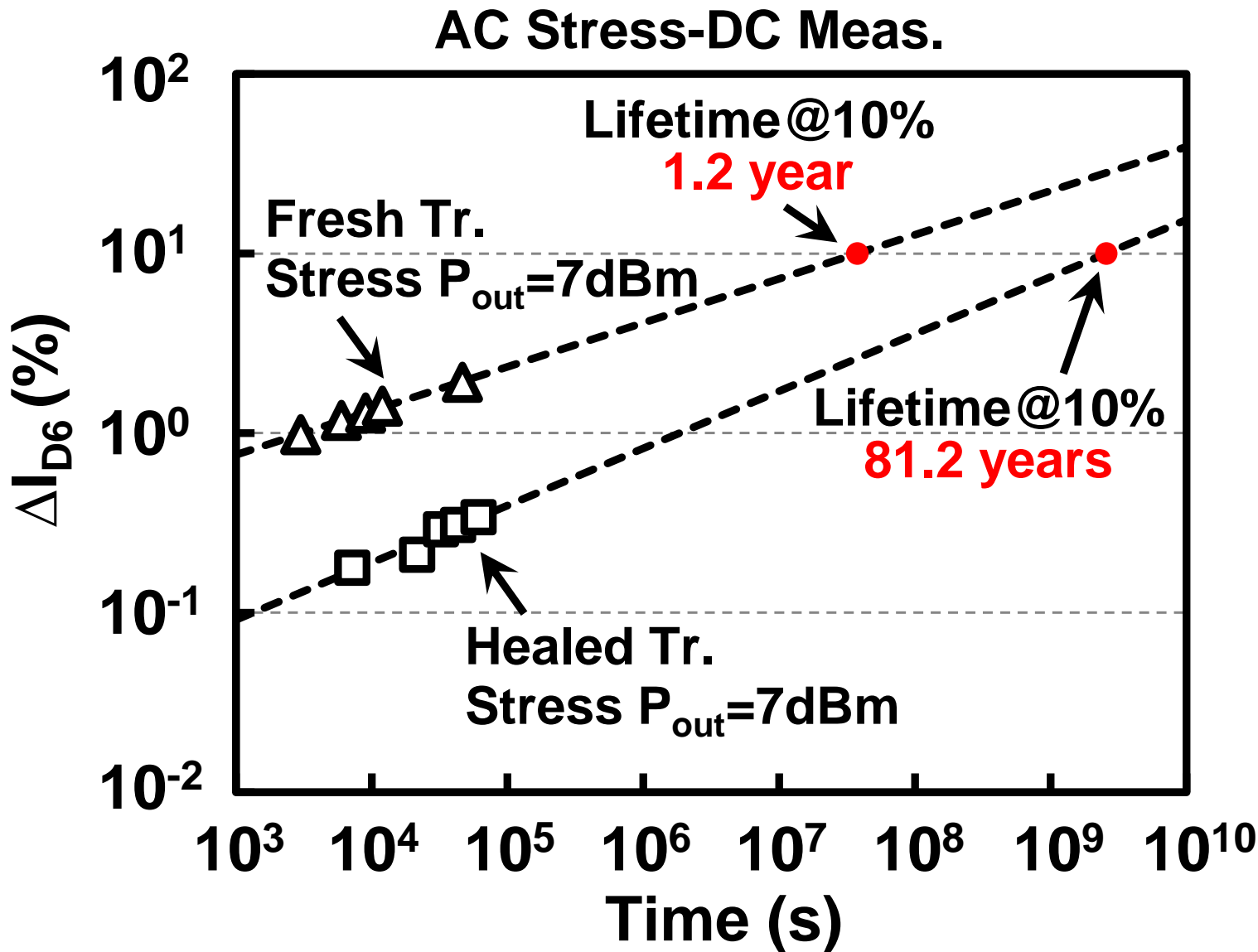


[*L. Negre *et al.*, JSSC 2012]

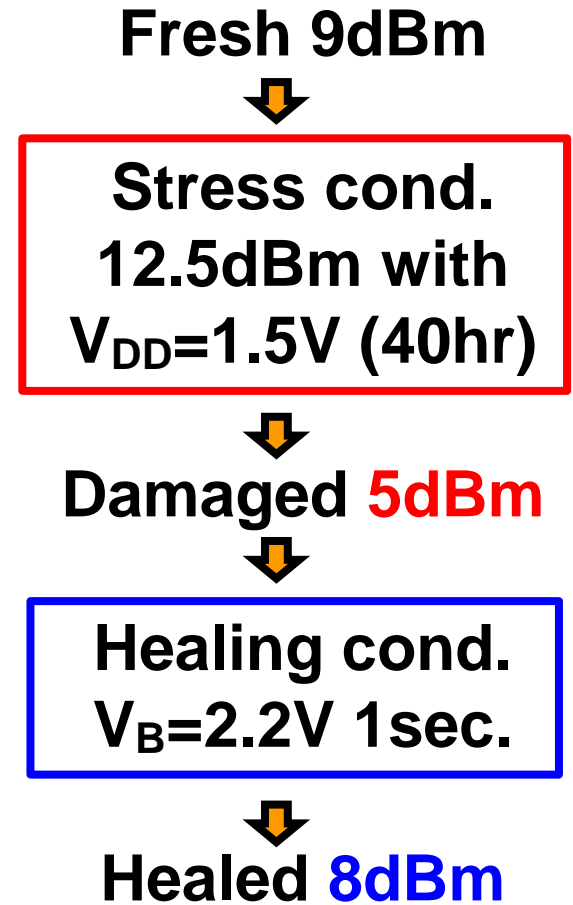
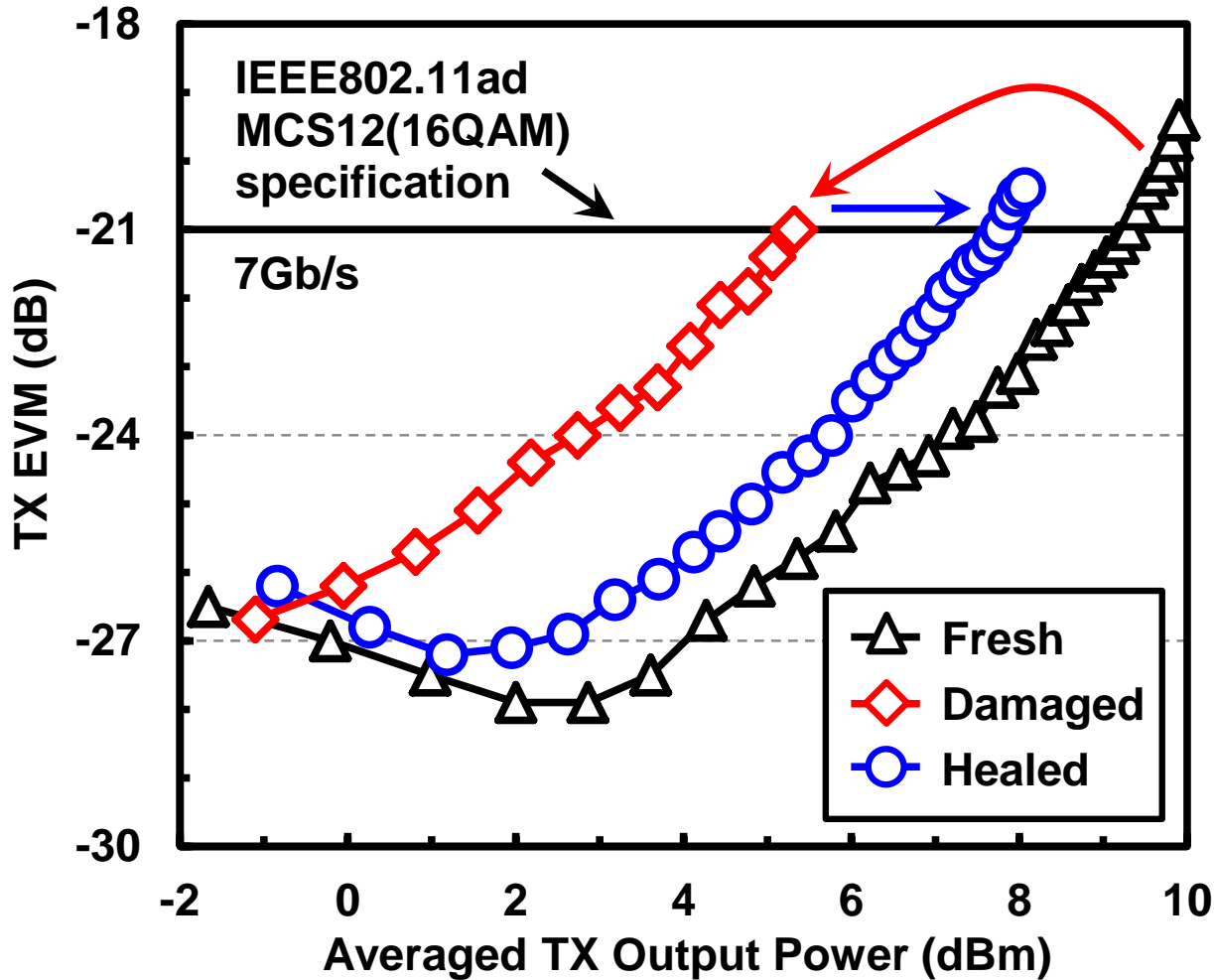
Measured P_{in} - P_{out} of the PA



Measured Lifetime of the PA



Measured TX EVM versus P_{out}



60GHz TRX Performance Comparison

Ref.	CMOS Process	Data rate (Modulation)	P_{out} /each PA (dBm)	TX efficiency P_{out}/P_{DC} (%)	HCI healing	Core area (mm ²)	Power Consumption
Tokyo Tech [1]	65nm	10.56Gb/s (64QAM) 28.16Gb/s (16QAM)	8.5* @TX EVM = -21dB	2.8	NO	3.9	TX: 251mW RX: 220mW
NEC [2]	90nm	2.6Gb/s (QPSK)	6	3.0 w/o PLL	NO	3.4	TX: 133mW RX: 206mW w/o PLL
Panasonic [3]	90nm	2.5Gb/s (QPSK)	1.9 @TX EVM = -19.6dB	0.4	NO	5.7	TX: 361mW RX: 260mW
Broadcom [4]	40nm	4.6Gb/s (16QAM)	-4* @TX EVM = -23dB	0.5	NO	26.3 [†]	TX: 1190mW RX: 960mW 16x16 array
This work	65nm	7Gb/s (16QAM)	9.3 @TX EVM = -21dB	3.9	YES	2.3	TX: 218mW RX: 188mW

*Estimated from literature †Chip area

Conclusions

- 60-GHz CMOS transceiver with **HCI damage healing** function by using charge ejection technique.
- 81-year lifetime **without sacrificing** the output power and efficiency
- The transceiver demonstrates an EVM of -27.9dB and can transmit 7Gb/s in 16QAM within 2.16GHz bandwidth.

Acknowledgement

This work is partially supported by MIC, SCOPE, MEXT, STARC, STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., Synopsys Inc., and Agilent Technologies Japan, Ltd.

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