A 2.2GHz -242dB-FOM 4.2mW ADC-PLL Using Digital Sub-Sampling Architecture

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Outline

- Motivation
- Phase Digitization
- ADC-Based Phase Detection
  - Digitized sub-sampling architecture
  - Resolution enhancement
- Circuit Implementation
  - 4-bit flash ADC
  - Push-pull class-C DCO
- Measurement Results
- Conclusion

Motivation

- PLL with low jitter and low power
- All-Digital PLL (AD-PLL)
  - TDC-based phase detection
  - Tradeoff in resolution and power consumption
- Applications
  - Wireless/Wireline transceivers
  - Digital clocks

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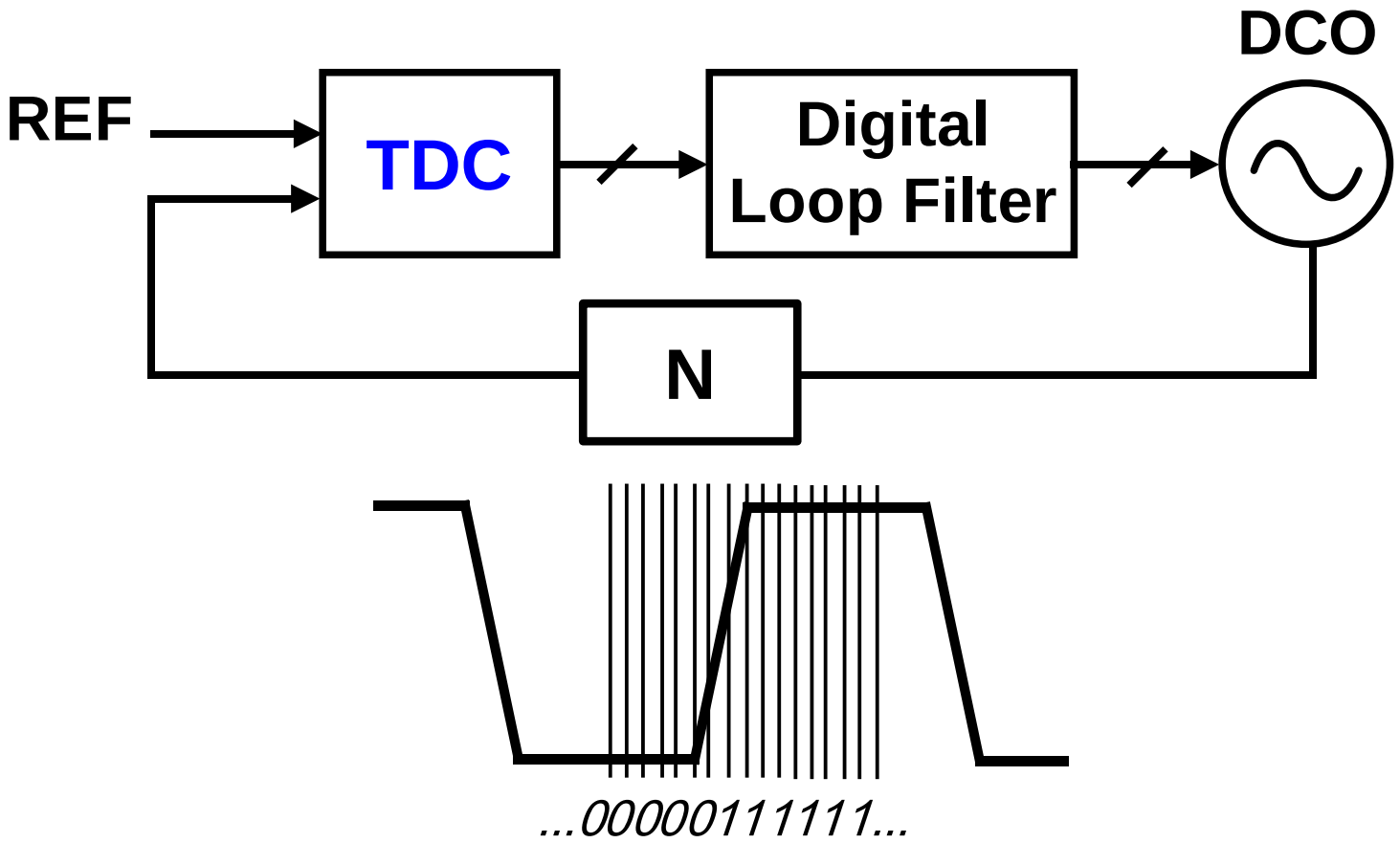
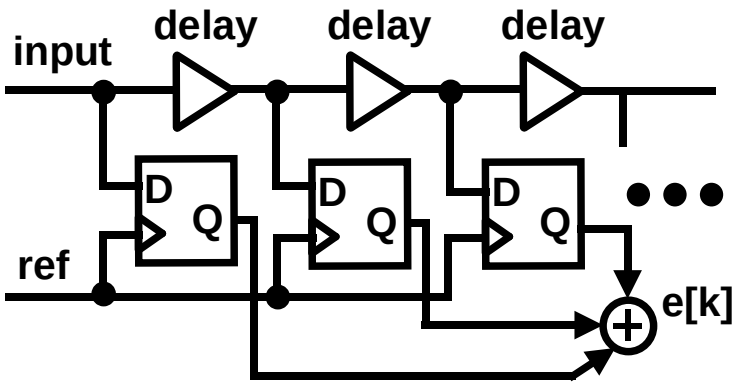
Phase Digitization in AD-PLL

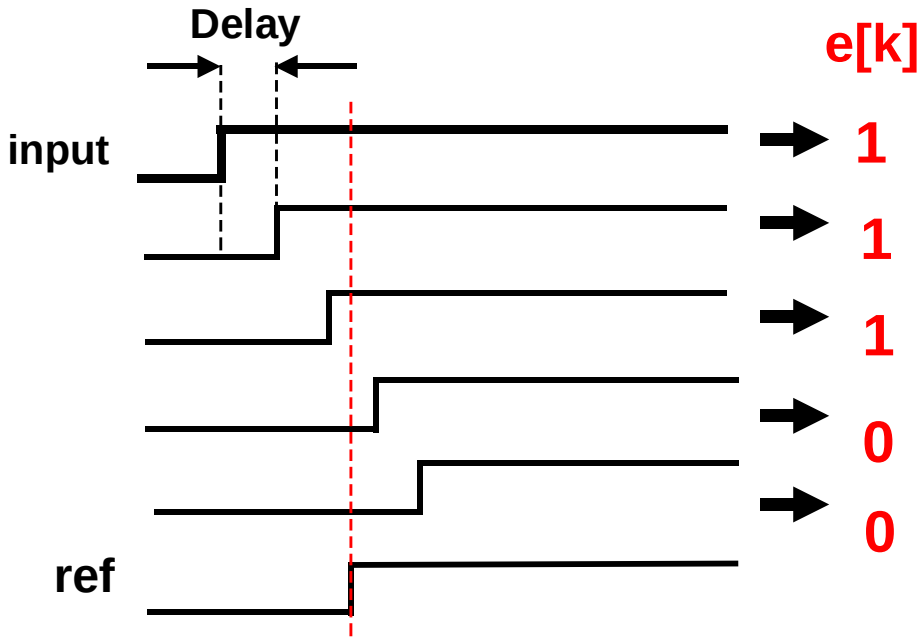


Digital phase detector is usually based on time-domain approach

Time-Domain Digitization

- **Inverter chain**

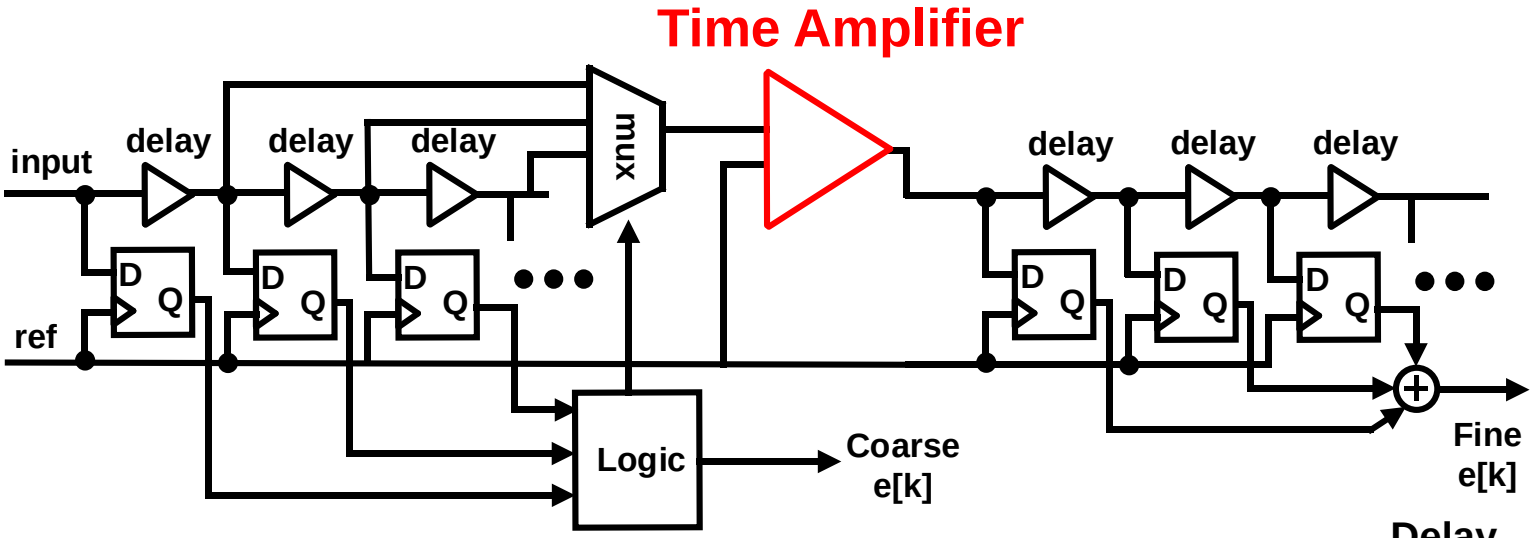




[1] R. Staszewski, JSSC 2005

- Resolution of inverter-chain TDC limited by one propagation delay
- Improved resolution by Vernier chain but worsen linearity and increase power

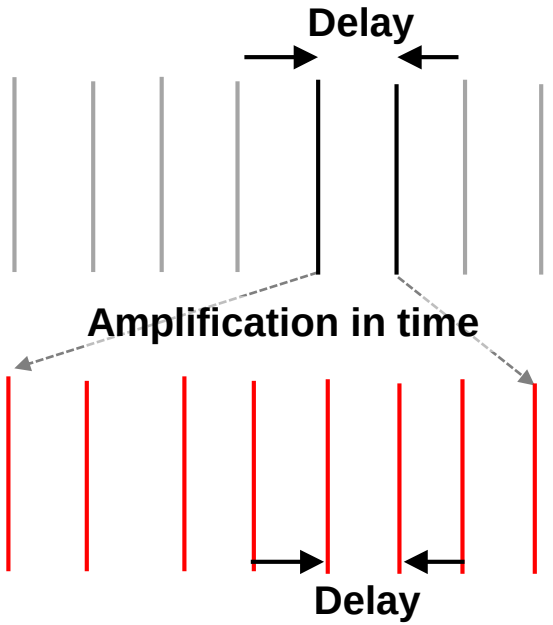
Time-Domain Digitization (Cont.)



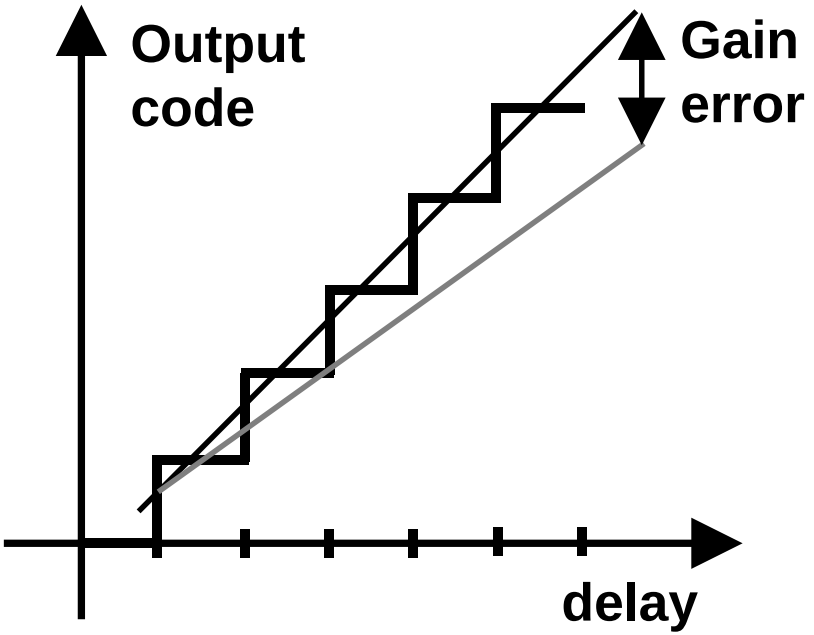
- **Time Amplifier ([2] M. Lee, JSSC 2008)**

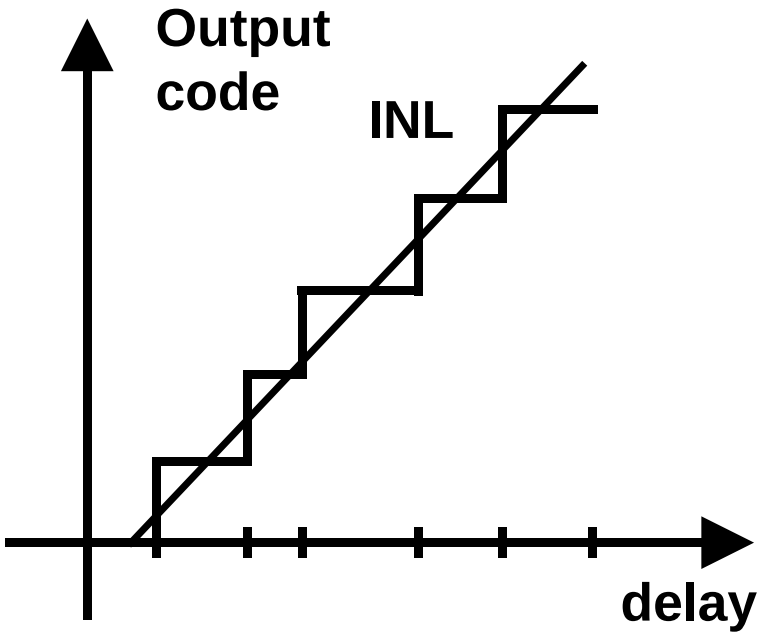
  - Improves resolution

  - Gain error, mismatch, nonlinearity of TA causes problems



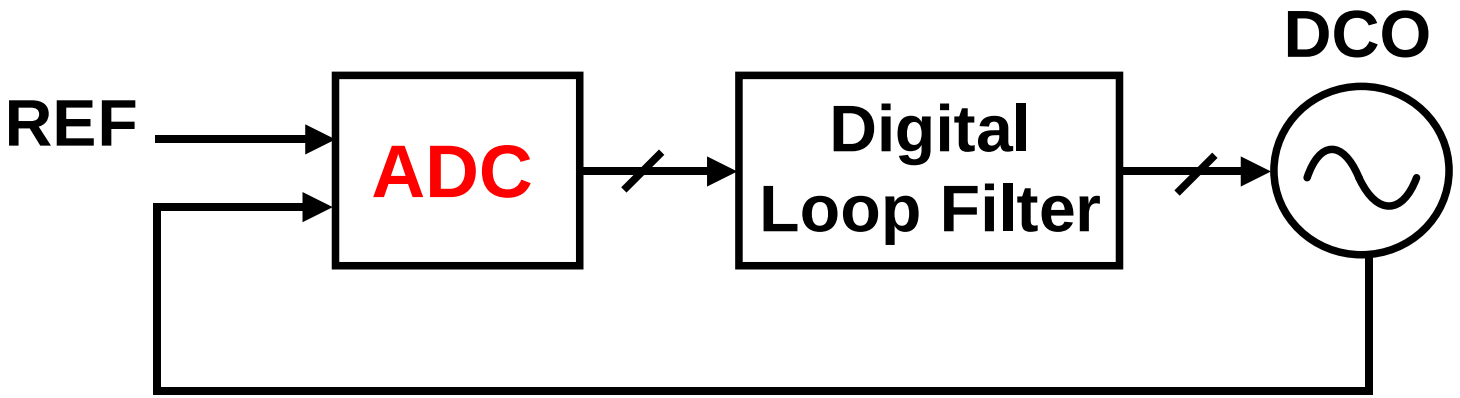
Common Issues in TDC

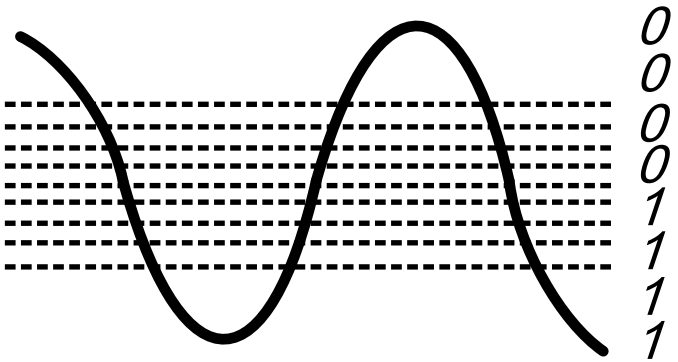




Jitter in delay line causes nonlinearity in TDC

Proposed ADC-PLL

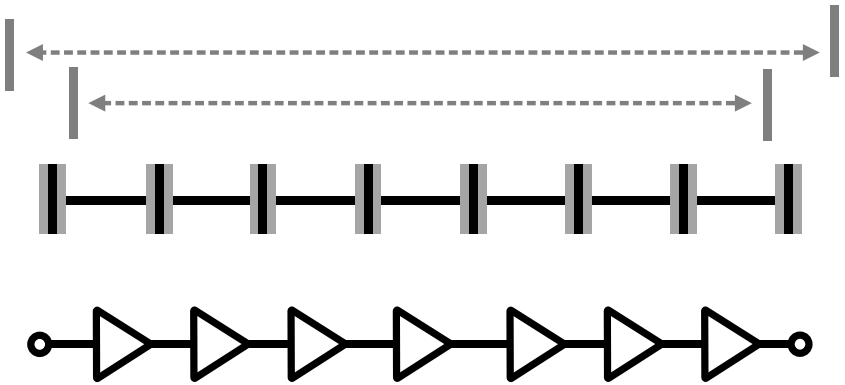




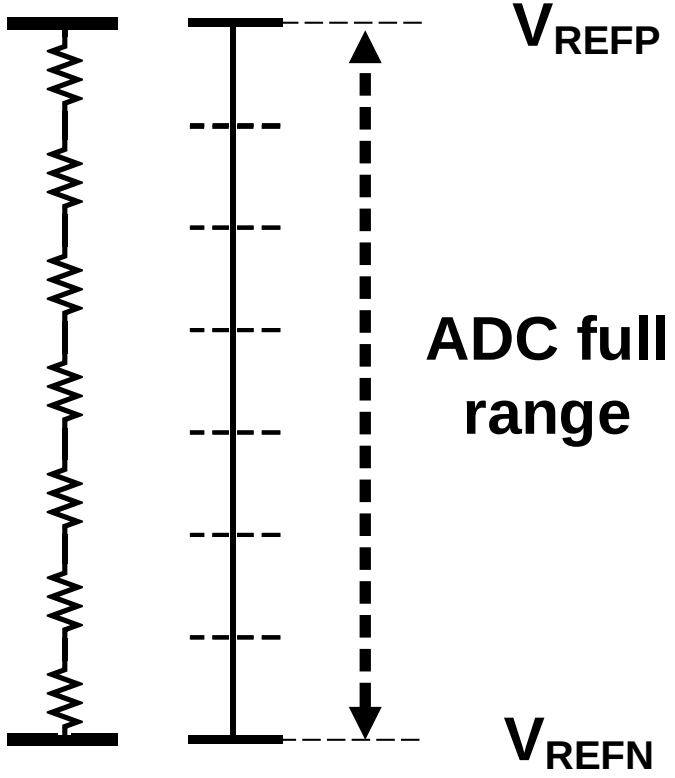
How about voltage-domain digitization?

Time vs. Voltage Domain

TDC full range varies over PVT variations

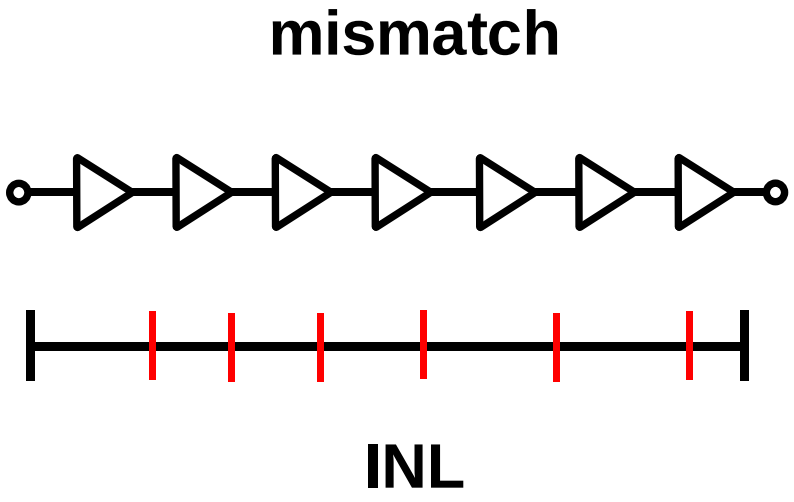


TDC gain needs calibration

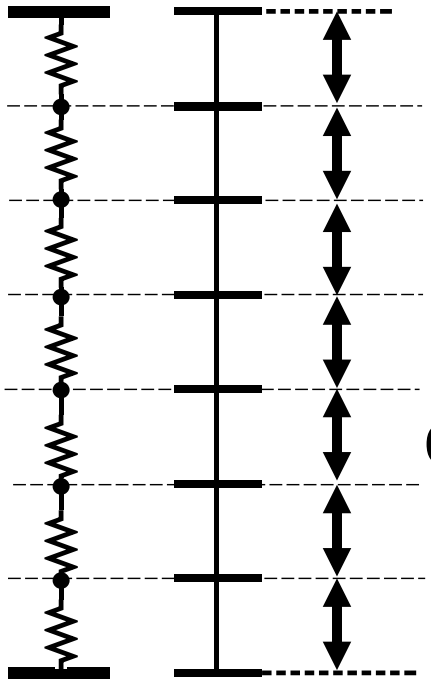


ADC full range can be accurately generated

Time vs. Voltage Domain (Cont.)

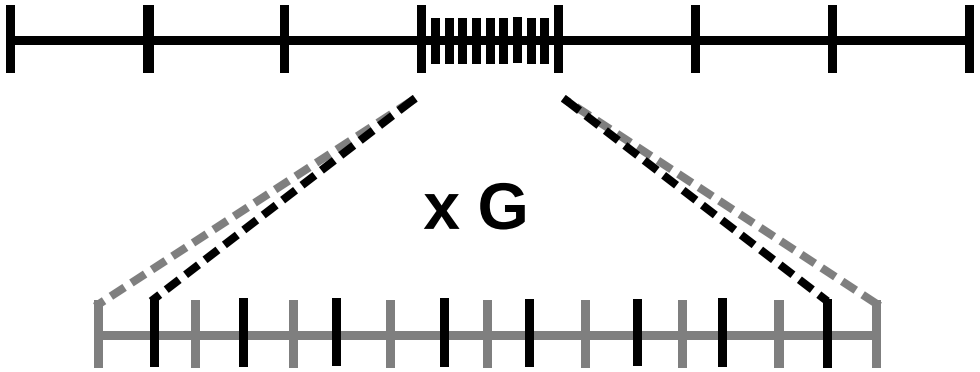


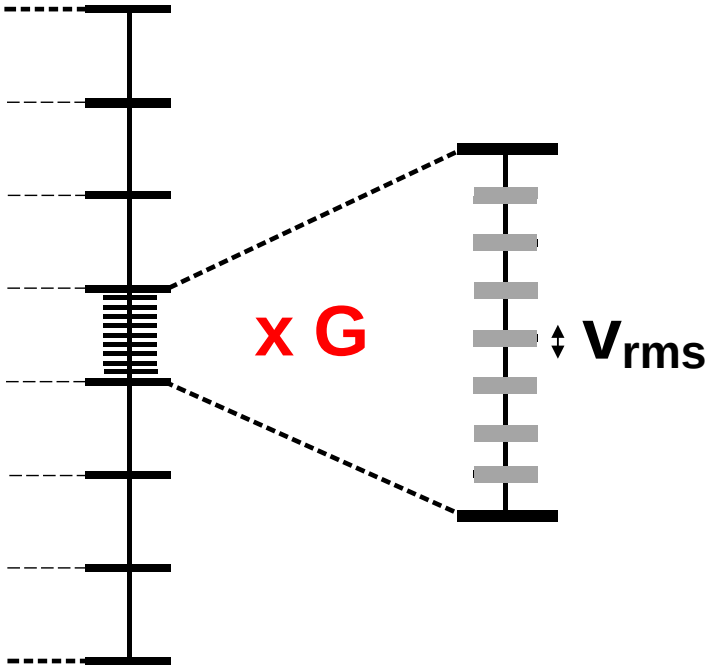
Require large hardware cost for nonlinearity calibration



Linear voltage division can be achieved by a resistor ladder

Time vs. Voltage Domain (Cont.)

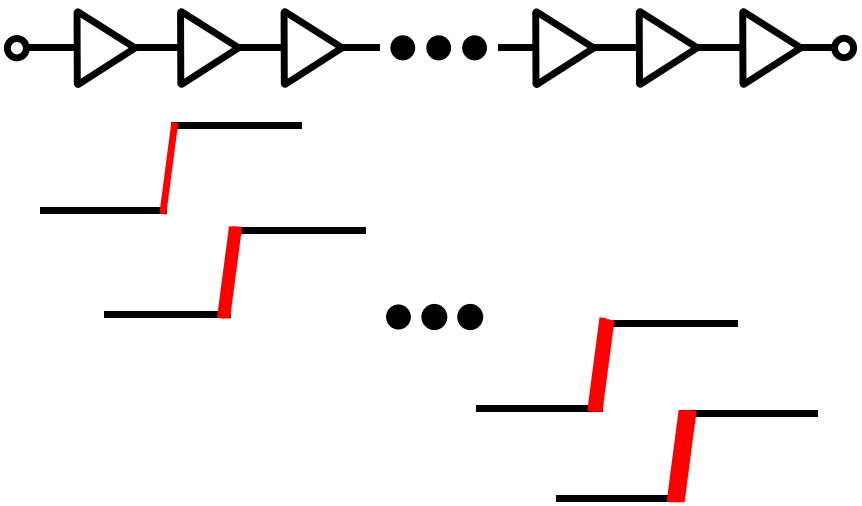


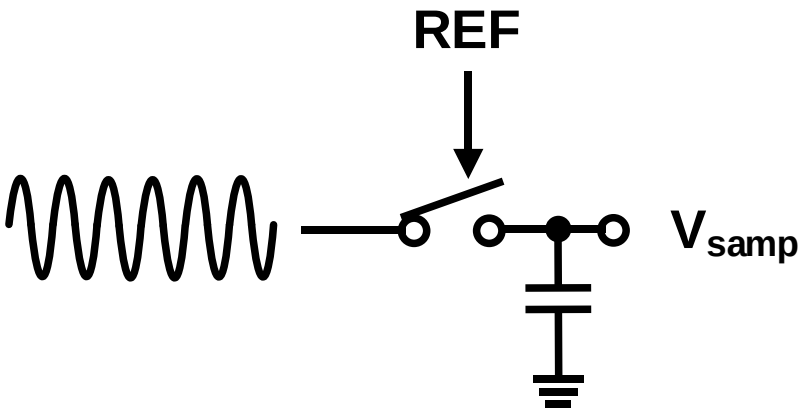


Time amplifier is not linear

Voltage amplifier can be very accurate

Time vs. Voltage Domain (Cont.)





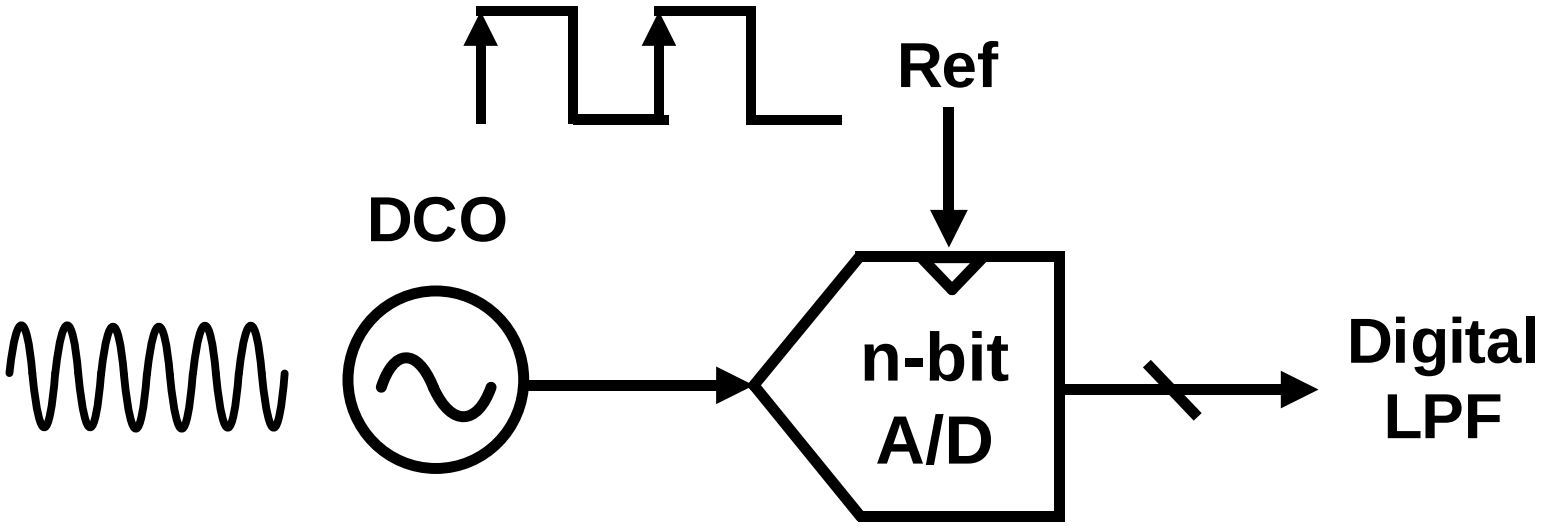
jitter α $\frac{kTC}{I_D^2}$

jitter α $\sqrt{kT/C}$

Not a factor of current

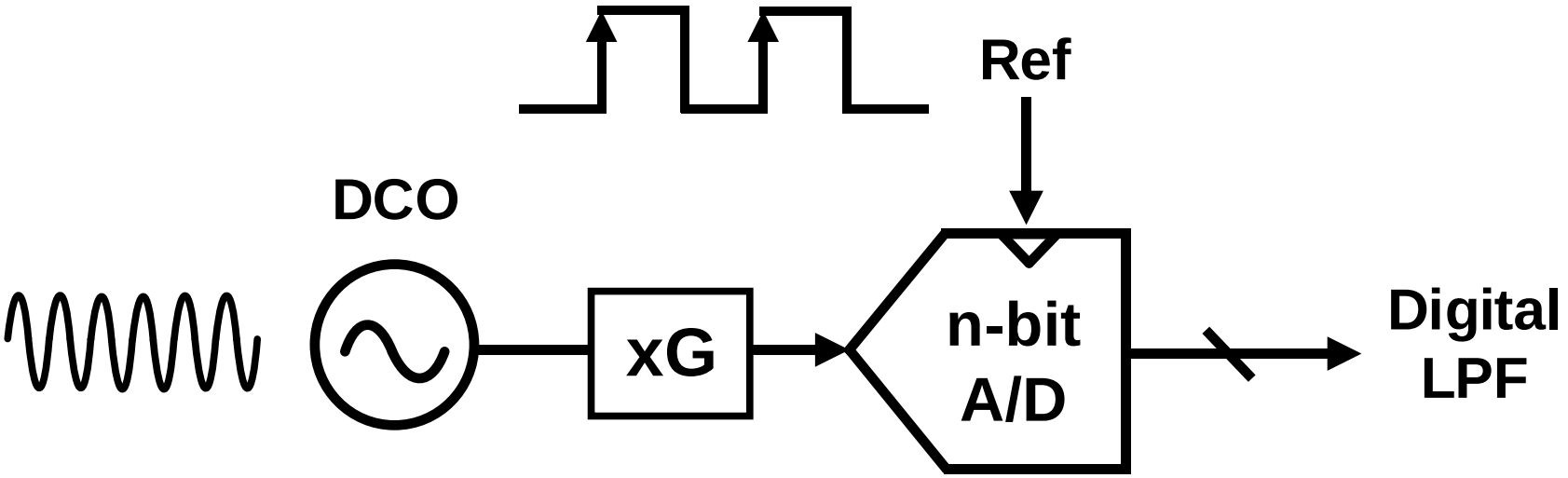
[14] A. Abidi, JSSC 2006

Simplified Operation



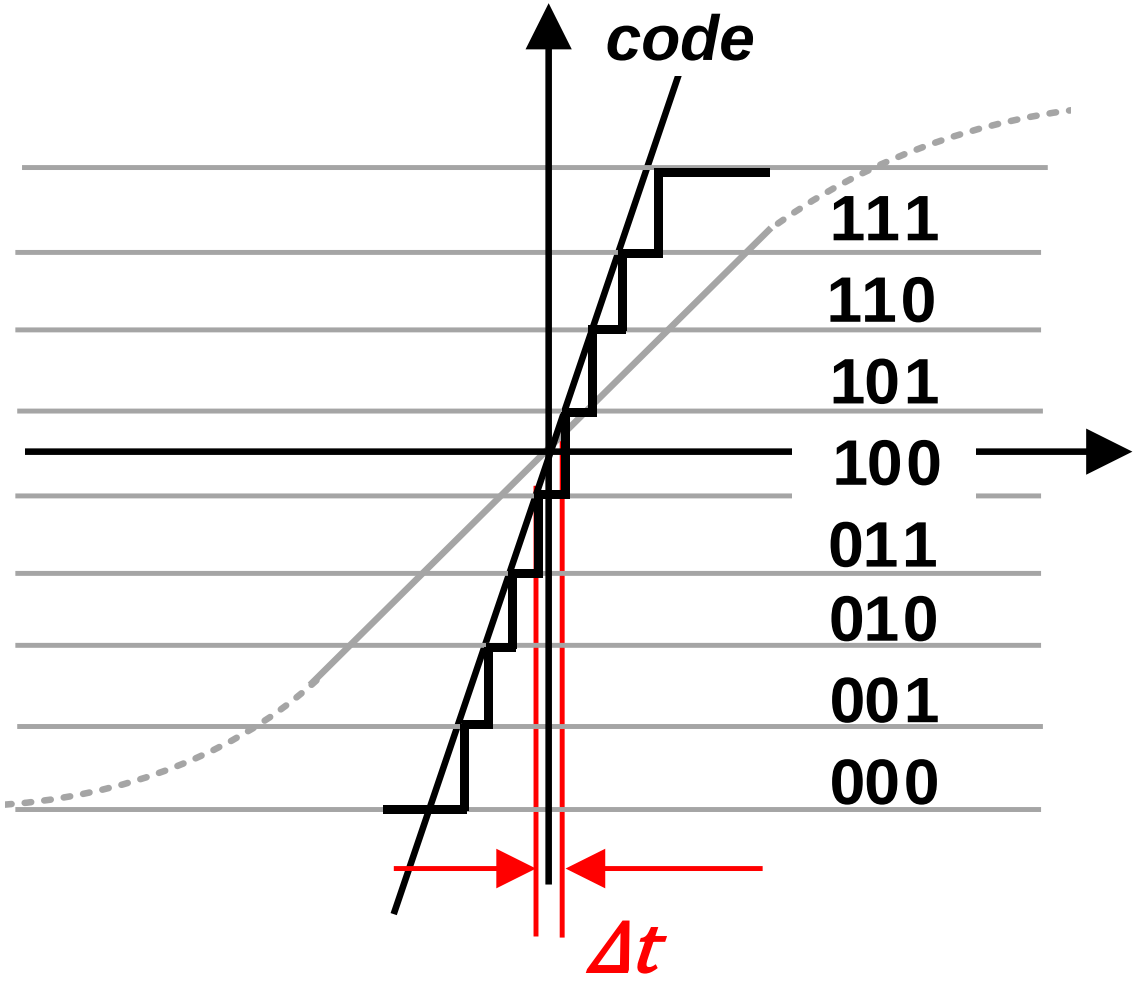
- **Phase leading or lagging can be detected by a simple ADC**
- **Low power operation can be achieved since operating at reference clock**

Simplified Operation (Cont.)



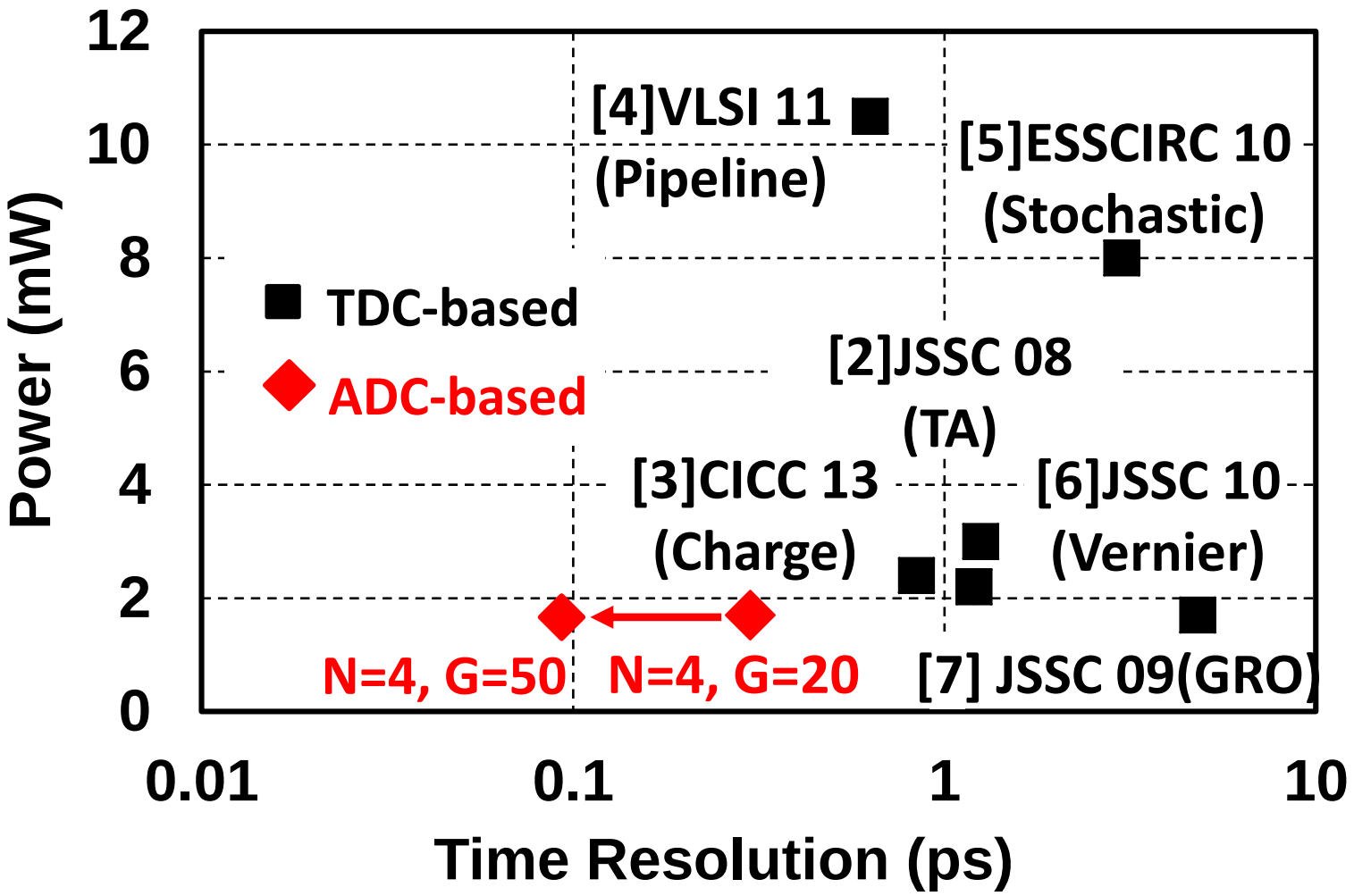
- **Time resolution can be improved by voltage gain amplifier**

Simplified Operation (Cont.)



- Voltage gain increases the slope of input signal resulting in high resolution in time

Trade-off in resolution and power



- Extremely fine resolution can be achieved by increasing gain in voltage

Time vs. Voltage Phase Digitization

	Time / TDC	Voltage / ADC
Full Range	Not accurate (calibration possible)	**Stable**
Linearity	Not accurate (Require lookup table)	**Accurate**
Resolution	Can be fine	**Fine**
Power (P_{DC})	High power is required to lower internal jitter	**Low**

- **Voltage-domain approach has a potential to break trade-off in resolution and power**

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  - **Digitized sub-sampling architecture**
  - **Resolution enhancement**
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  - 4-bit flash ADC
  - Push-pull class-C DCO
- Measurement Results
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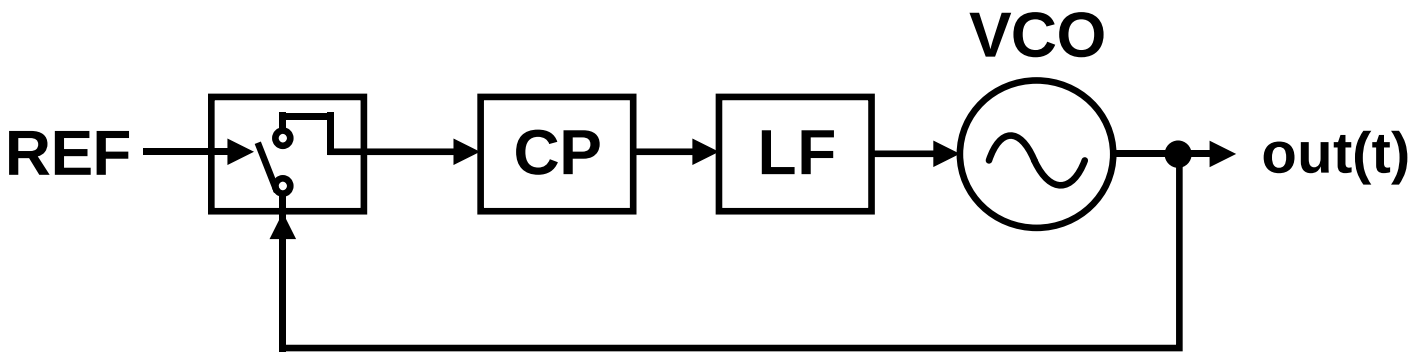
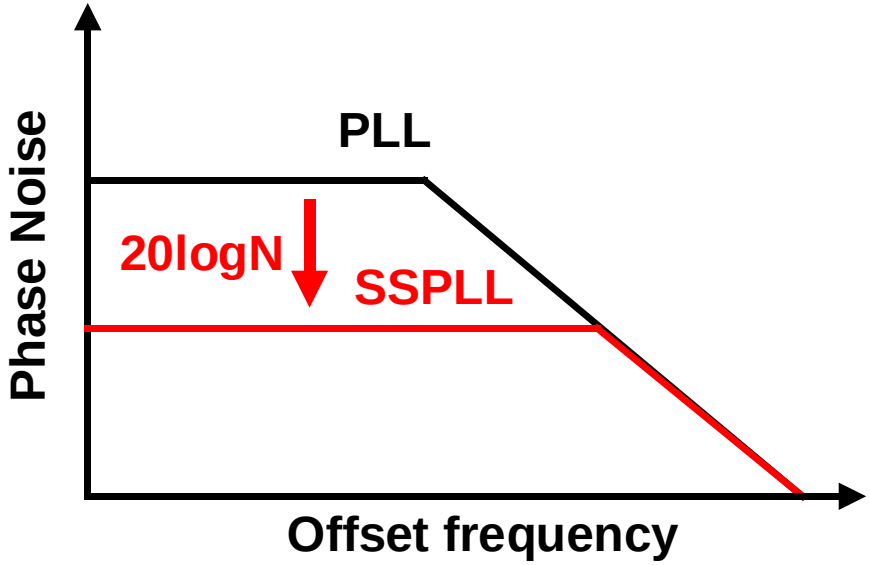
Analog Sub-Sampling PLL



[8] X. Gao, ISSCC 2009

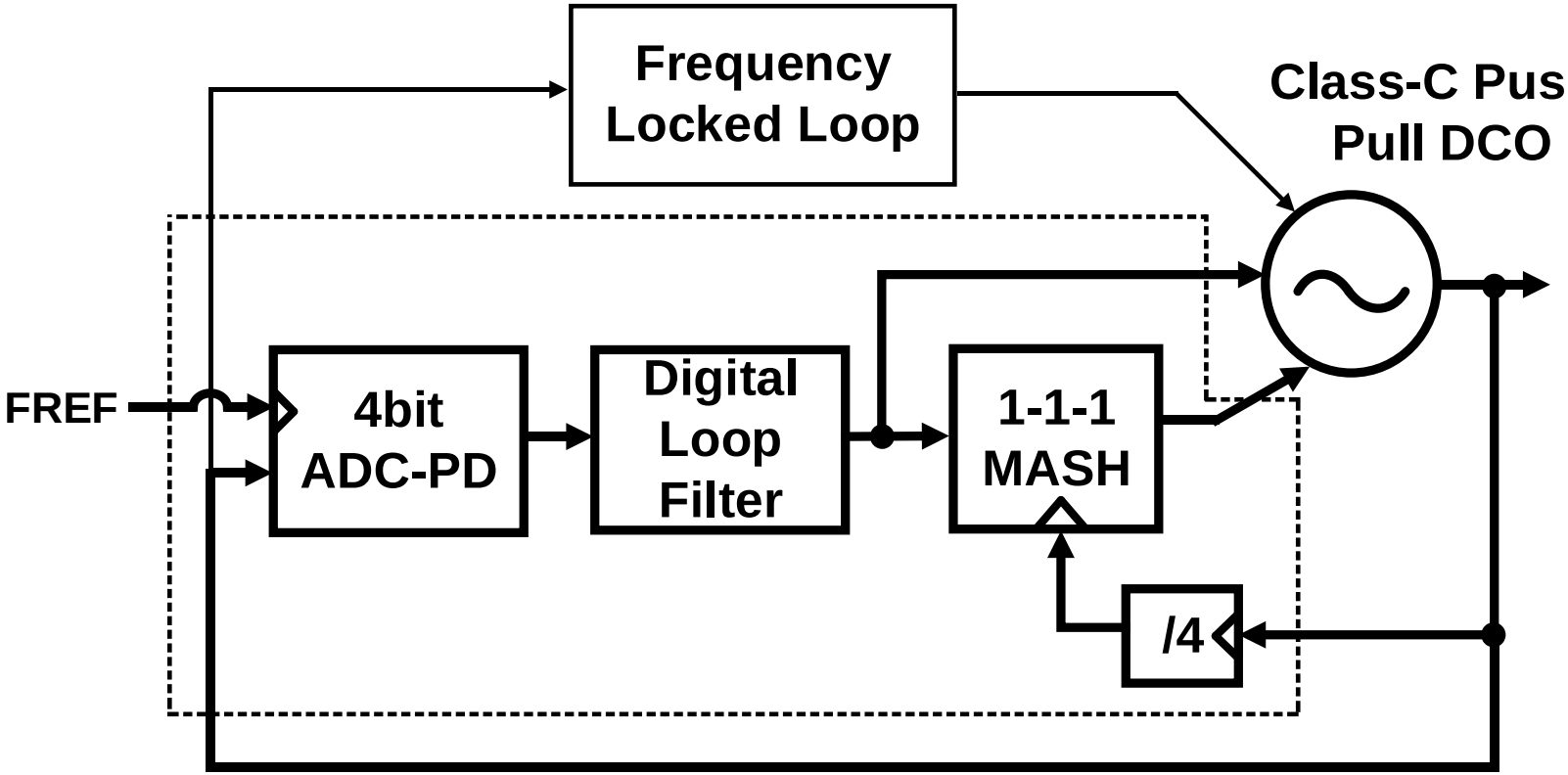
- PD/CP noise is not multiplied by N^2
- No divider noise
- Bulky analog LF
- PVT variations



Proposed ADC-PLL

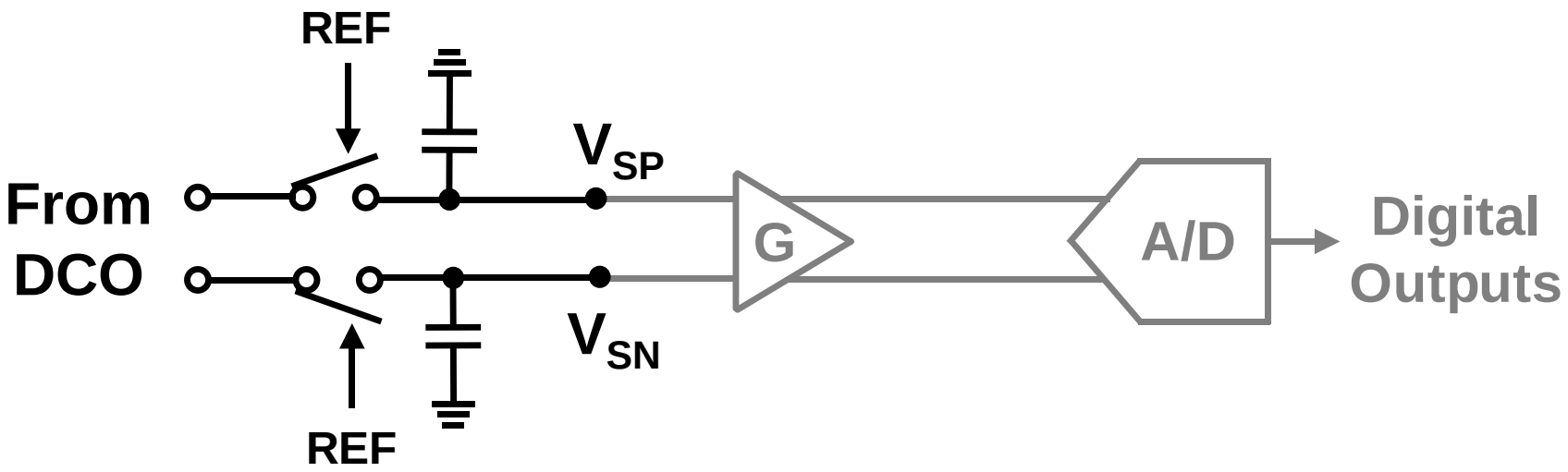
- **ADC-Based PLL**
  - **Digital sub-sampling architecture**
    - **Voltage-domain digital PLL with enhanced resolution**
  - **Resolution enhancement by voltage amplification**
  - **No analog loop filter**
- **Other Building Blocks**
  - **A 4-bit flash ADC with resistive averaging**
  - **Class-C push-pull DCO with adaptive biases**

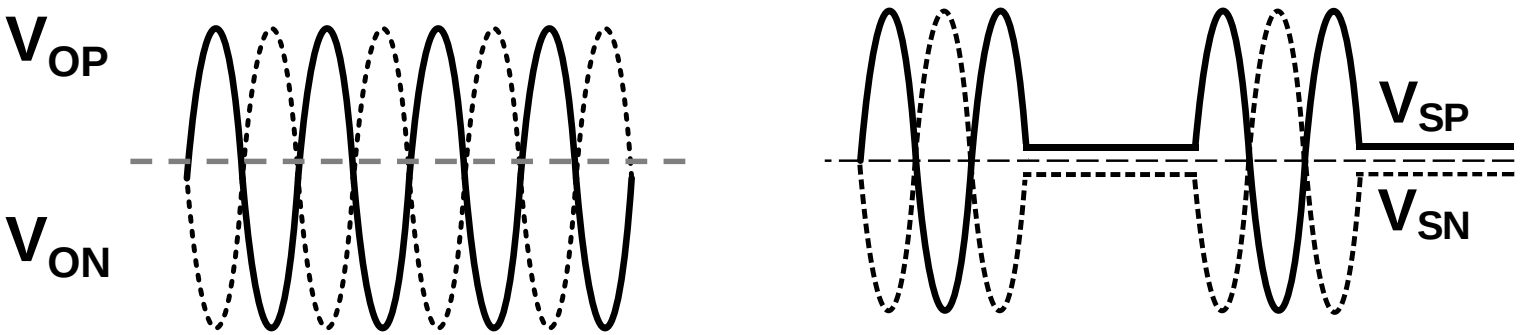
Simplified Block Diagram



- **Frequency locked loop is used to assist the limited acquisition range of ADC PD**

Sample and Hold

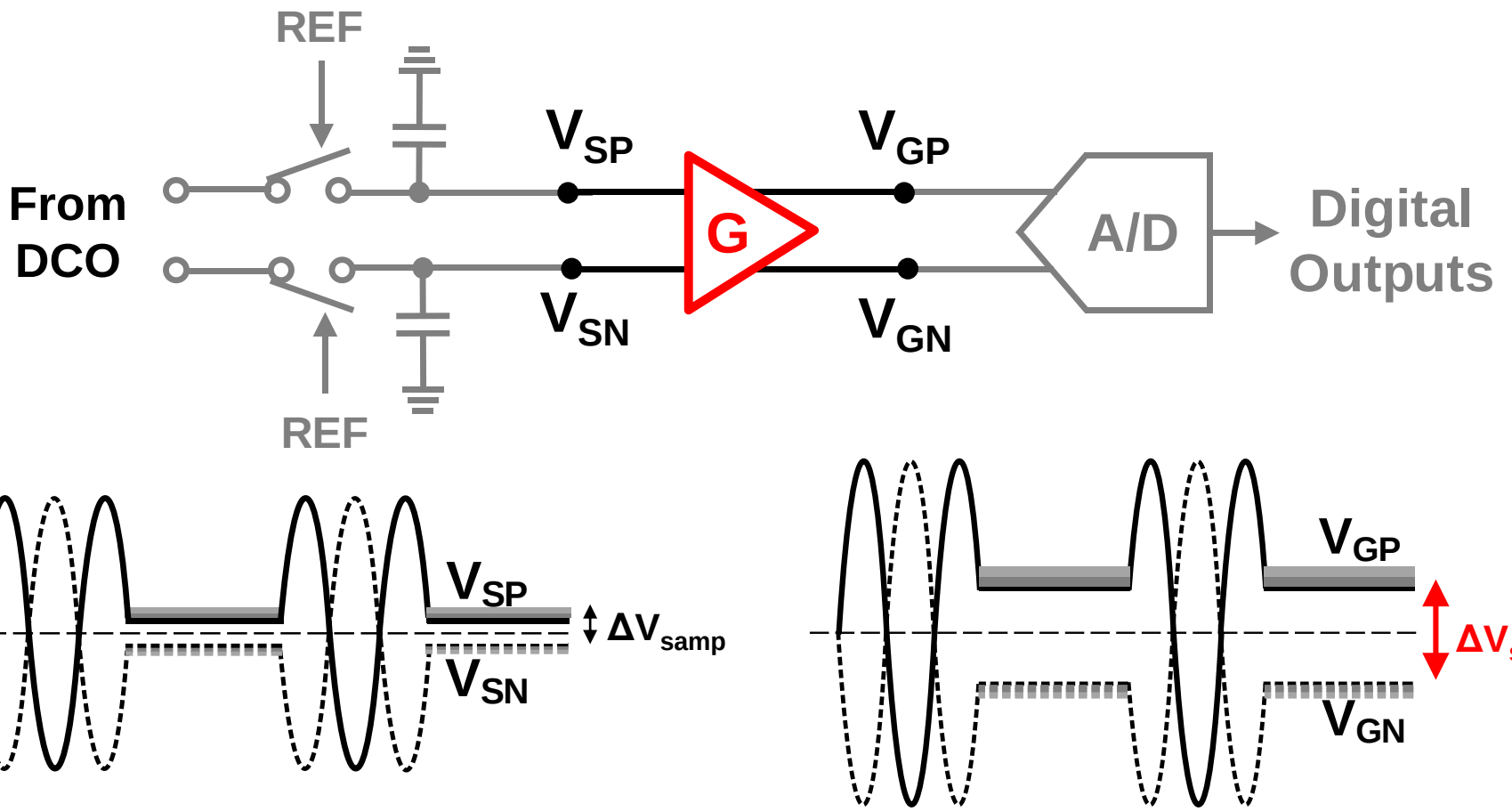




From DCO | After Sampler

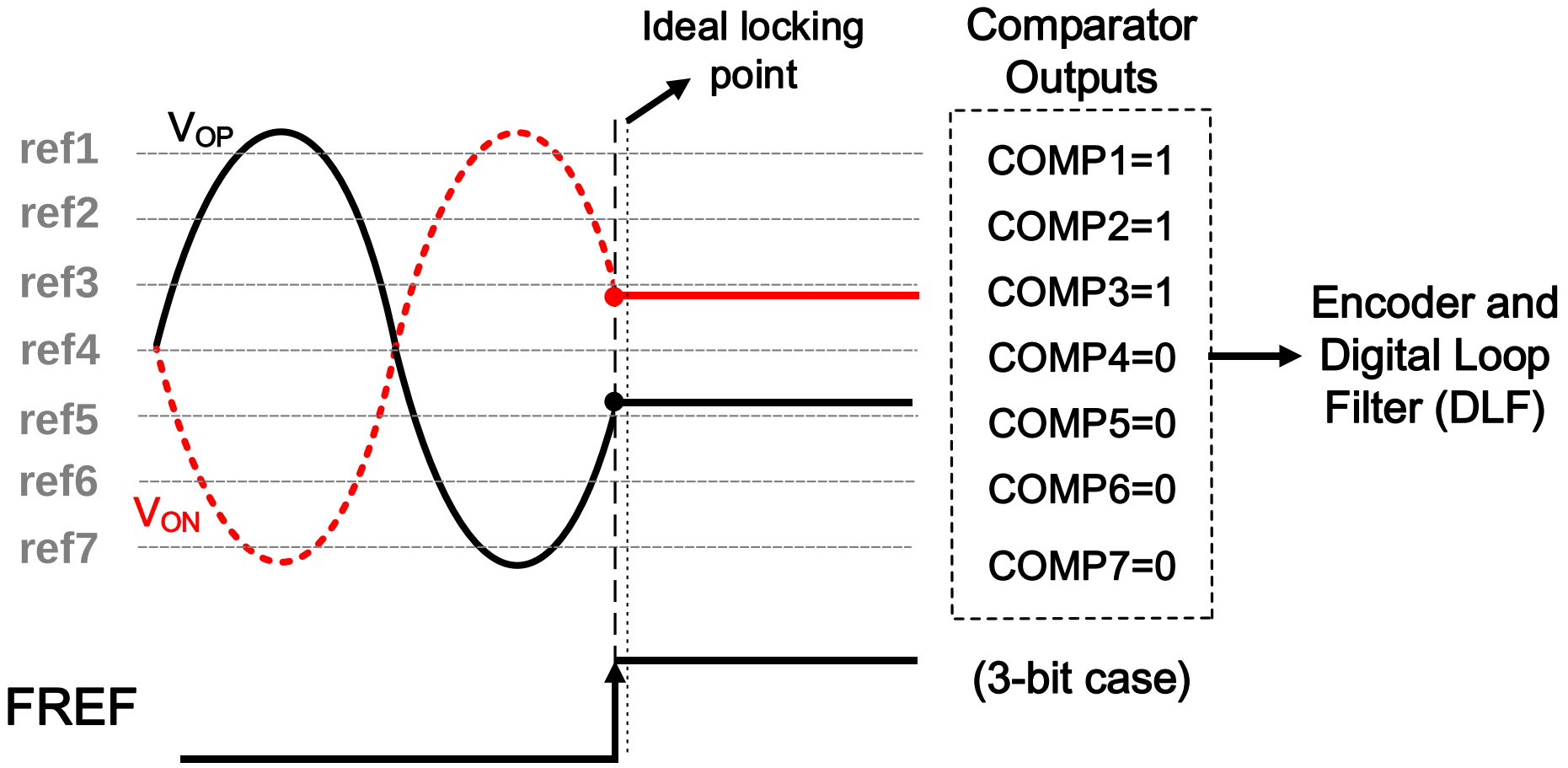
- **Phase difference is sampled into voltage difference**

Gain Amplification



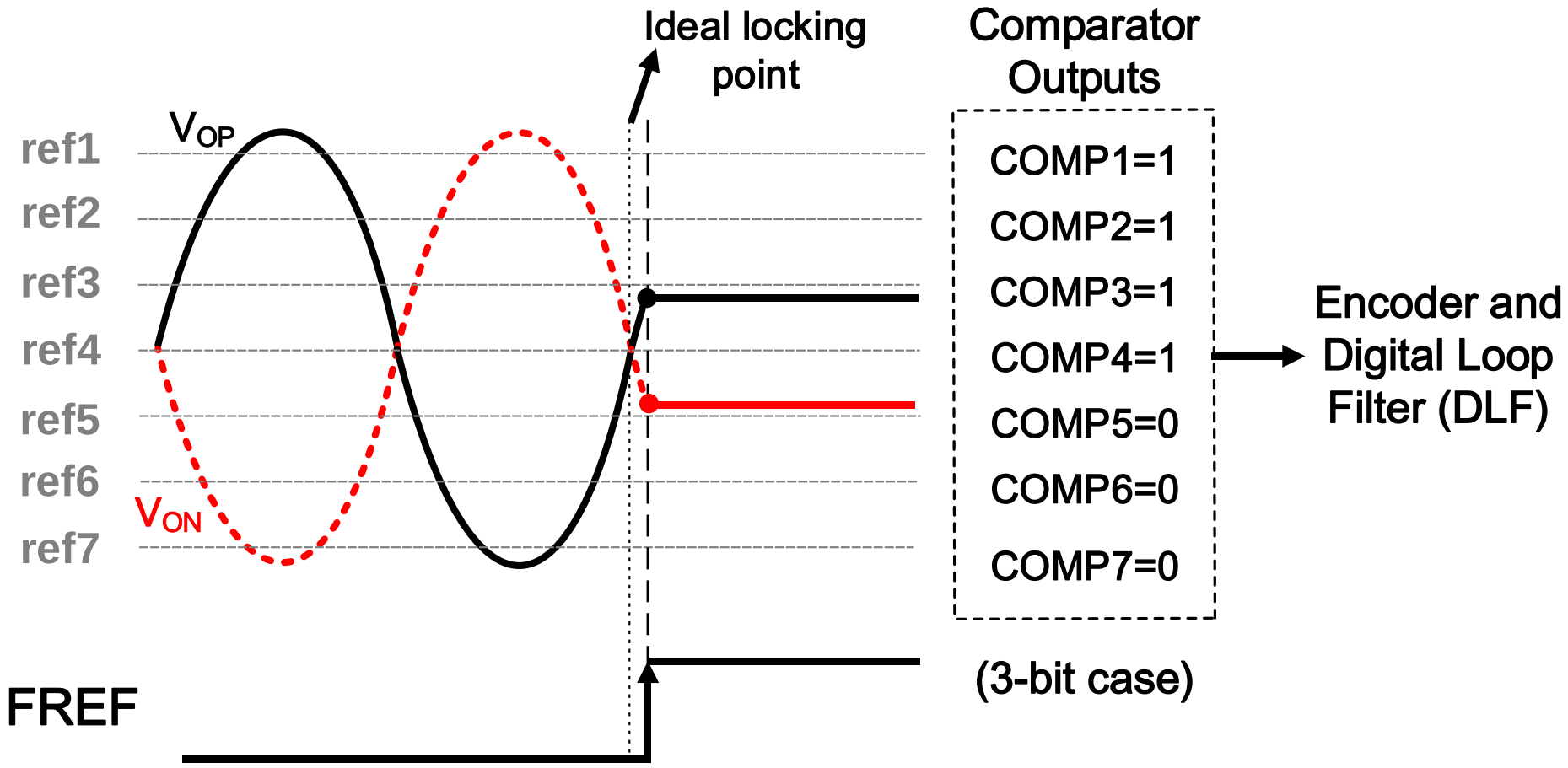
- **Voltage difference can be further amplified for finer resolution**

ADC Phase Detection



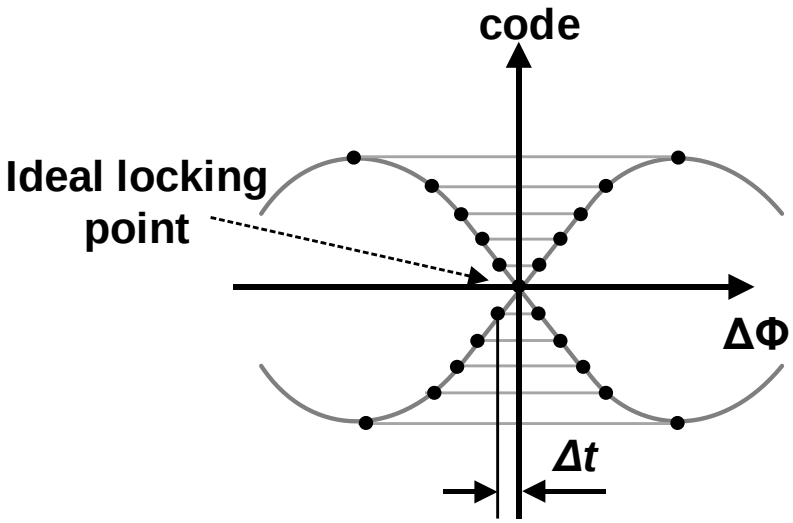
- **Phase of reference clock is faster than that of DCO**

ADC Phase Detection (Cont.)



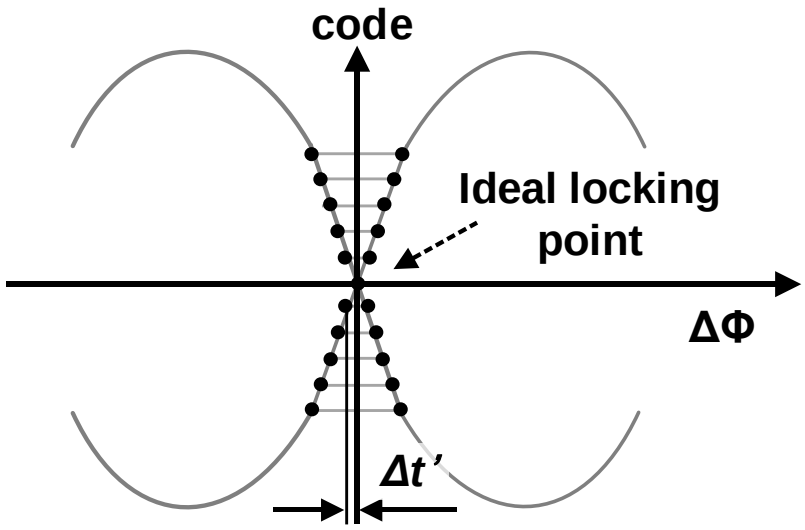
- Phase of reference clock is slower than that of DCO

Resolution Enhancement



$$\Delta t \cong \frac{V_{range}}{2^N \cdot V_{DCO}} \cdot \frac{1}{2\pi f_{DCO}}$$

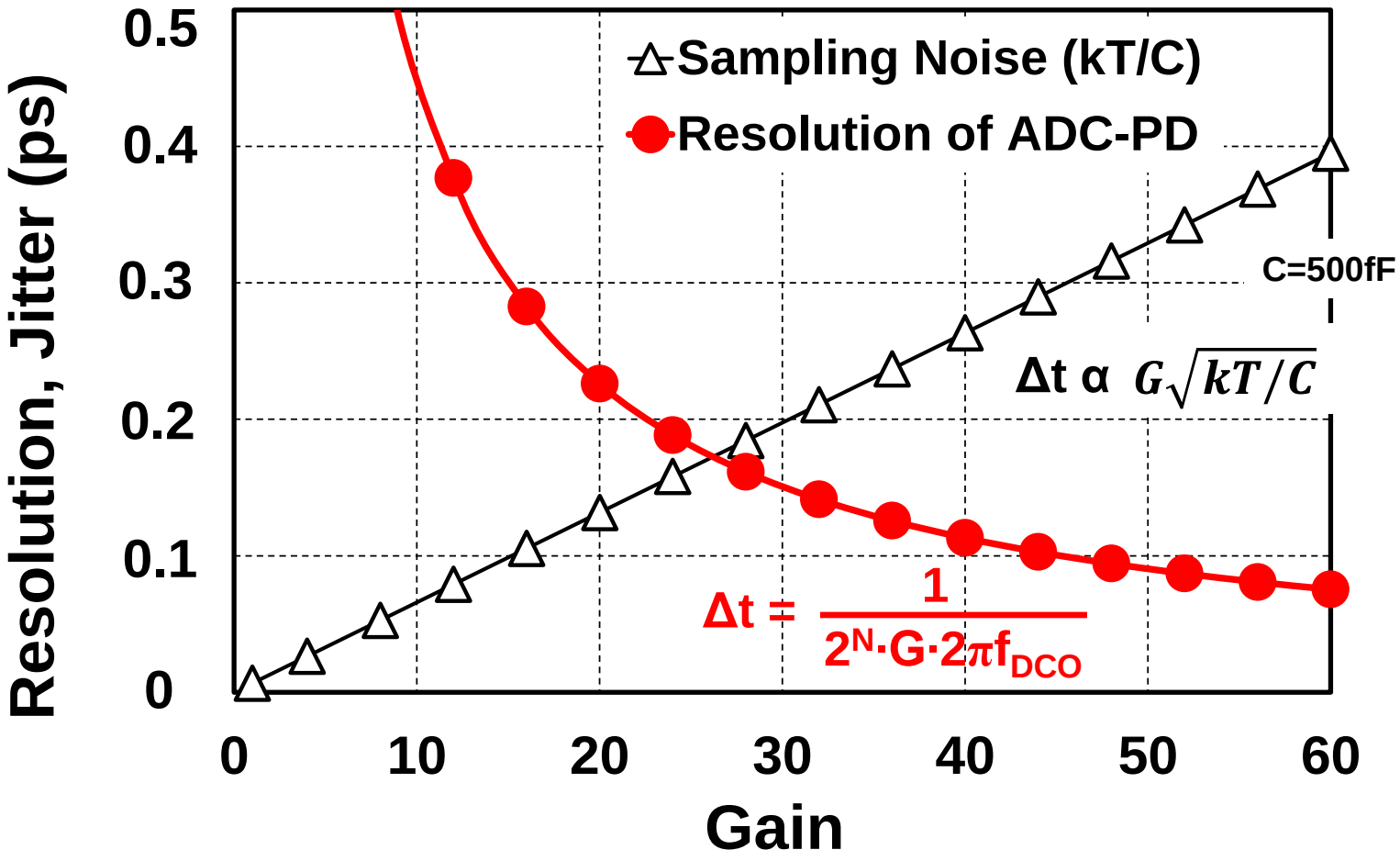
without pre-amplifier G



$$\Delta t' = \frac{1}{G} \cdot \Delta t$$

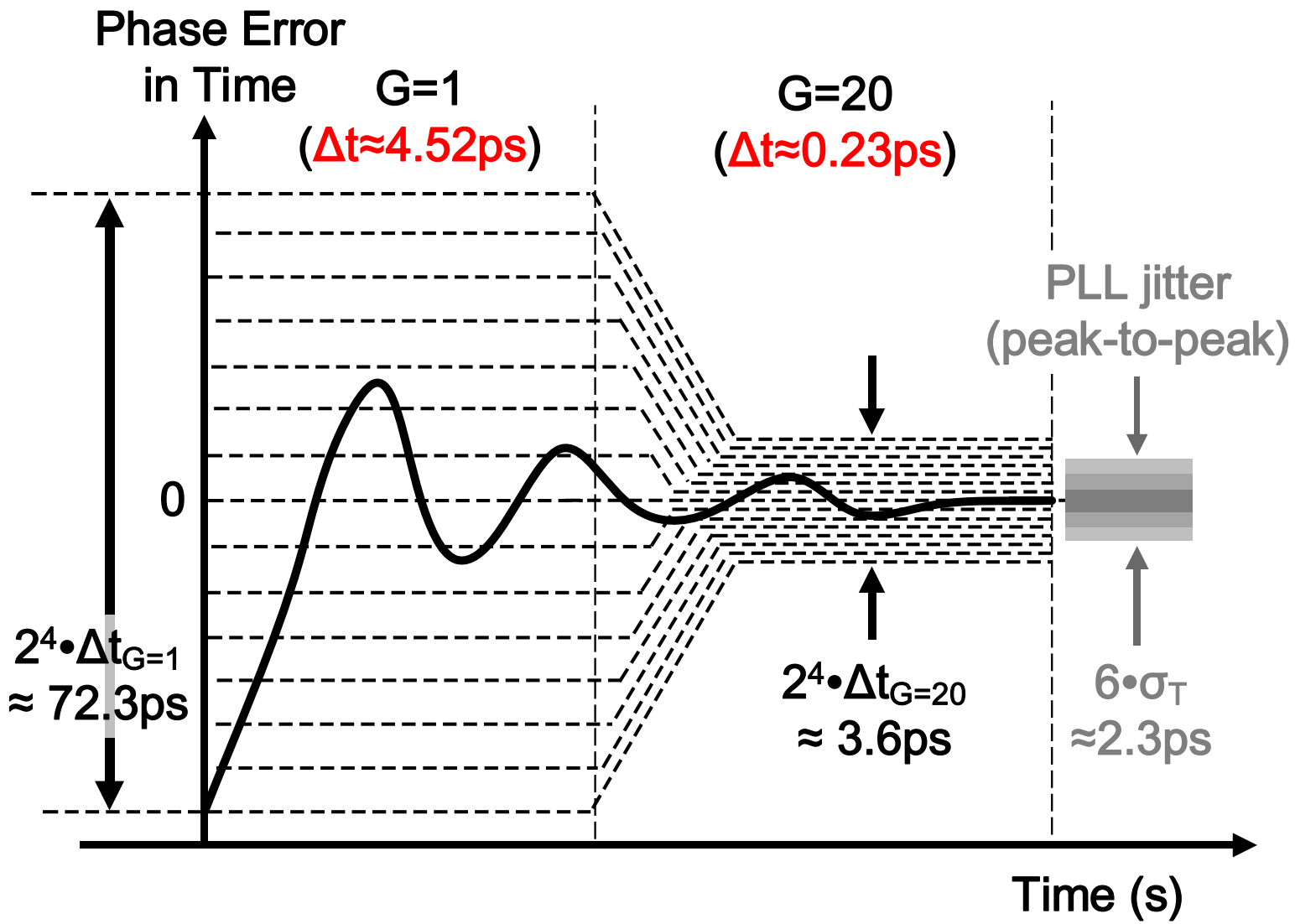
with pre-amplifier G

High Resolution in ADC-PD



- Comparator noise is negligible but sampling noise could limit the PLL phase noise performance

Effect of Resolution Enhancement



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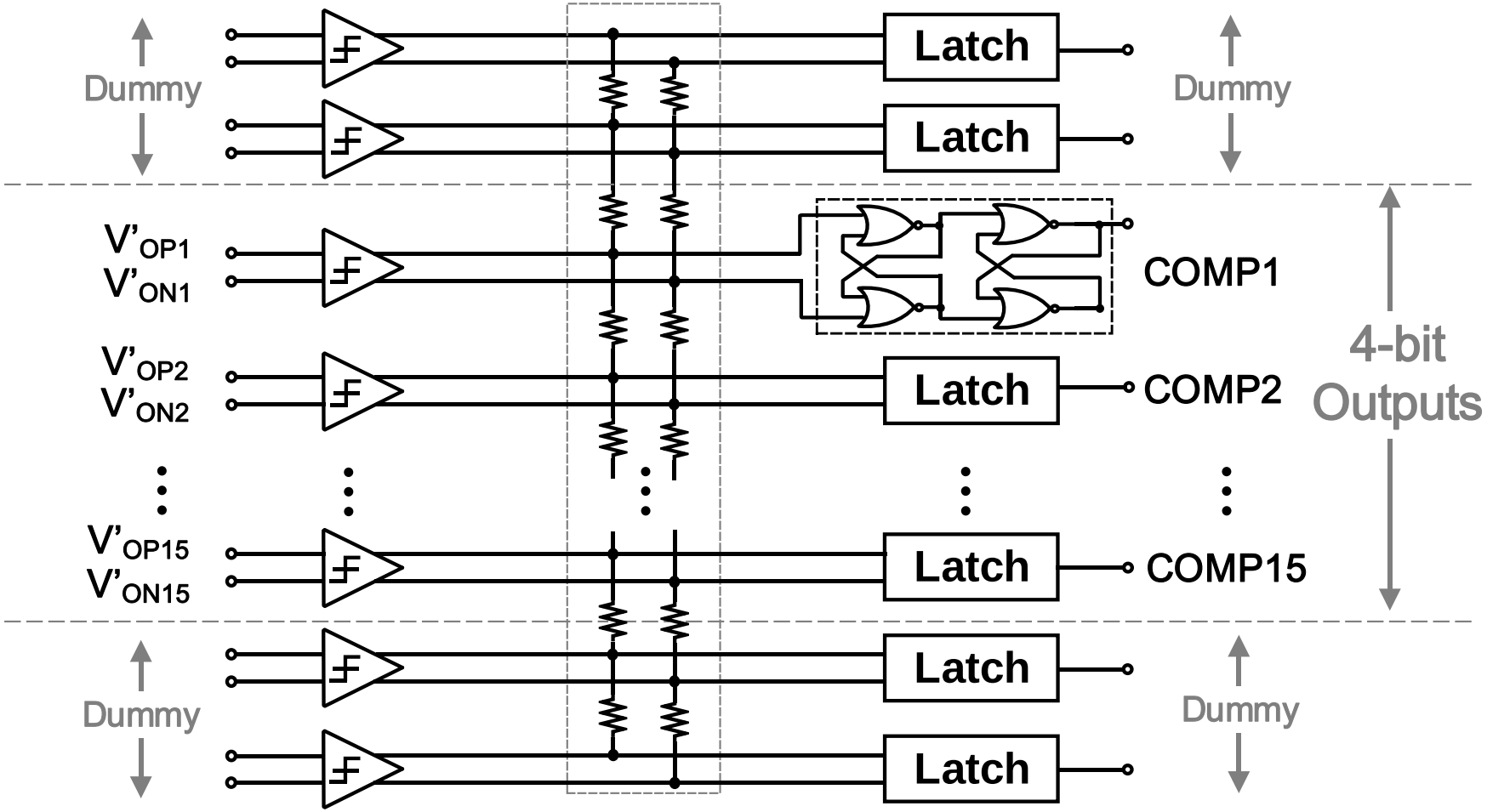
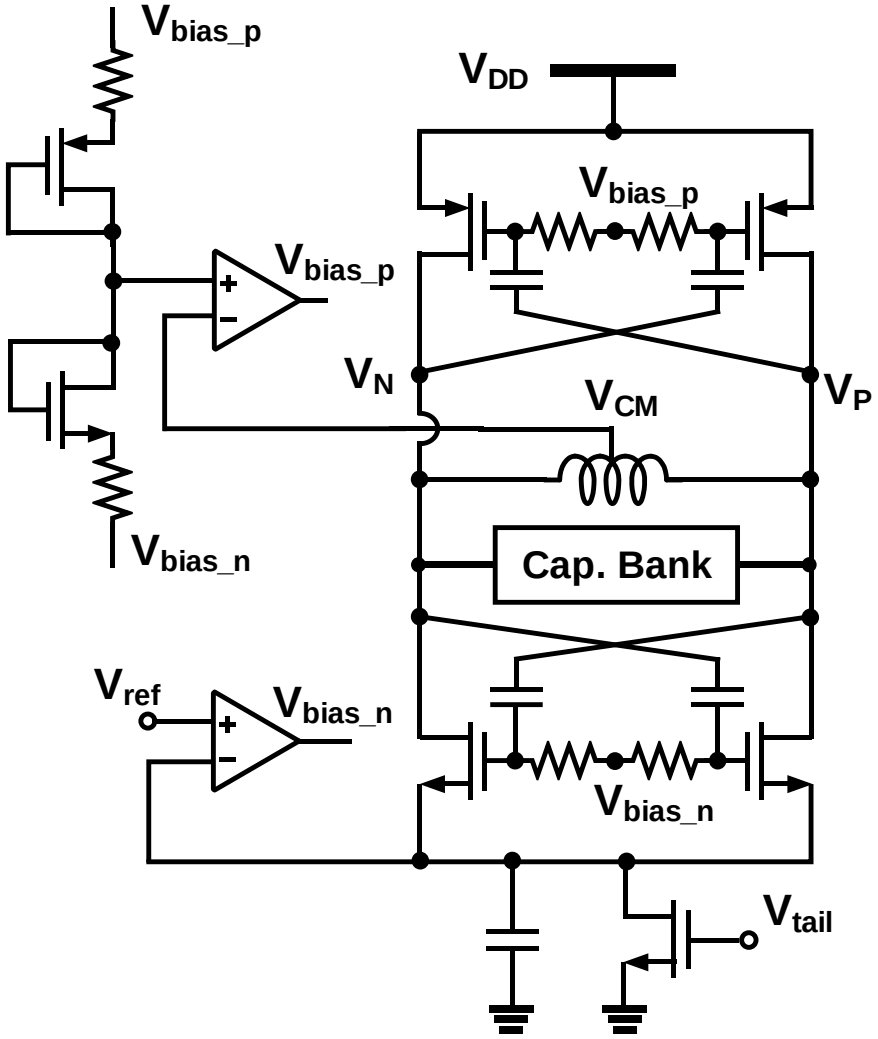
4-Bit Flash ADC

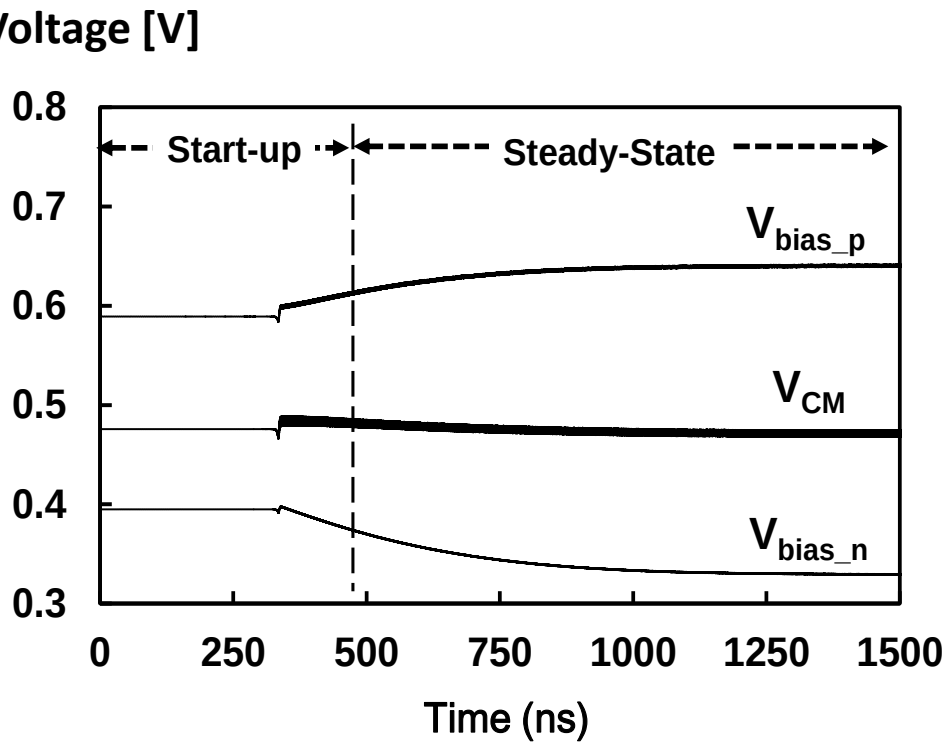


[9] M. Miyahara, ISSCC 2014

- **ADC achieves 10-mV min. resolution with non-calibrated 2.5-mV_{rms} offset**

Class-C Push-Pull DCO

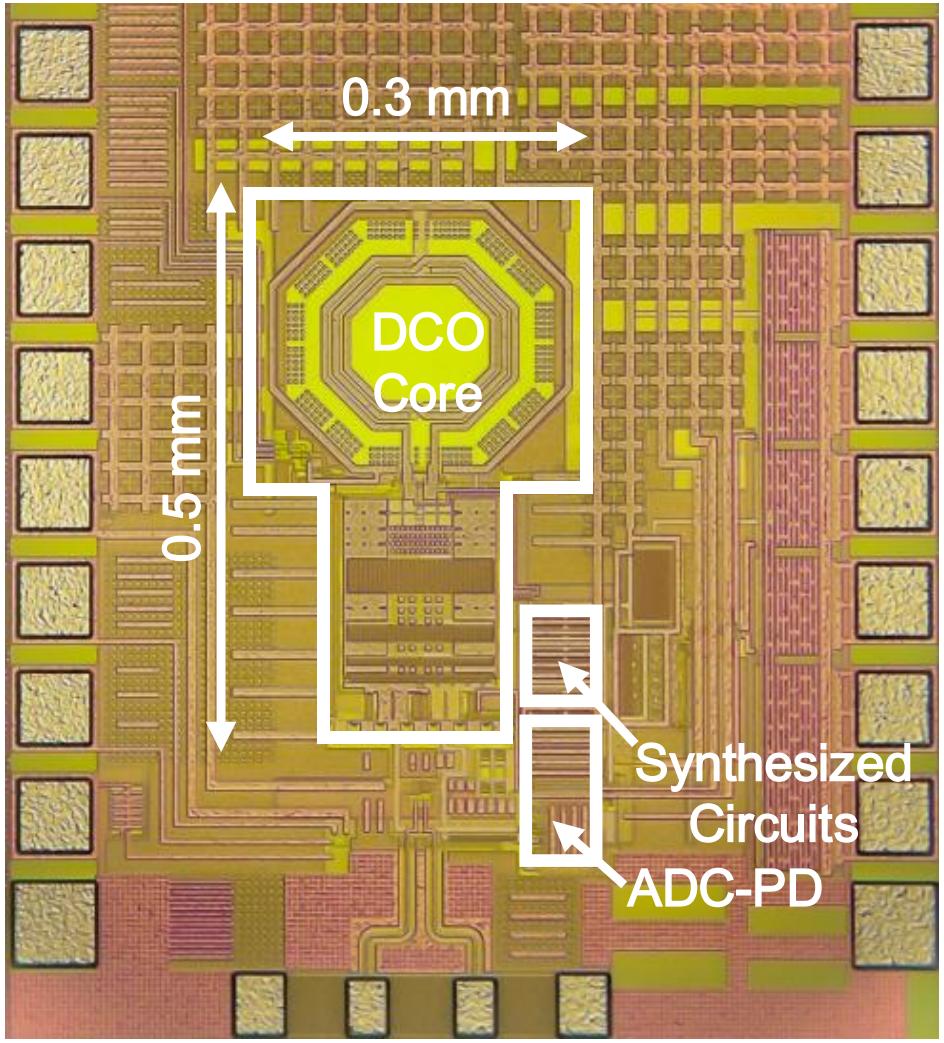




- **Robust Startup**
- **Enhance oscillation swing at steady state**

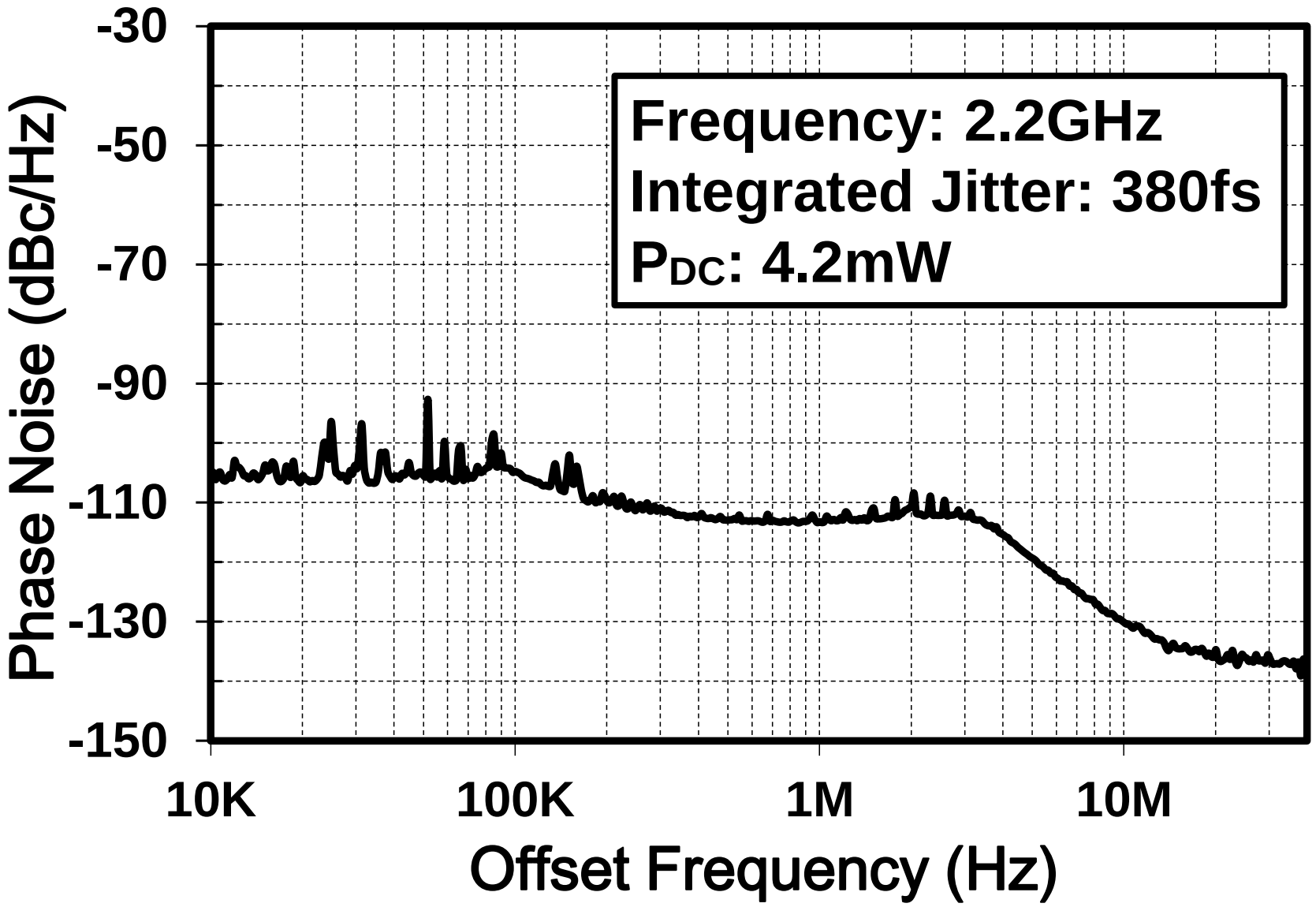
[10] A. Mazzanti, JSSC 2013

Chip Microphotograph

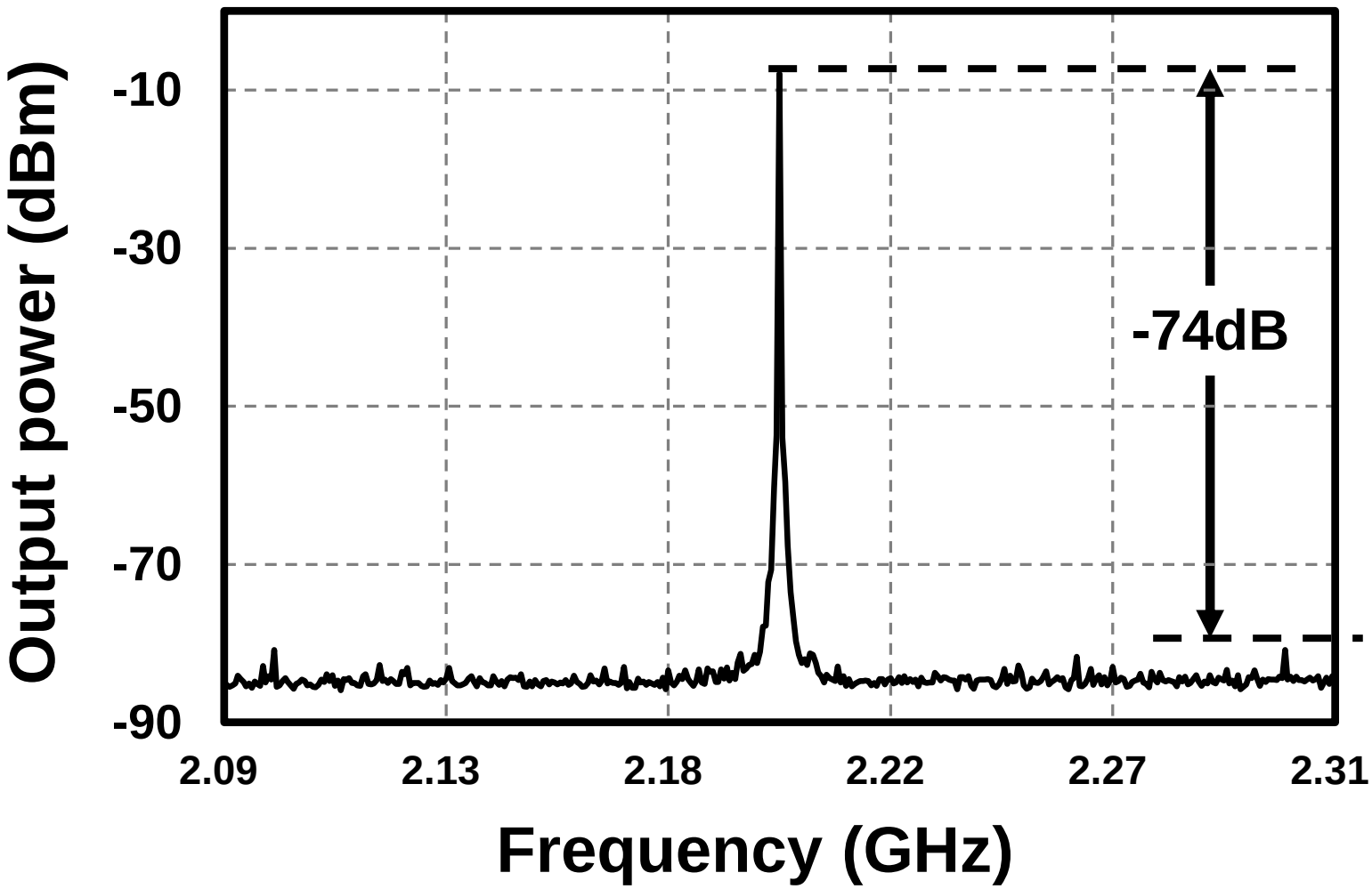


- 65nm CMOS
- Core Area: 0.15 mm^2
- Supply Voltage: 1V
- Power: 4.2mW
  - DCO ~ 1.5mW
  - ADC ~ 1.2mW
  - VGA ~ 0.5mW
  - Others ~ 1mW

Phase Noise



Measured Spur Level



Performance Summary of AD-PLL

	This Work	C. Hsu, JSSC'08	Rylyakov, ISSCC'09	C.Yao, JSSC'13	Chilara, ISSCC'14	M. He, ISSCC'14
Topology	ADC-based	TDC-based	BB-based	TDC-based	TDC-based	TDC-based
Freq.	2.2GHz	3.6GHz	20GHz	2.7GHz	2.4GHz	5.8GHz
RMS Jitter	380fs	200fs	1ps**	230fs	1.71ps	175fs
In-band Phase Noise	-112 dBc/Hz	-107 dBc/Hz	-83** dBc/Hz	-110 dBc/Hz	-90 dBc/Hz	-105 dBc/Hz
Ref. Spur	-74dBc	-65dBc	N/A	-75dBc	-70dBc	N/A
PLL FoM*	-242dB	-237dB	-220dB**	-240dB	-236dB	-244dB
Power	4.2mW	47mW	64mW	17mW	0.9mW	12.9mW
Area	0.15mm^2	0.95mm^2	0.11mm^2	0.62mm^2	0.20mm^2	N/A
Tech.	65nm	130nm	65nm	180nm	40nm	40nm

*PLL FOM is calculated based on RMS jitter

** Estimated from the figure

Conclusions

- **ADC-based AD-PLL is proposed using Voltage-domain digitization in sub-sampling architecture**
- **Resolution can be enhanced by voltage amplification**
- **Voltage domain approach can help achieving high resolution in phase detection without calibrations**

Acknowledgement

This work was partially supported by MIC, SCOPE, MEXT, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc.

Reference

[1] R. B. Staszewski, *et al.*, “All-digital PLL and transmitter for mobile phones,” IEEE Journal of Solid-State Circuits (JSSC), vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

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Reference (Cont.)

[8] X. Gao, *et al.*, "A 2.2-GHz -7.6mW Sub-Sampling PLL with -126dBc/Hz In-Band Phase Noise and 0.15psrms Jitter in 0.18um CMOS," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, pp. 392-393, Feb. 2009.

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