A 0.048-mm² 3-mW Synthesizable Fractional-*N* PLL with a Soft Injection-Locking Technique

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Outline

- **Introduction**
- **Concept of Soft Injection Locking**
- **Circuit Implementations**
- **Measurement Results**
- **Conclusion**

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Introduction

- **Why High Performance PLL**
  - **Clock generation/distribution**

- **Key Specifications for SoC Clocking**
  - **Small area**
  - **Low power consumption**
  - **Low jitter**
  - **Insensitive over environment variations**
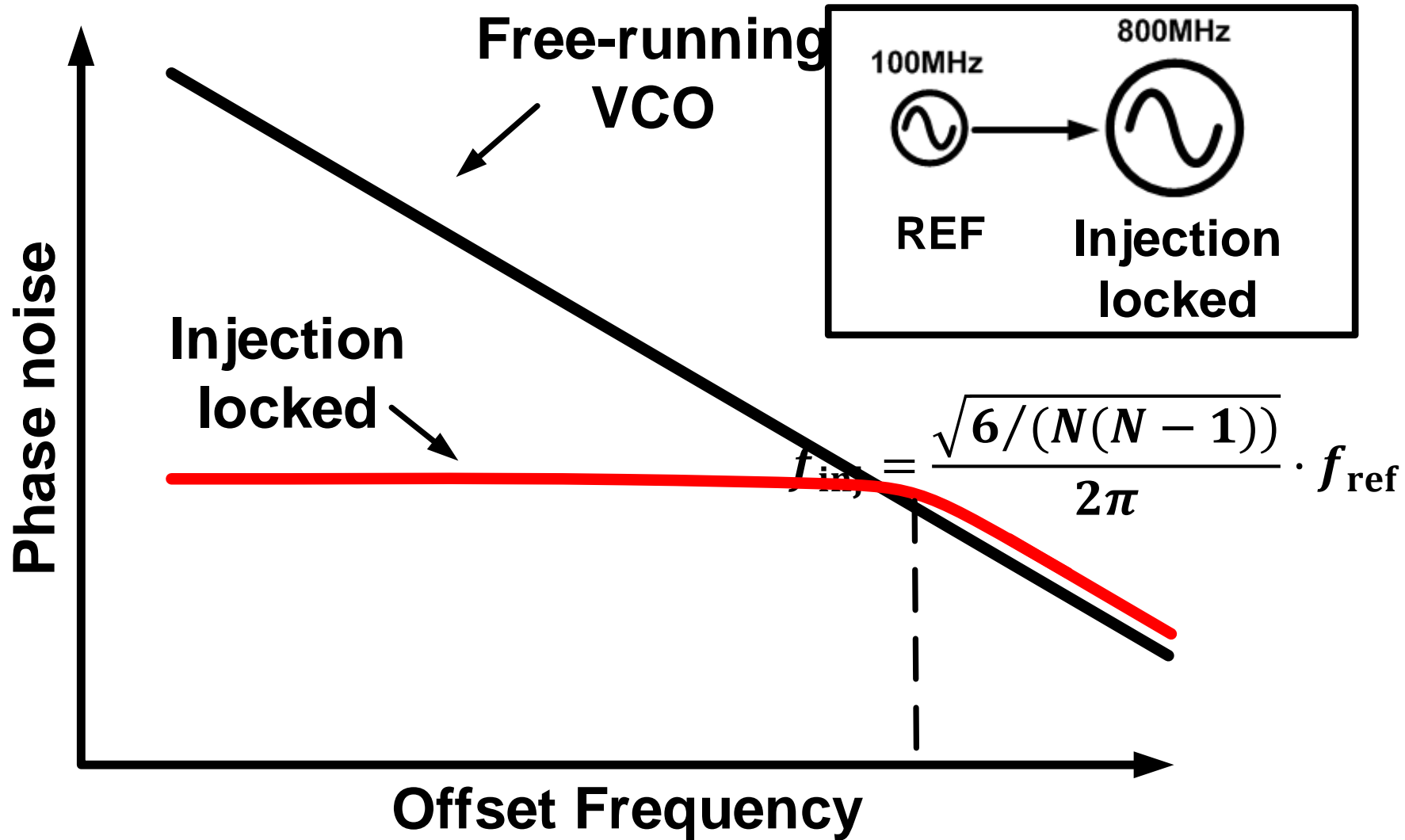 - **Scalable with technology advancement**
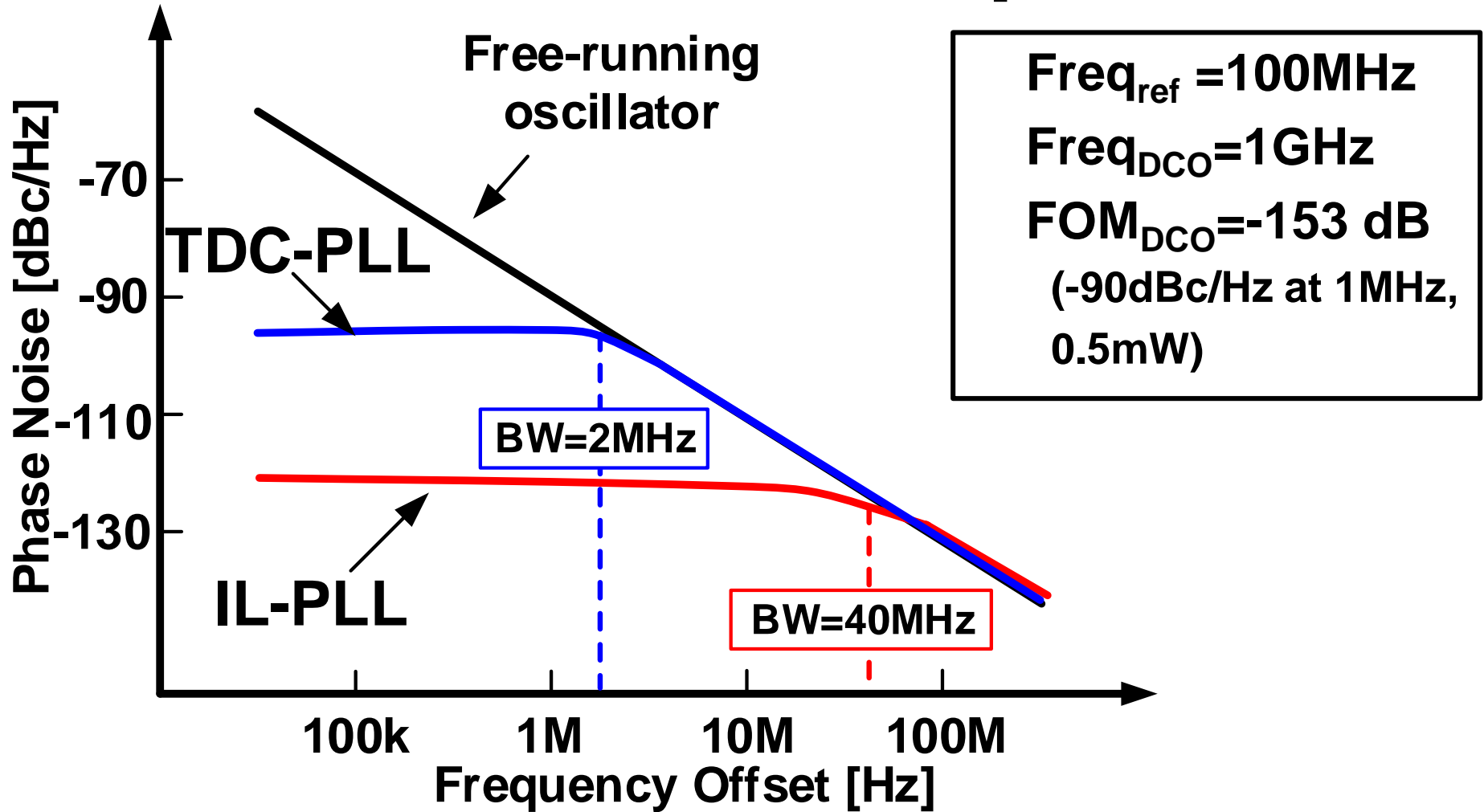
All-digital PLLs

- **TDC-based architecture**
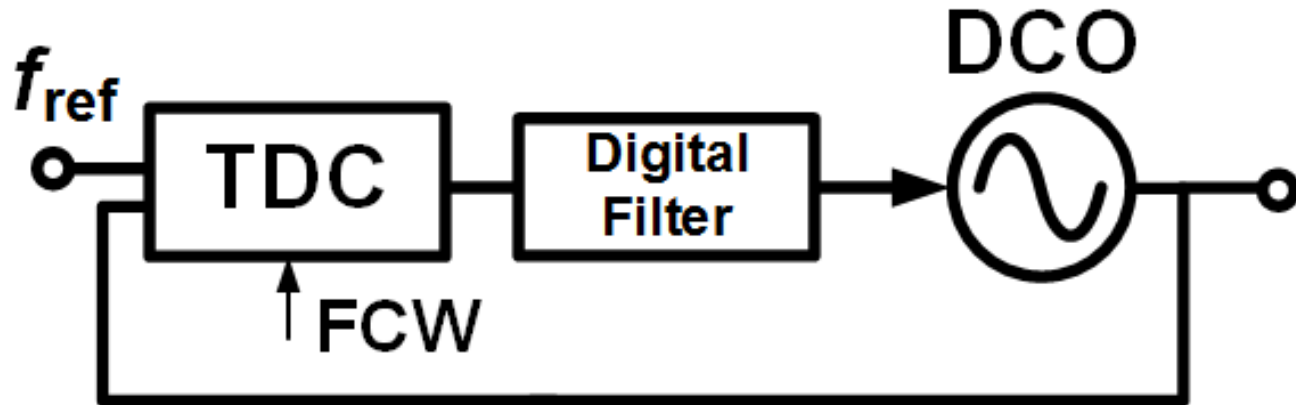
- ☺ – **Taking advantages of digital circuits**
- ☺ – **Compact chip area**
- ☹ – **Cannot fully utilize digital design flow**
  - **Layout uncertainty caused by Auto Place & Route degrades TDC and DCO linearity.**

Injection Locking Technique

Free-running VCO

Injection locked

800MHz

100MHz

REF   Injection locked

$$f_{\mathrm{in}} = \frac{\sqrt{6/(N(N-1))}}{2\pi} \cdot f_{\mathrm{ref}}$$

Phase noise

Offset Frequency

[N.D. Dalt, TCAS II 2014]

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Phase Noise Comparison

- Jitter$_{TDC-PLL}$=**6.4**ps   Jitter$_{IL-PLL}$=**1.5**ps

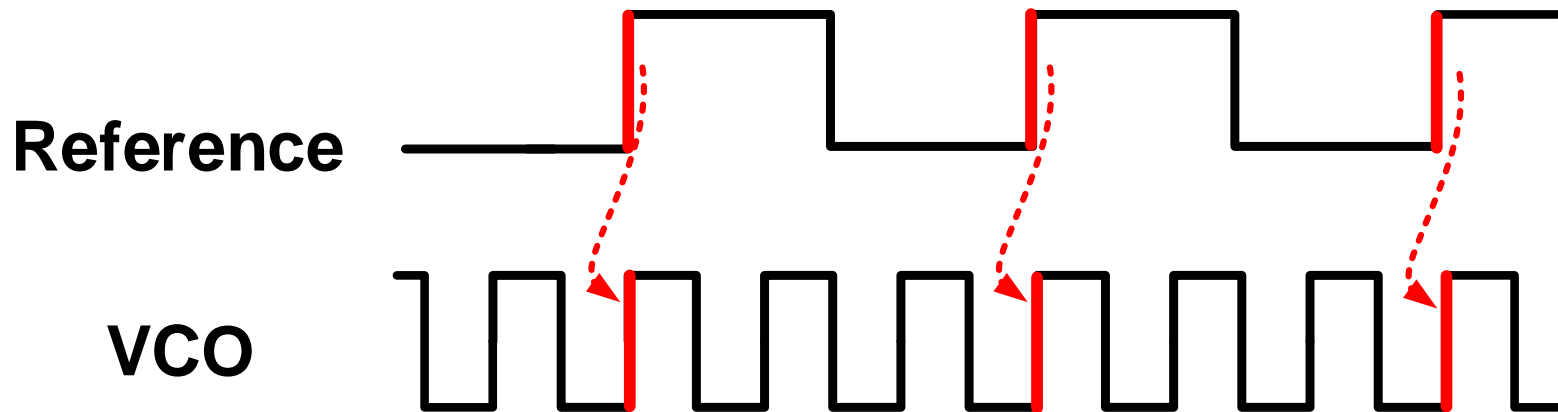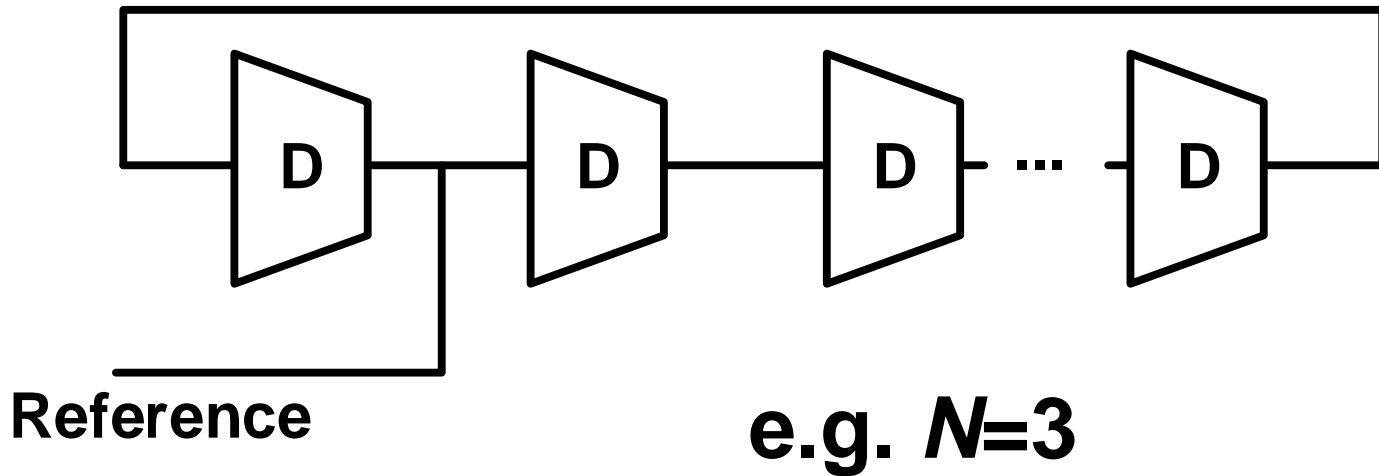*14.1: A 0.048-mm^2 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique*

Injection Method

- ## Pulse Injection [B. Helal, *et al.*, JSSC 2009]
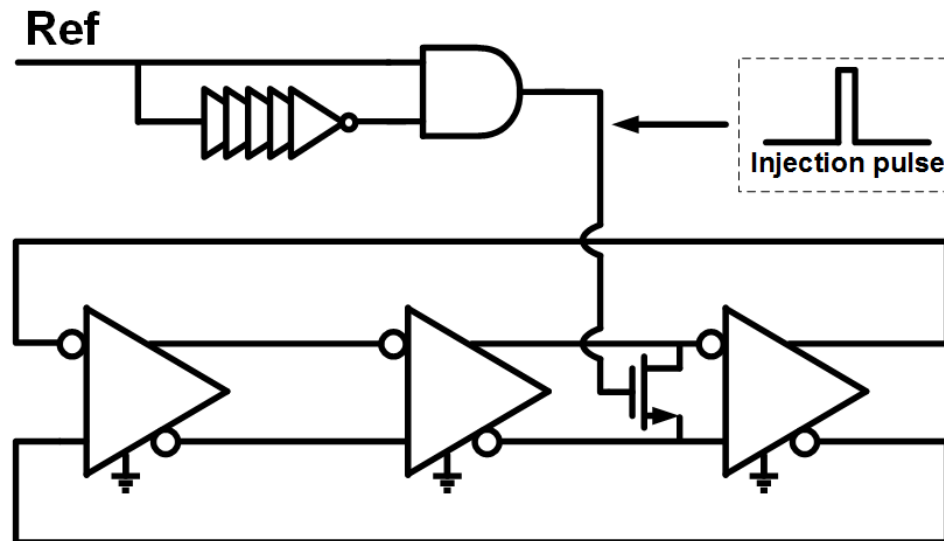
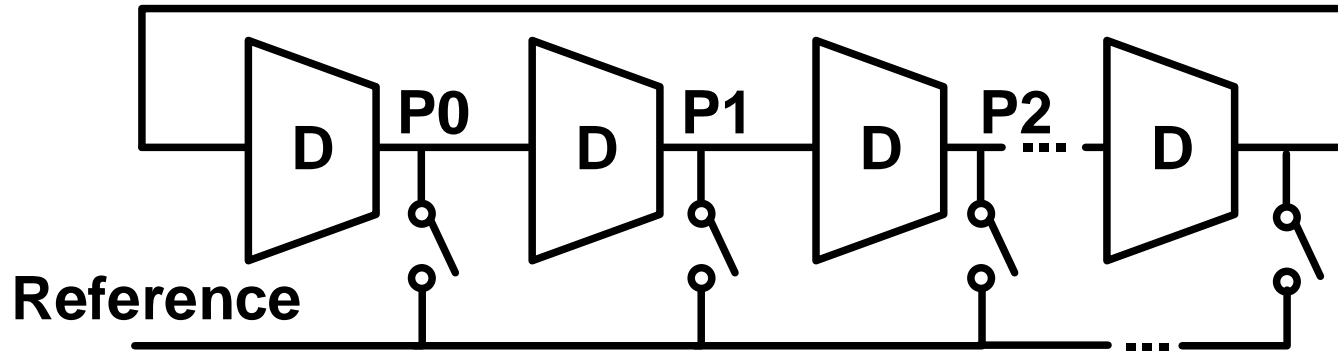- ## Multiplying DLL [S. Ye, *et al.*, JSSC 2002]
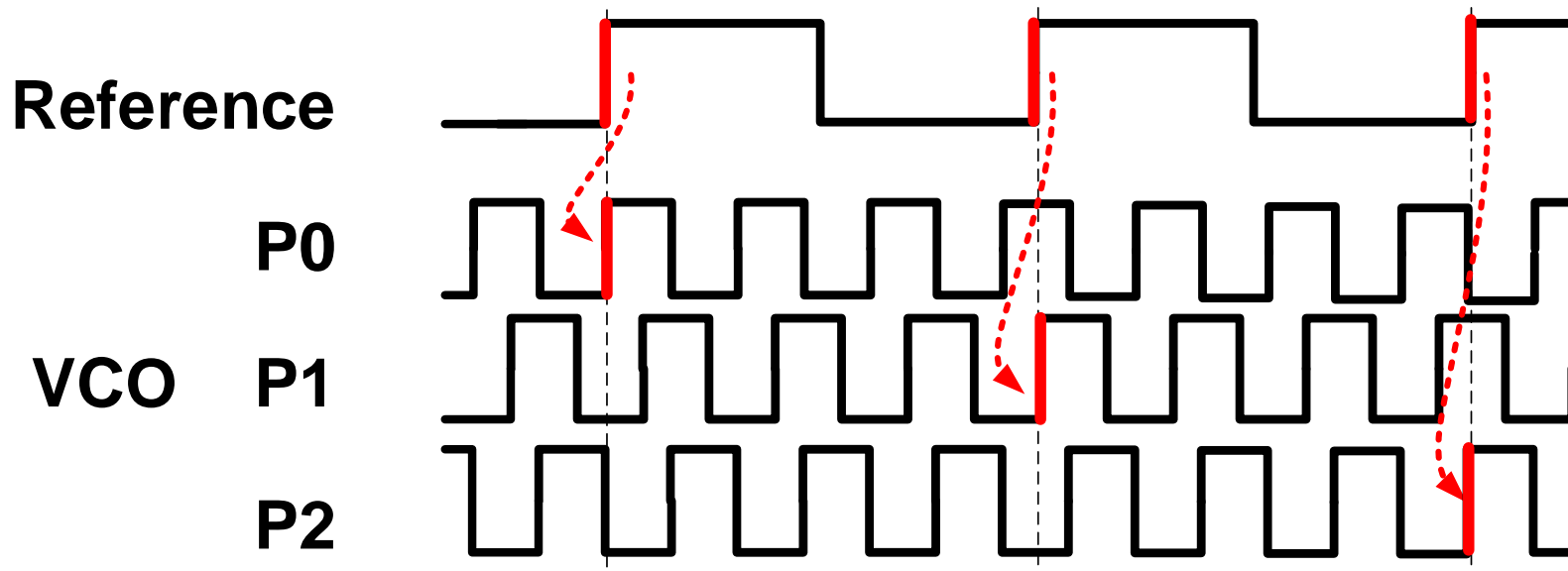
- ## Edge Injection [W. Deng, *et al.*, ISSCC 2014]
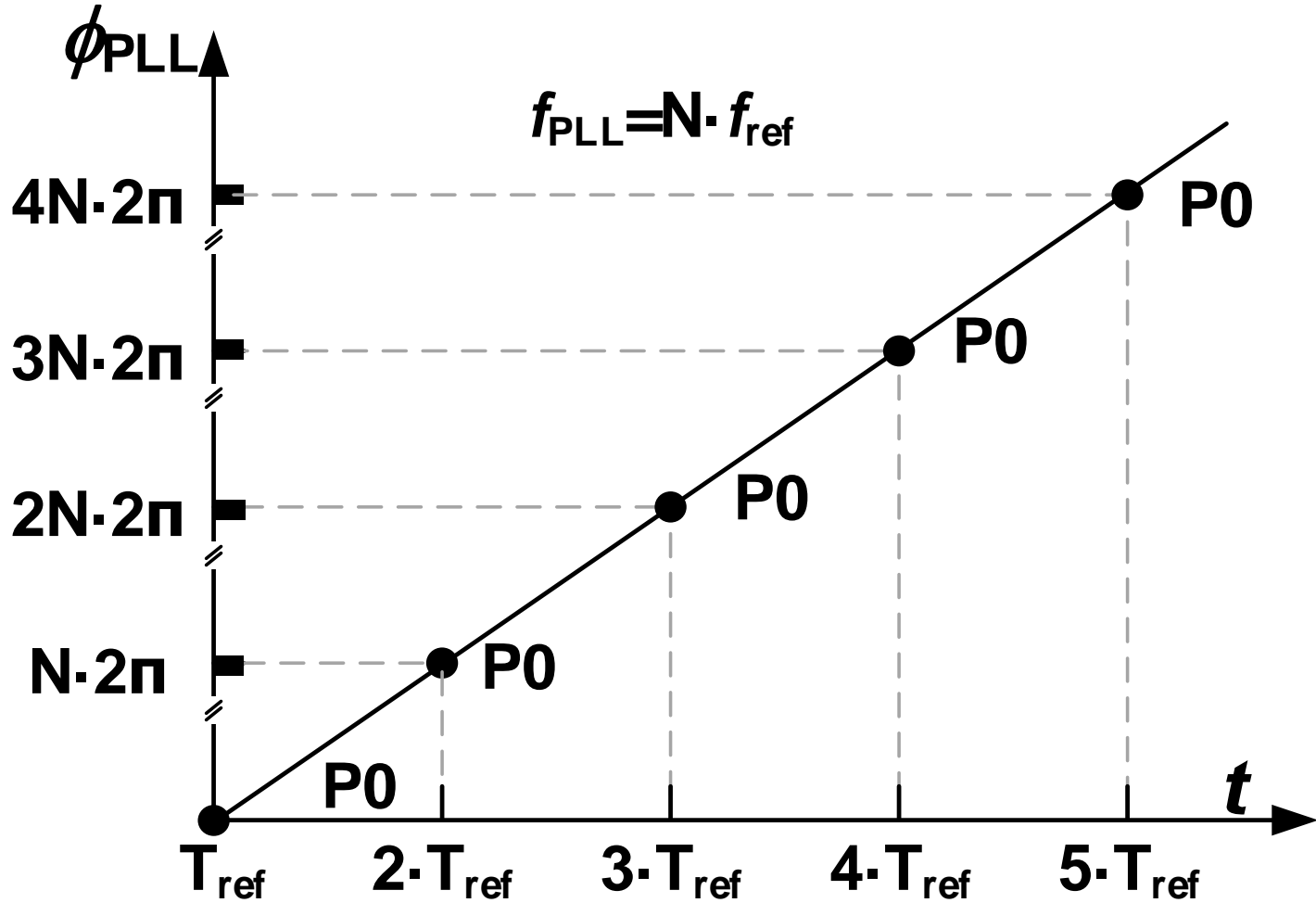
Integer-*N* Operation

Reference

e.g. *N*=3

Reference

VCO

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Sub-Integer-*N* Operation

e.g. *N*=3+(1/M)

[P. Park, *et al.,* ISSCC 2012]

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Phase Domain (Integer-*N*)

$f_{PLL} = N \cdot f_{ref}$

P0 → P0 → P0 → P0 → P0 → P0 → P0 …

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Phase Domain (Sub-Integer-*N*)

$$f_{PLL} = (N + 1/M) \cdot f_{ref}$$

ϕ_{PLL}

$4 \cdot (N+1/M) \cdot 2\pi$ — P4

$3 \cdot (N+1/M) \cdot 2\pi$ — P3

$2 \cdot (N+1/M) \cdot 2\pi$ — P2

$(N+1/M) \cdot 2\pi$ — P1

P0

T_{ref} $2 \cdot T_{ref}$ $3 \cdot T_{ref}$ $4 \cdot T_{ref}$ $5 \cdot T_{ref}$ *t*

P0 → P1 → P2 → P3 → … → P0 → P1 …

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Phase Domain (Fractional-*N*)

$$f_{PLL}=(N+\textcolor{red}{0.5}/M)\cdot f_{ref}$$

ϕ_{PLL}

$(4\cdot N+2/M)\cdot 2\pi$ — P2

$(3\cdot N+1/M)\cdot 2\pi$ — P1

$(2\cdot N+1/M)\cdot 2\pi$ — P1

$N\cdot 2\pi$ — P0

P0

T_{ref} $2\cdot T_{ref}$ $3\cdot T_{ref}$ $4\cdot T_{ref}$ $5\cdot T_{ref}$ *t*
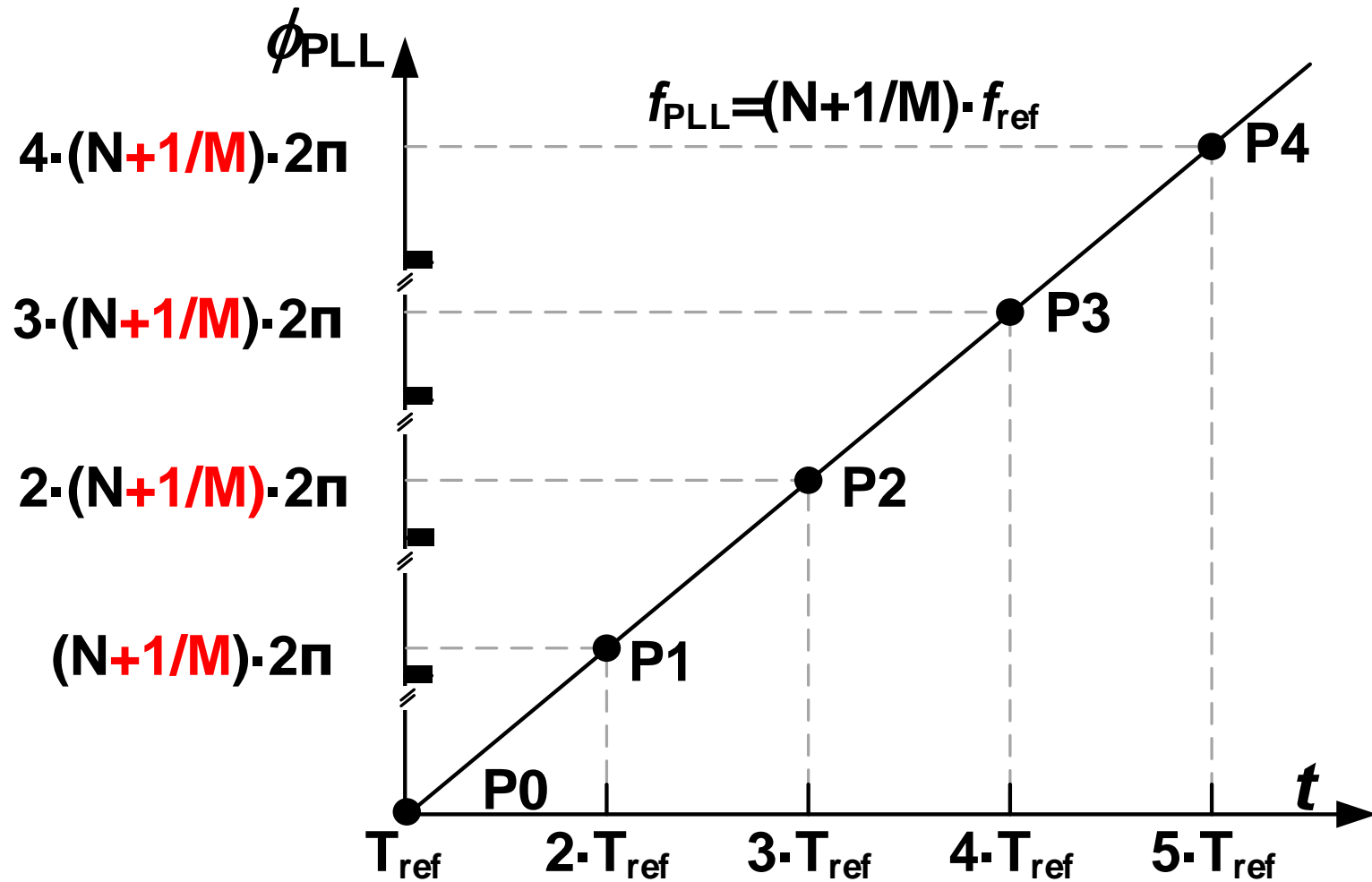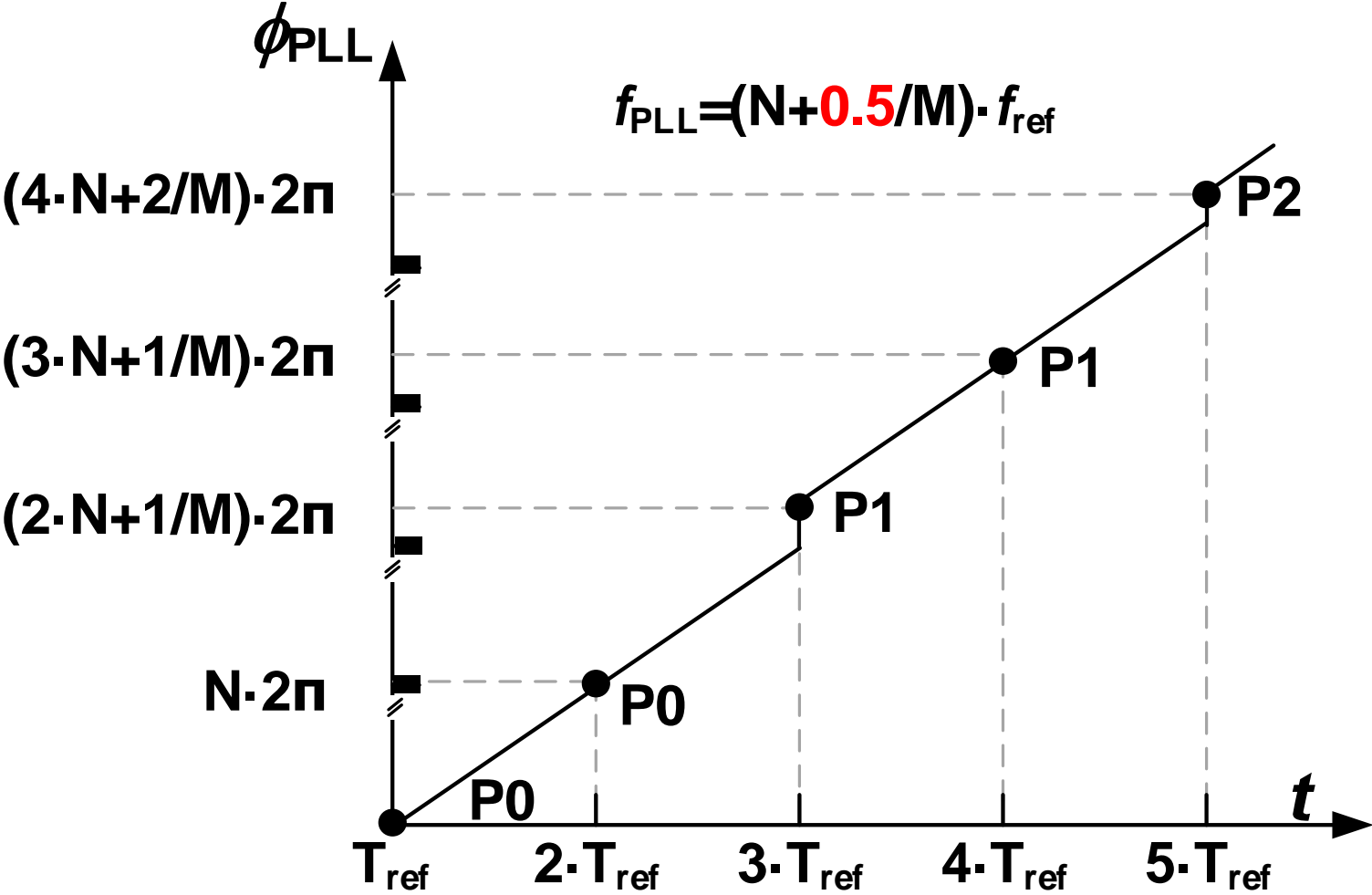
P0 → P0 → P1 → P1 → P2 → P2 → P3 …

Time Domain (Fractional-*N*)
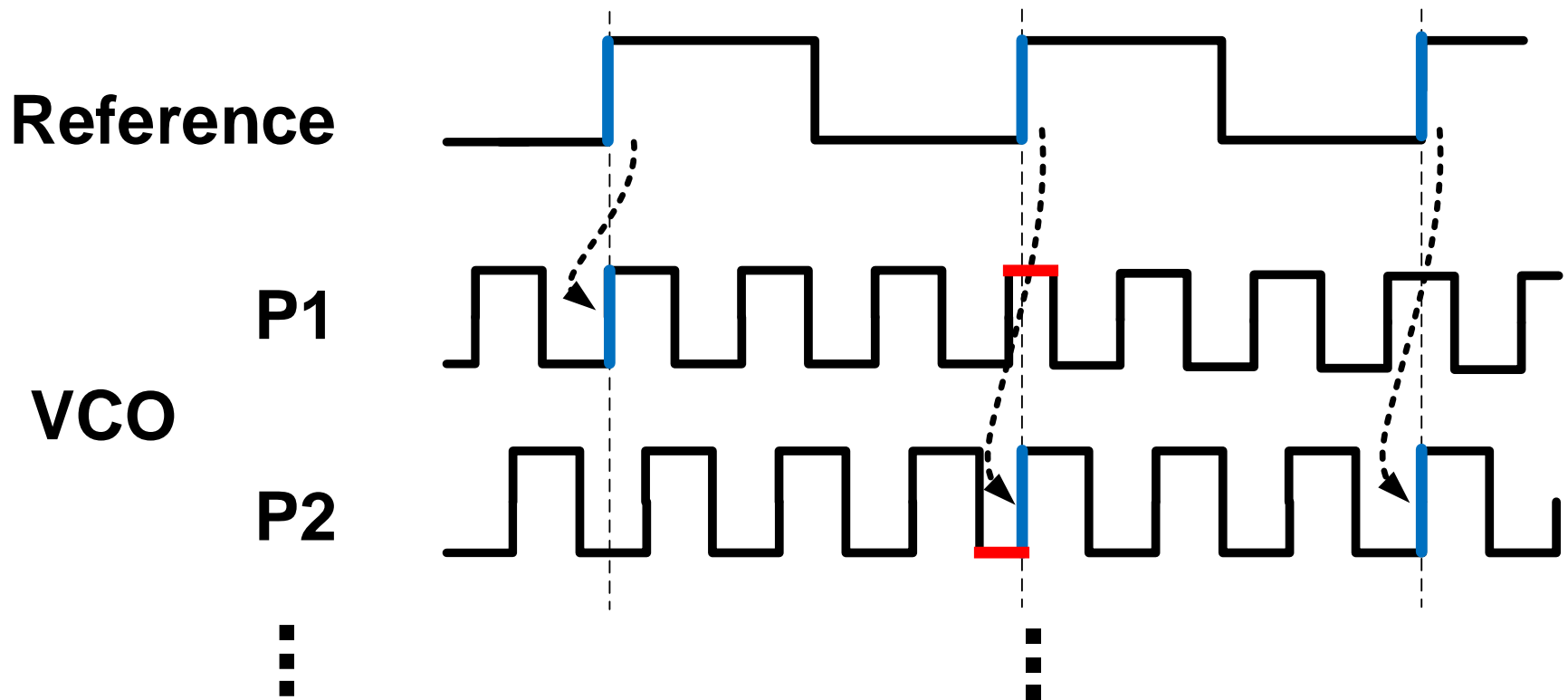
- **Spur is caused by "hard" switching**

Proposed Soft Injection

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique
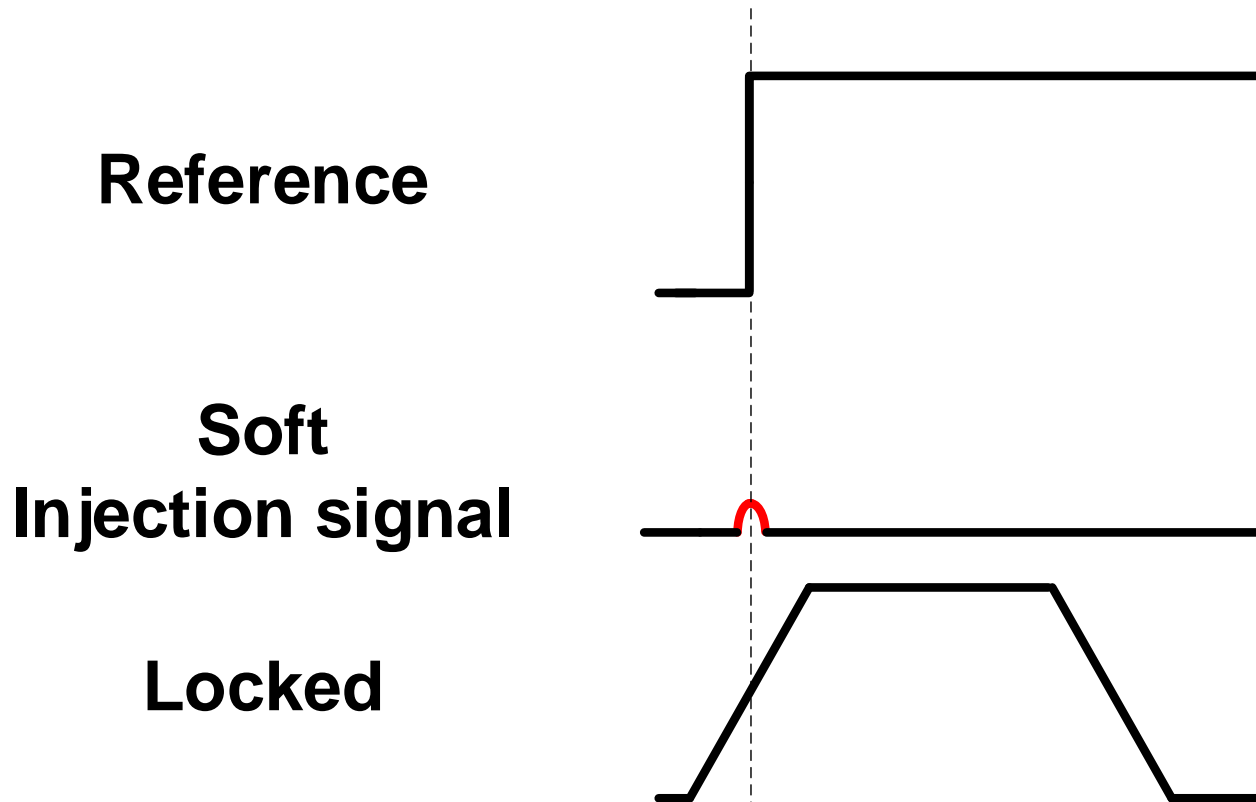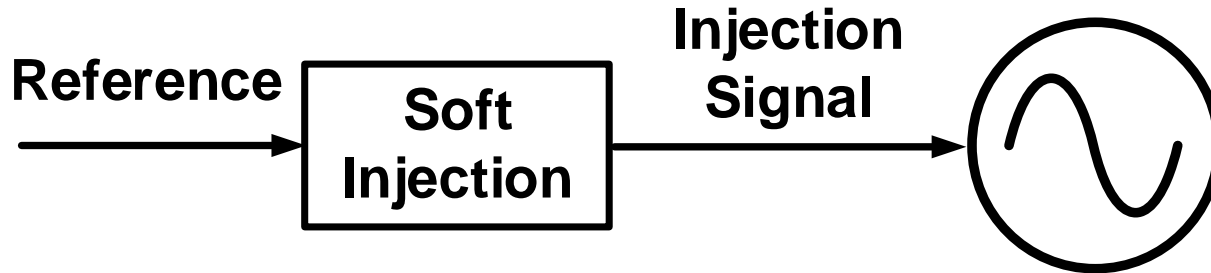
"Hard" vs "Soft" Injection

Injection at ϕ_0   **Injection at ϕ_{10}**

Reference

ϕ_{10} w/o inj

ϕ_{10} w/ inj

Conventional "hard" injection

Soft injection

ϕ_{10} w/o inj

ϕ_{10} w/ inj

Proposed "soft" injection

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Injection Strength

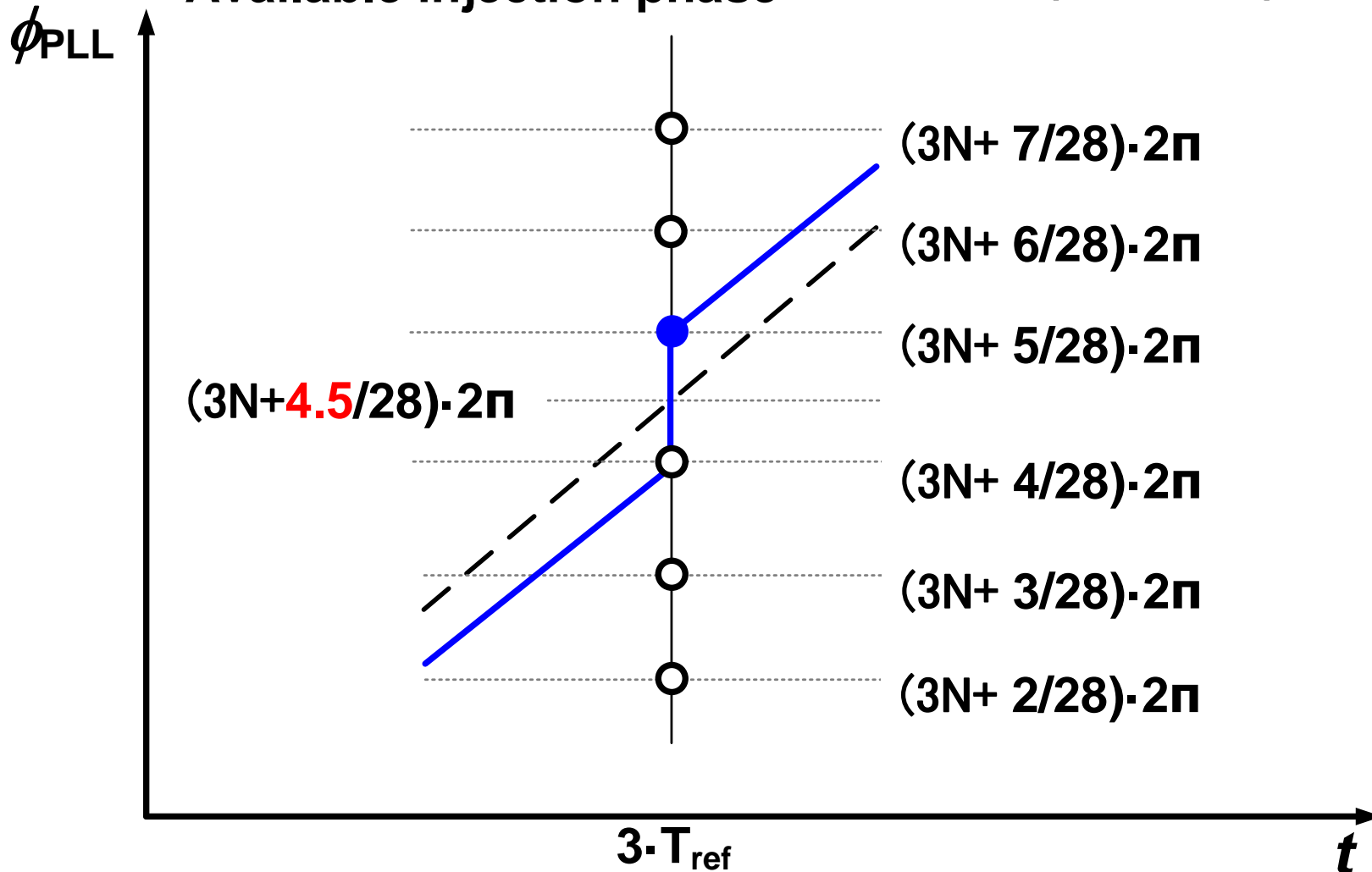- **Soft injection signal level determines injection strength**
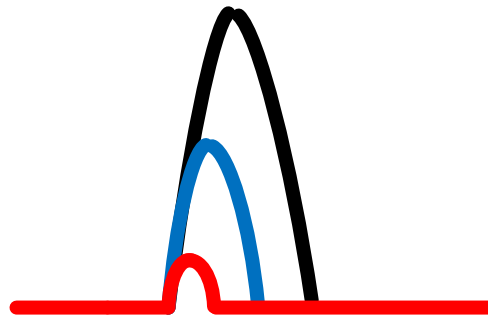
Soft Injection Signal

- **Stronger injection strength leads to larger phase shift**

Fractional-*N* Operation (Hard)

● **Selected injection phase**
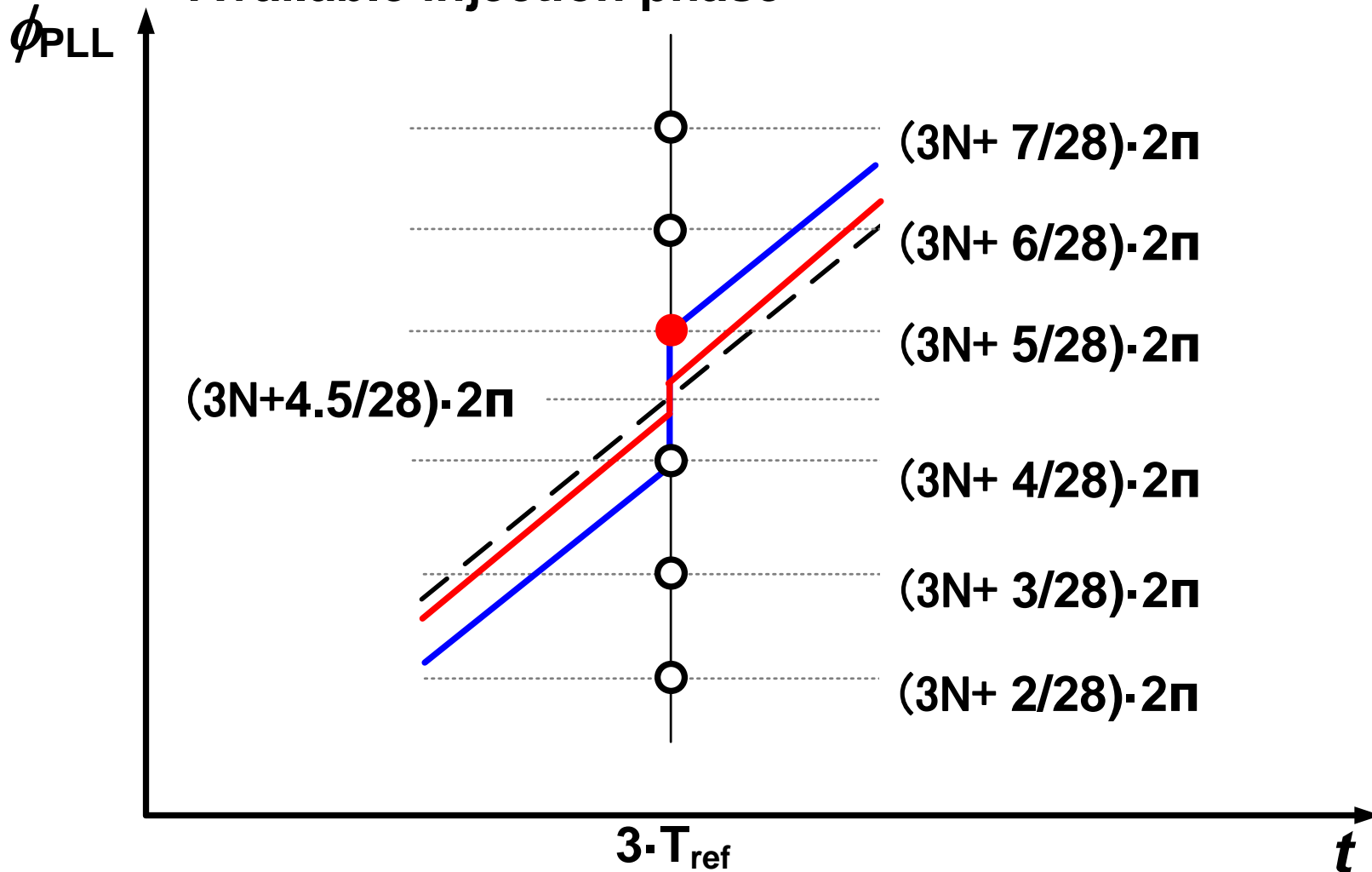○ **Available injection phase**

$f_{PLL} = (N + 1.5/28) \cdot f_{ref}$

$(3N + 7/28) \cdot 2\pi$

$(3N + 6/28) \cdot 2\pi$

$(3N + 5/28) \cdot 2\pi$

$(3N + 4.5/28) \cdot 2\pi$

$(3N + 4/28) \cdot 2\pi$

$(3N + 3/28) \cdot 2\pi$

$(3N + 2/28) \cdot 2\pi$

ϕ_{PLL}

$3 \cdot T_{ref}$

t

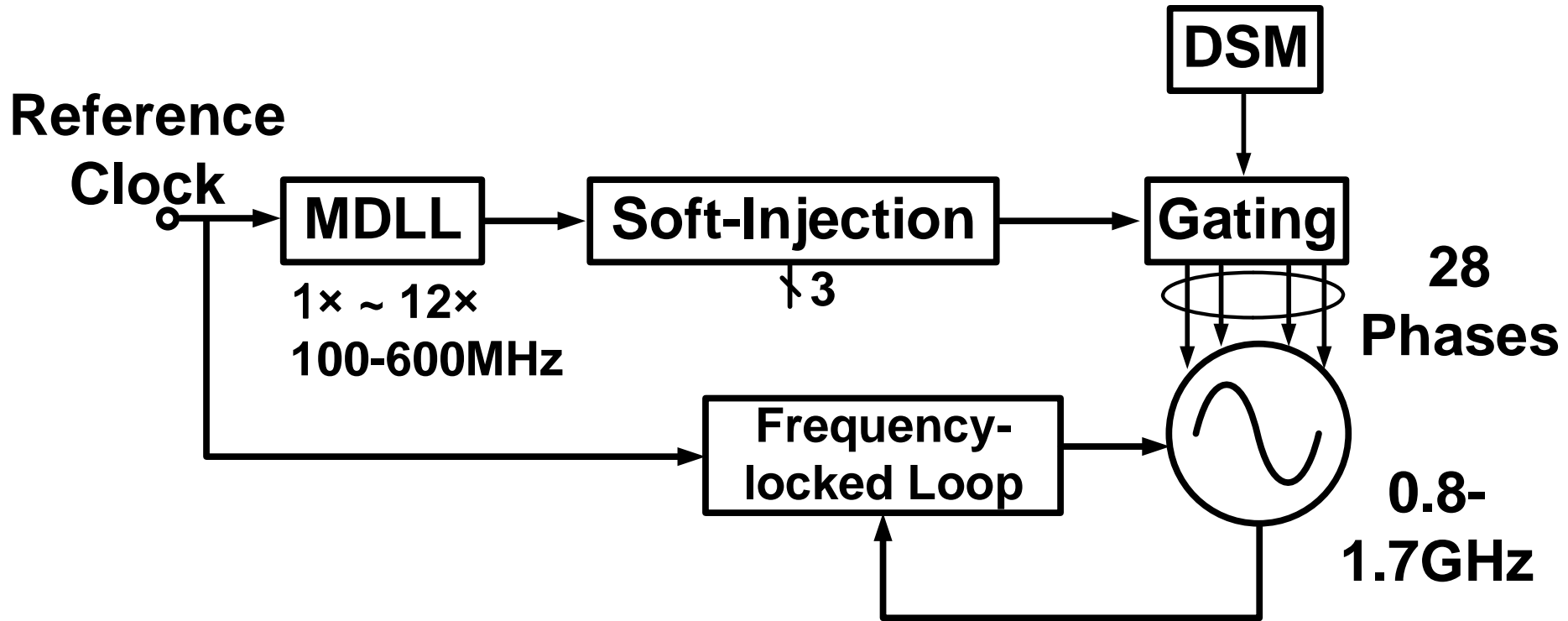*14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique*

Fractional-*N* Operation (Soft)

- ● **Selected injection phase**
- ○ **Available injection phase**

$f_{PLL} = (N + 1.5/28) \cdot f_{ref}$

ϕ_{PLL}

$(3N + 7/28) \cdot 2\pi$

$(3N + 6/28) \cdot 2\pi$

$(3N + 5/28) \cdot 2\pi$

$(3N + 4.5/28) \cdot 2\pi$

$(3N + 4/28) \cdot 2\pi$

$(3N + 3/28) \cdot 2\pi$

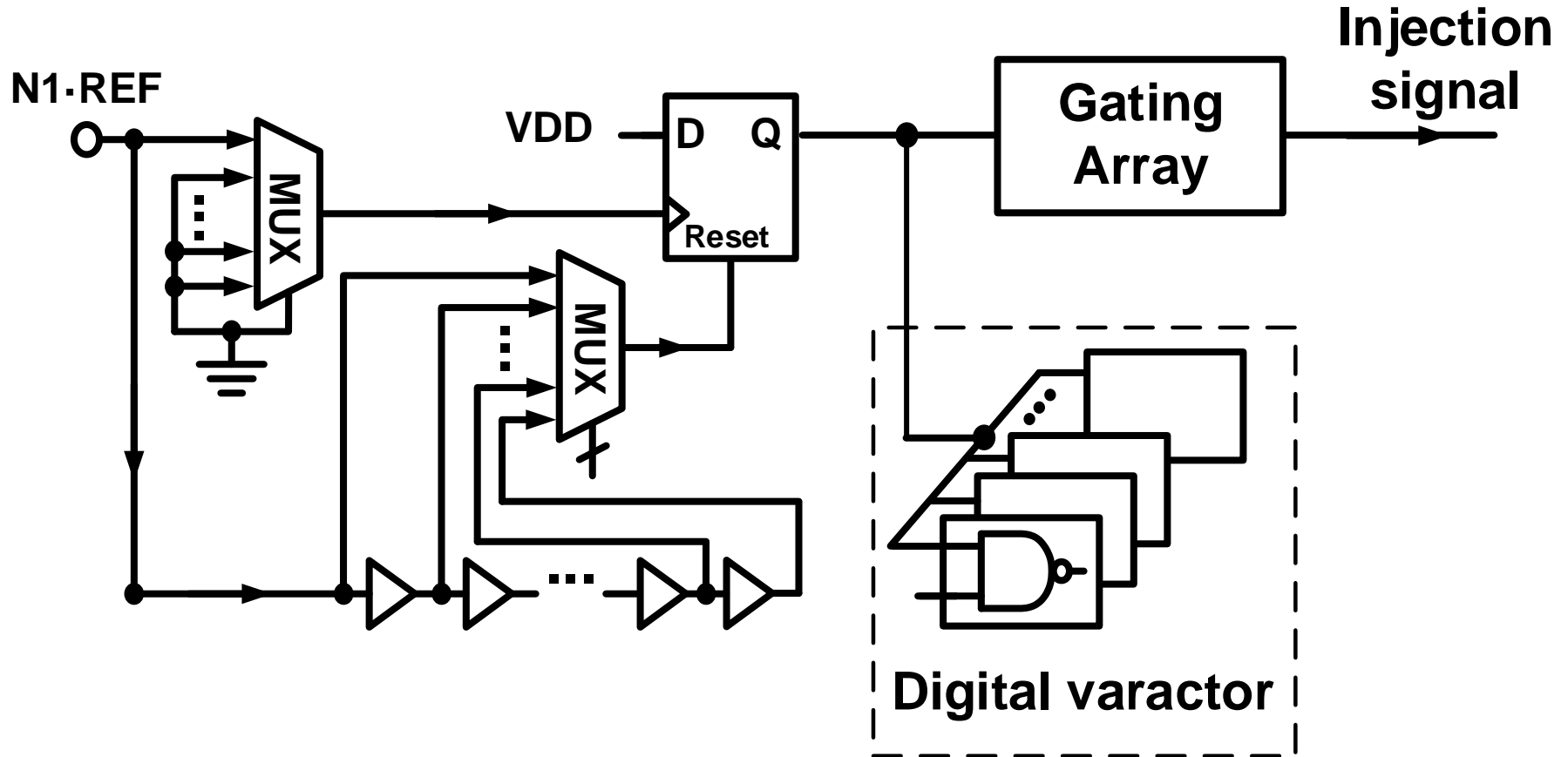$(3N + 2/28) \cdot 2\pi$

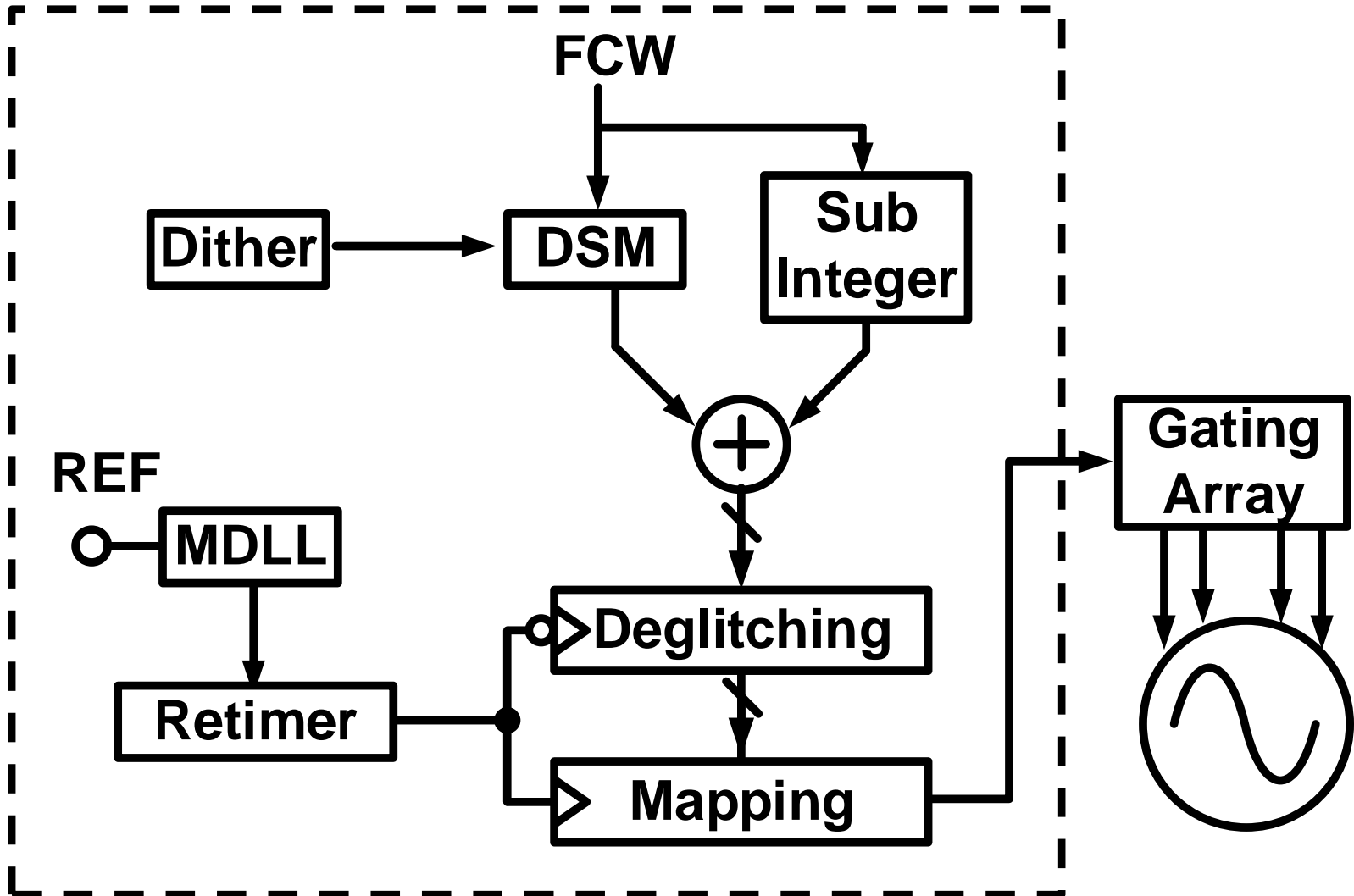$3 \cdot T_{ref}$

t

PLL with Soft Injection

- **Cascading topology**

Soft Injection Generator

- **<u>Effective soft injection signal</u> is generated by soft injection generator and gating array.**
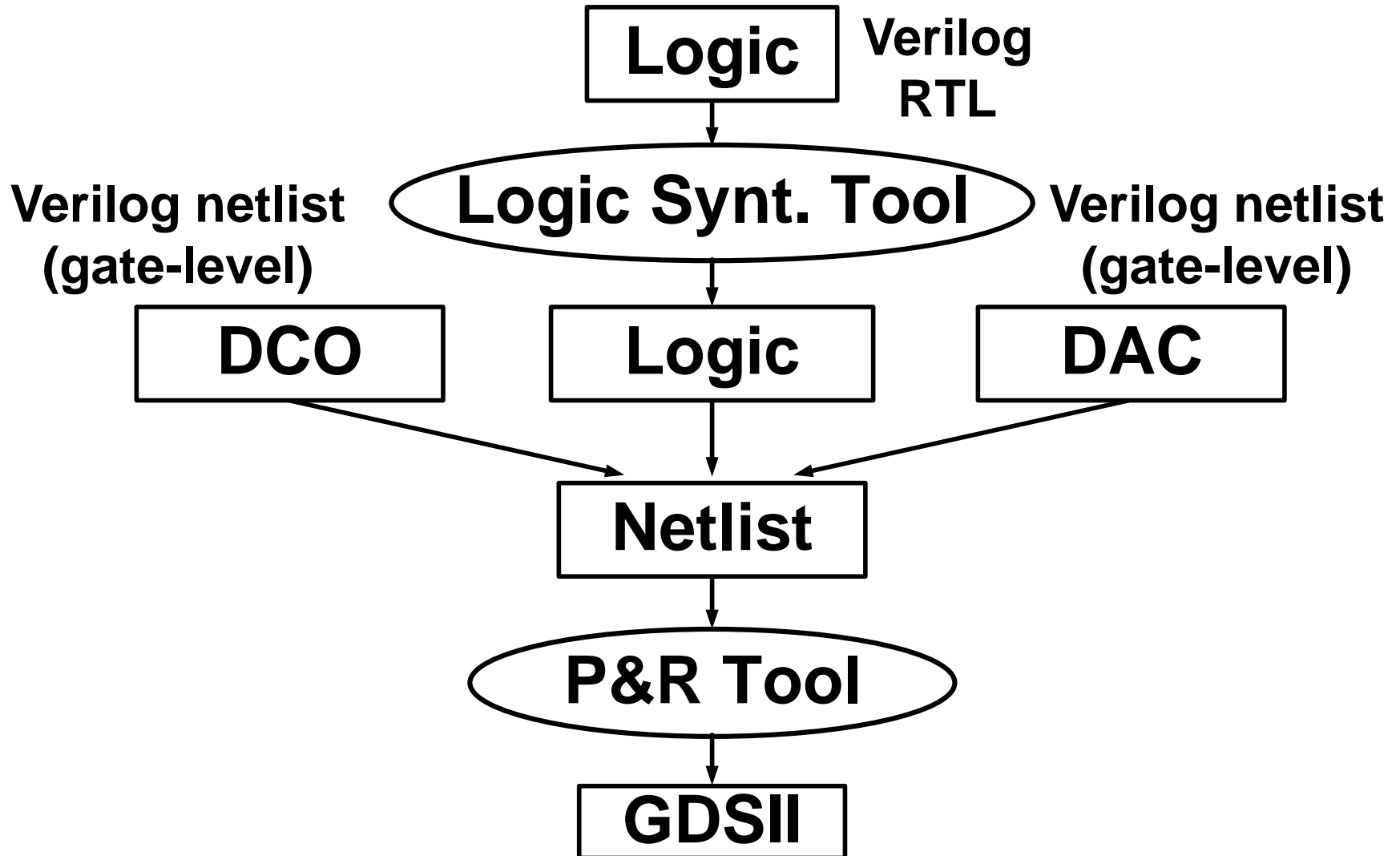
14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Fractional-*N* Controller

Gating Array

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Interpolative phase coupled DCO

- **Standard cell design**

- **Interpolative phase coupling for accurate phase**

[W. Deng, *et al.,* ISSCC 2014]

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique
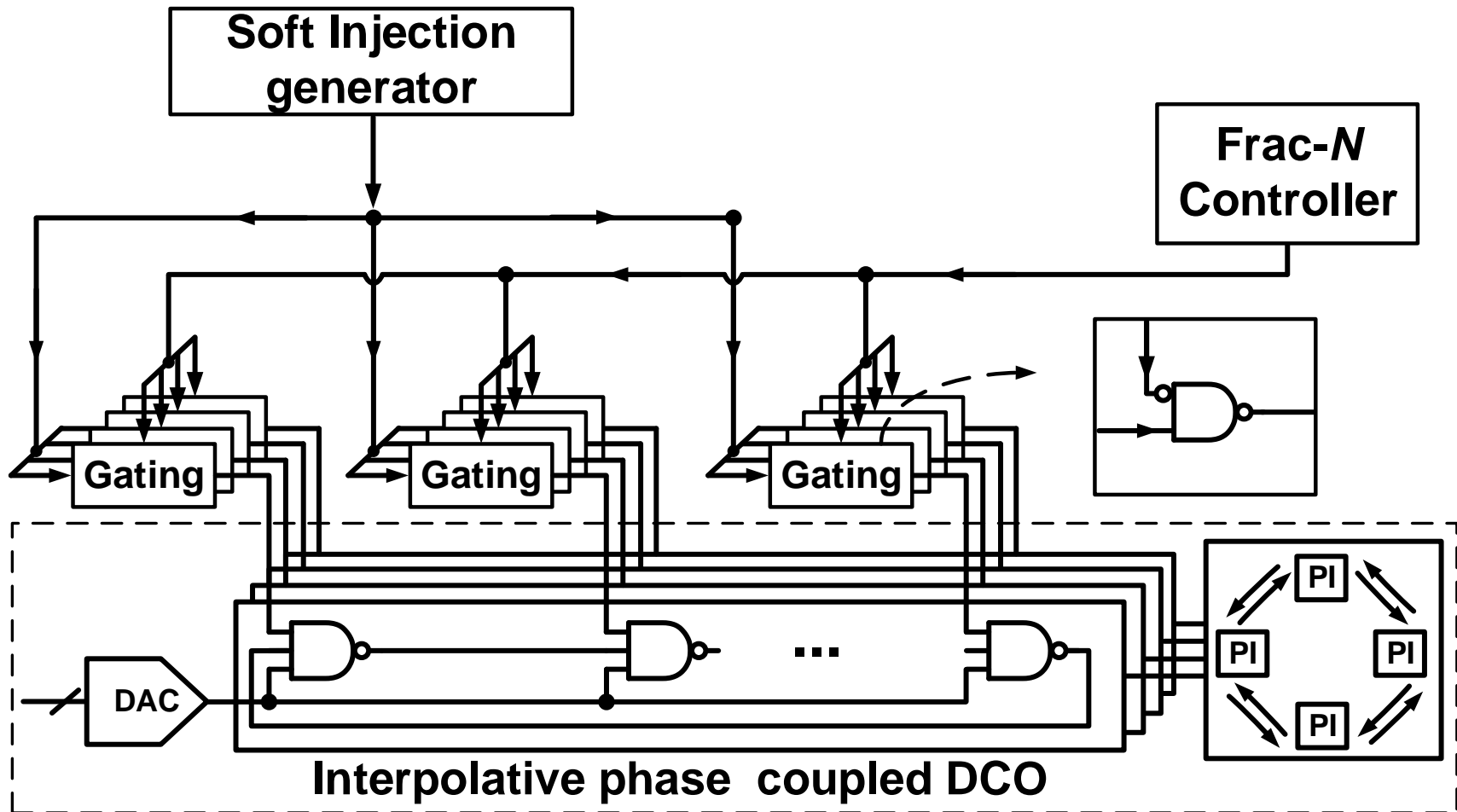
Design Procedure

Chip Microphotograph

65nm CMOS technology

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Phase Noise

Frequency: 1.2576 GHz
Integrated Jitter: 2.5 ps
P_{DC}: 2.9 mW
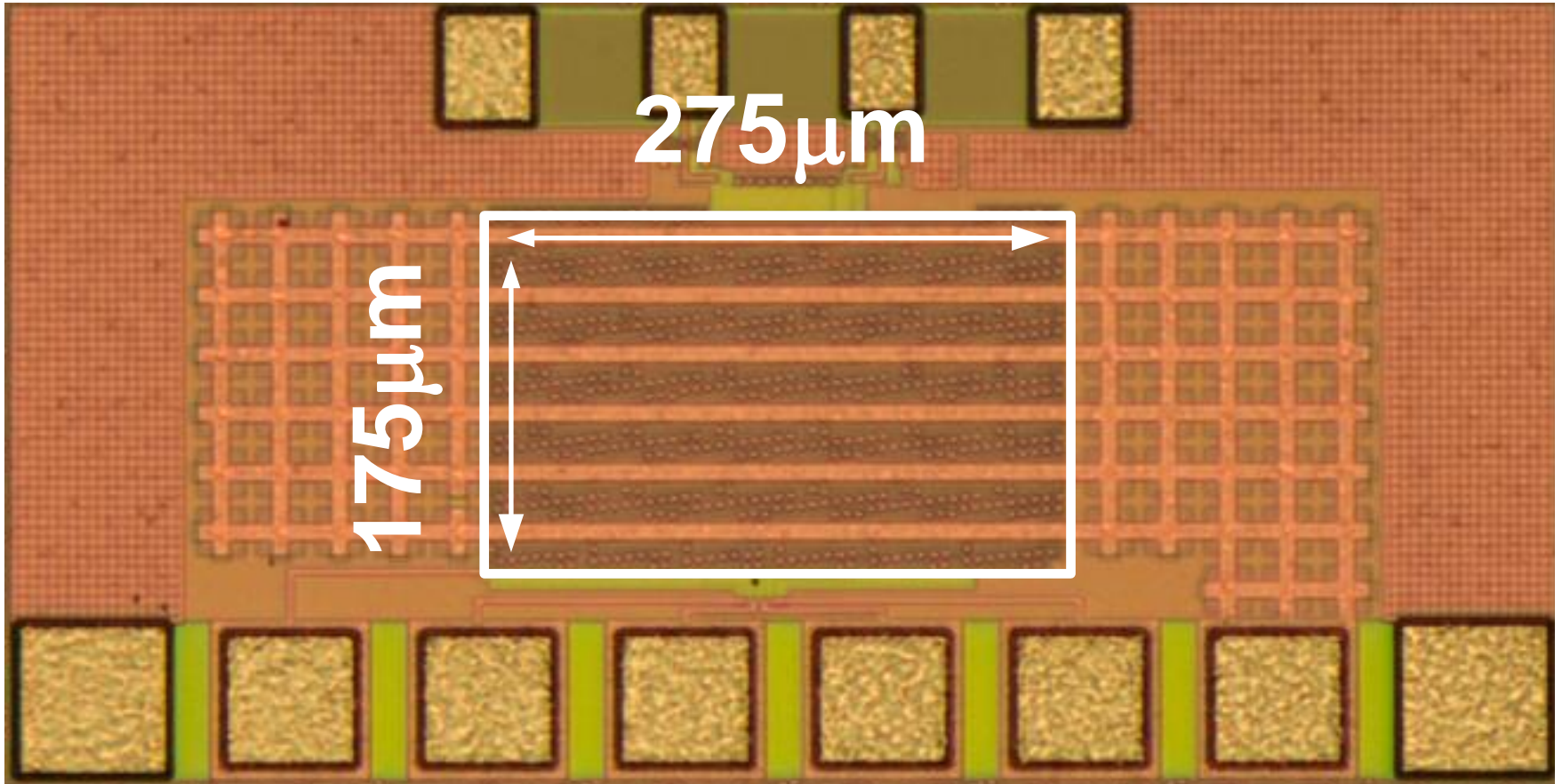
14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique
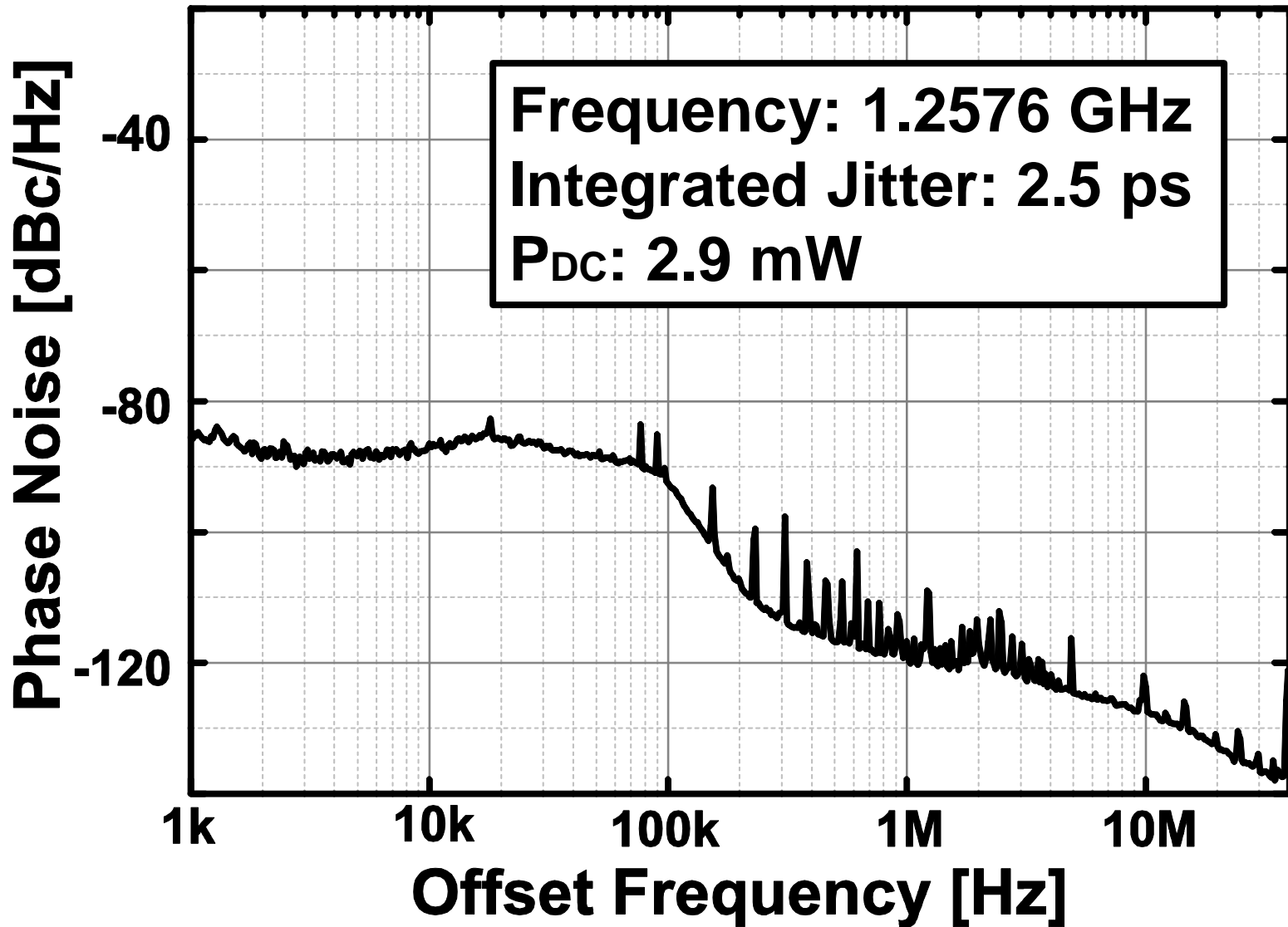
Spur against Inj. Strength

Jitter against Inj. Strength

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique
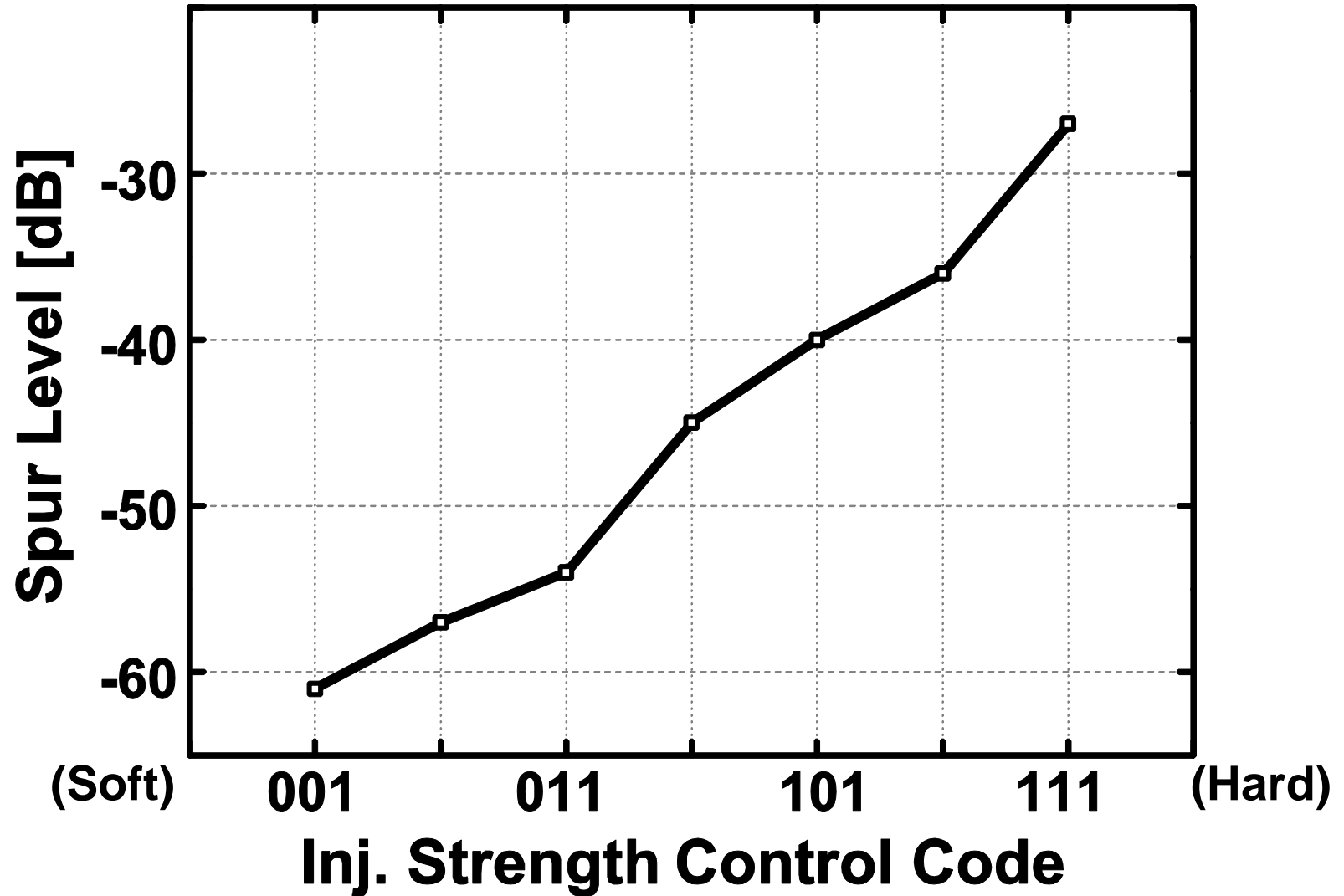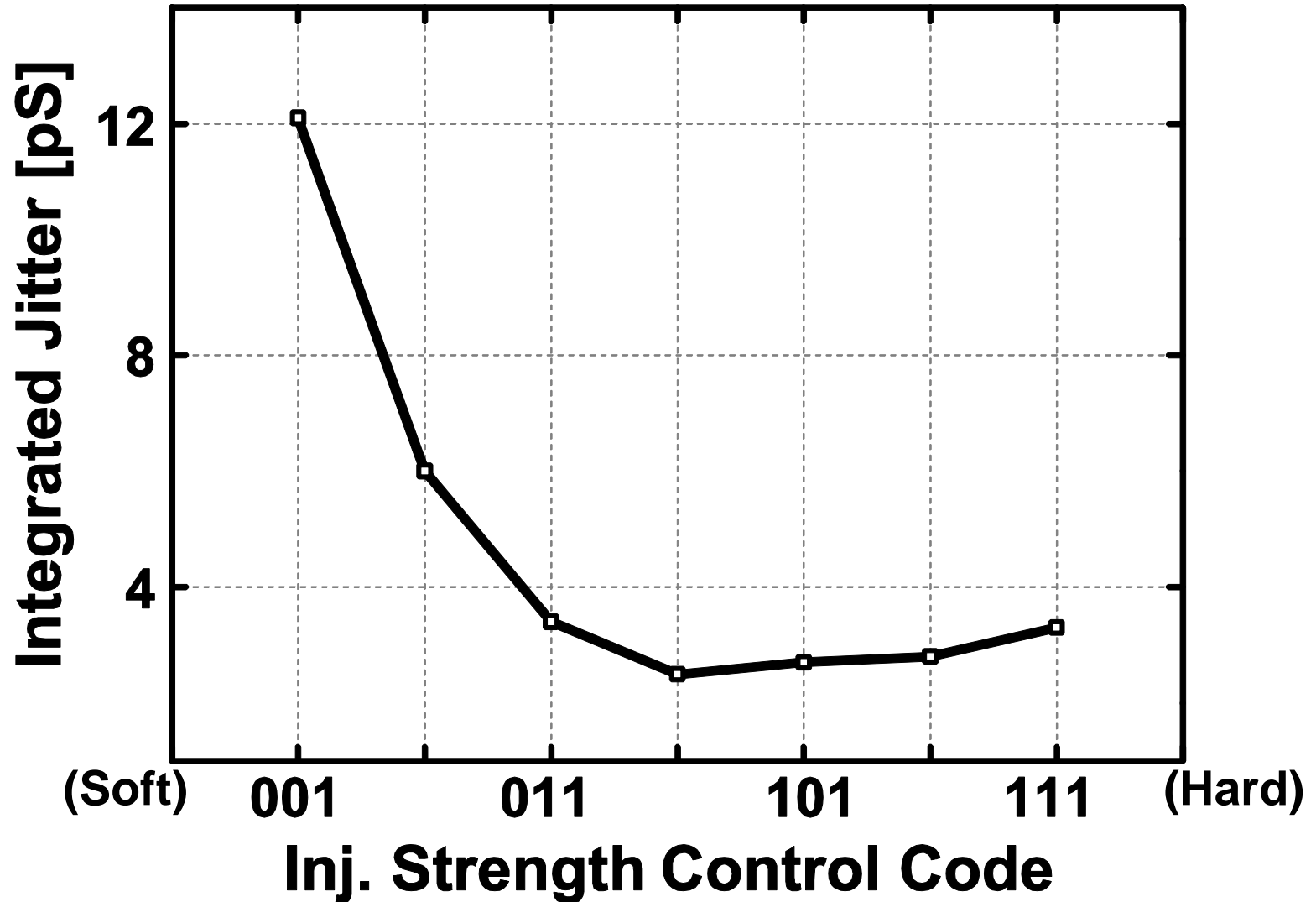
Comp. of Synthesizable PLLs

	This work	[1]	[2]
Technology	65nm	65nm	65nm
Power [mW]	2.9 @1.2576GHz	0.78 @0.9GHz	13.7 @2.5GHz
Area [mm²]	0.048	0.0066	0.04
Integ. Jitter [ps]	2.5	1.7	3.2*
FOM [dB]	-227	-237	-219*
Topology	Soft-IL	IL	TDC-based
Type	Frac-*N*	Integer-*N*	
Synthesized?	YES		

*FOM is calculated based on RMS jitter.

[1] W. Deng, *et al.*, ISSCC 2014 [2]Y. Park, *et al.*, CICC 2011

14.1: A 0.048-mm² 3-mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

Performance Comparison
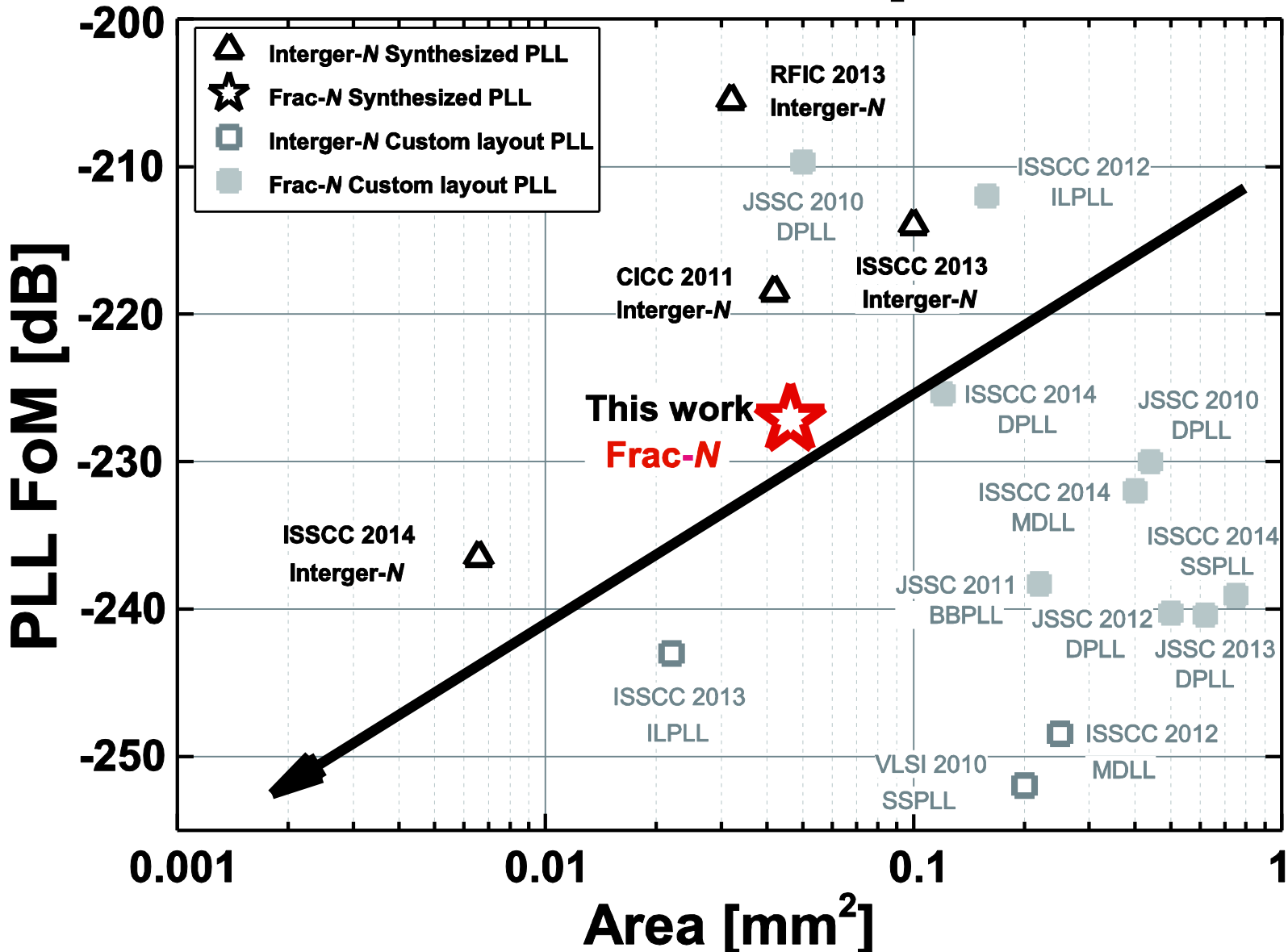
Conclusion

- **A synthesizable fractional-*N* PLL with a soft-injection locking technique is presented.**

- **The soft injection locking technique provides potentials for future clock generation circuit designs.**

Acknowledgement

This work is partially supported by STARC, MIC, SCOPE, MEXT, STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc.