

14.1 A 0.048mm² 3mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique

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Phase-locked loops (PLLs) are a crucial building block in modern Systems-on-Chip (SoCs), which contain microprocessors, I/O interfaces, memories, power management, and communication systems. Fully synthesizable PLLs [1-2], designed using a pure digital design flow, have been proposed to reduce the design cost and allow easier integration. To achieve high-frequency resolution, PLLs are required to operate in fractional- N mode, in addition to integer- N mode. There are several architectures available [5-6] for realizing fractional- N operation. However, the existing topologies are not well suited for synthesis, as they require a time-to-digital converter (TDC) [3] and a digital-to-time converter (DTC) [4-5]. TDCs and DTCs are vulnerable to layout uncertainty, arising from automatic place and route (P&R), introducing linearity degradation and leading to poor in-band and out-of-band phase noise in PLLs. Injection locking is a promising technique for synthesizable PLLs. Unfortunately, it suffers from large spur caused by a periodic hard refresh, and limited fractional resolution, which is bounded to the inverse of the number of ring oscillator delay stages [6]. This paper describes a fully synthesizable fractional- N PLL with a soft injection-locking technique for smoothing switching and fine fractional resolution, and a cascading topology for suppressing the free-running oscillator phase noise over a wide loop bandwidth.

Figure 14.1.1 shows a block diagram of the two-stage fractional- N PLL incorporating the soft injection-locking technique. The PLL comprises a first-stage PLL, a second-stage PLL, a soft-injection generator, gating circuits, and a fractional- N controller. All of the circuits shown, including the soft-injection circuit and the digitally controlled oscillator (DCO), are designed and implemented using a digital design flow without any manual manipulation. The first-stage PLL is constructed with an integer- N digital multiplying delay-locked loop (MDLL), which generates a low-phase-noise high-frequency injection signal from a clean external reference source. The second stage is a dual-loop PLL that further boosts the output frequency from several hundred MHz to a few GHz. With a high injection frequency and a small multiplication factor in the second stage, the noise contributed by the oscillator in the second PLL is minimized, since it can be suppressed over a much wider loop bandwidth. The soft-injection circuitry helps to reduce the spur caused by injection locking. The high-resolution fractional- N operation is achieved using the gating circuit together with the fractional- N controller, described below.

Conventionally, multiplexing a clean edge from a reference clock periodically replaces an oscillator's noisy edge, causing the oscillator edge to be aligned with the reference clock, removing accumulated jitter. Since the phase replacement and alignment are done in one reference cycle, this injection method is referred to as "hard" switching. Unfortunately, the conventional injection-locking technique is limited to integer- N and sub-integer- N frequency multiplication (if a multi-phase oscillator is available). In this work, fractional- N operation is achieved by dynamically selecting one of the oscillator phase edges ($\phi_0 - \phi_{27}$) at every reference cycle, which is forced to be aligned with the reference edge in the case of conventional "hard" switching. The phase difference between the reference clock and target injecting-oscillator edge, which is introduced by a delta-sigma modulator (DSM), will be eliminated by the phase replacement and alignment operation. However, the consequent "hard" refresh operation leads to a large spur, degrading deterministic jitter. Reduced spur can be achieved via a "soft" injection technique, which causes the injected oscillator edge to be "pulled toward" the position of the injected reference edge, as shown in Fig. 14.1.2. As a result, the resetting procedure is smoother, leading to lower spur. Note, however, that the "soft" injection approach may degrade injection efficiency. This issue is addressed by using a higher injection frequency, which maintains a sufficient injection-loop bandwidth for suppressing the phase noise of the free-running oscillator.

Figure 14.1.3 shows the locking transients of the oscillator using conventional "hard" injection and the proposed "soft" injection technique. In this design, the target reference-injected delay stage number is determined by logical operations of sub-integer- N controller output, D_{sub} , and DSM output D_{DSM} . A weak injection signal, originating from the reference clock, directly feeds the oscillator without a hard refresh operation.

Figure 14.1.4 shows the block diagram of the oscillator in the second-stage PLL, the fractional- N controller, the gating array, and soft-injection circuitry. Note that because the oscillator is built using four 7-stage oscillators coupled with phase interpolators, there are total twenty-eight unit gating circuits, corresponding to the total number of delay stages. A 16b DSM produces an effective fractional time resolution of $T_{\text{DCO}}/(28 \cdot 2^{16})$, where T_{DCO} is the period of the DCO. The correct phase sequence and injection timing for fractional- N operation are guaranteed by mapping, de-glitching, and retiming circuitry in the fractional- N controller. The gating function is realized by an array of NAND logic gates. An input to each NAND gate is connected to the output of the soft-injection circuit and the other inputs are connected to the fractional- N controller. The soft-injection signal is generated by a digitally controlled rectangle pulse generator, digital varactors [1], and the corresponding gating circuit.

The proposed fractional- N PLL has been synthesized and fabricated in a 65nm digital CMOS process and occupies a core area of $275\mu\text{m} \times 175\mu\text{m}$. Analog blocks, including DCOs, are registered as macro cells during P&R to minimize routing uncertainty. The phase-noise characteristic is evaluated using a signal-source analyzer (Agilent E5052B) and the spectrum is measured by using a spectrum analyzer (Agilent E4407B). Fig. 14.1.5 shows the measured phase noise and spectrum at 1.5222GHz output with a 380MHz reference clock. The phase noise maps to a 3.6ps integrated jitter (from 1kHz to 100MHz). The measured results show a frequency tuning range from 0.8 to 1.7GHz. At a 1.5222GHz output frequency, the power consumption is 3mW, excluding output buffers, with a 0.8V power supply.

Figure 14.1.6 summarizes the measured performance and compares this work with state-of-the-art digital PLLs. The synthesizable fractional- N PLL in this paper offers comparable performance in terms of power, jitter, and area. The typical figure of merit (FoM) is -224.6dB at the output frequency of 1.5222GHz, where FoM is defined as $10\log[(\sigma_j/1\text{s})^2 \cdot (P_{\text{DC}}/1\text{mW})]$, such that σ_j is the integrated jitter, and P_{DC} is the DC power consumption. The fully synthesizable two-stage fractional- N PLL uses little area and provides low-jitter clock generation.

To summarize, this paper has presented a fractional- N PLL with a soft-injection-locking technique, designed using standard digital design flows. The chip micrograph of the synthesized PLL is shown in Fig. 14.1.7.

Acknowledgments:

This work is partially supported by STARC, MIC, SCOPE, MEXT, STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc.

References:

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- [6] P. Pyoungwon, *et al.*, "An All-Digital Clock Generator Using a Fractionally Injection-Locked Oscillator in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 336-337, 2012.

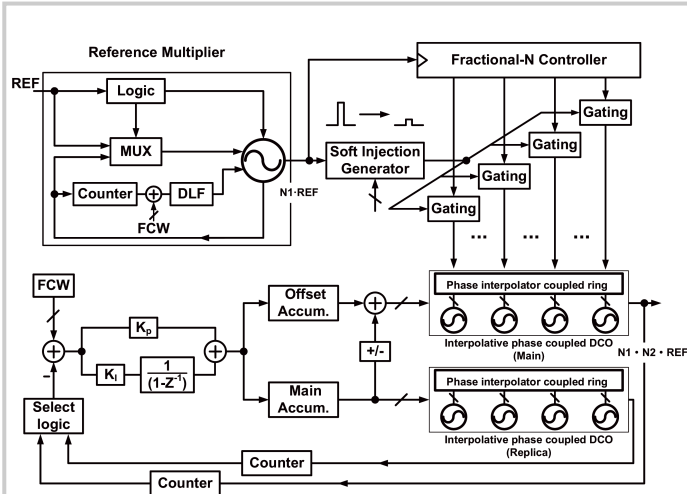


Figure 14.1.1: Block diagram of the proposed synthesizable two-stage fractional-N PLL using a soft injection-locking technique.

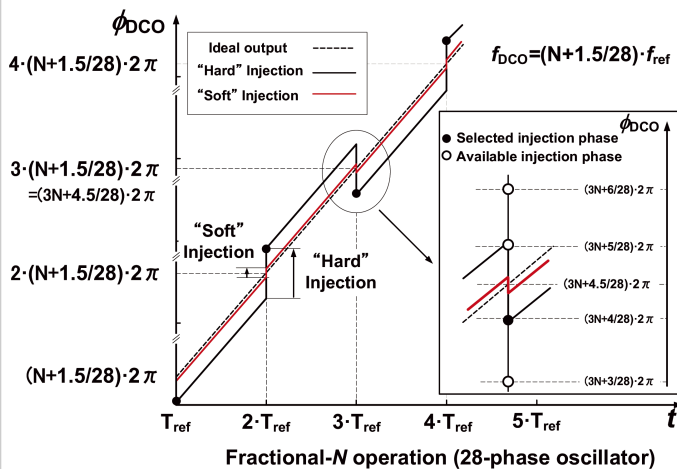


Figure 14.1.2: Conceptual phase diagram of a fractional-N injection locking oscillator using a conventional "hard" injection and the proposed "soft" injection.

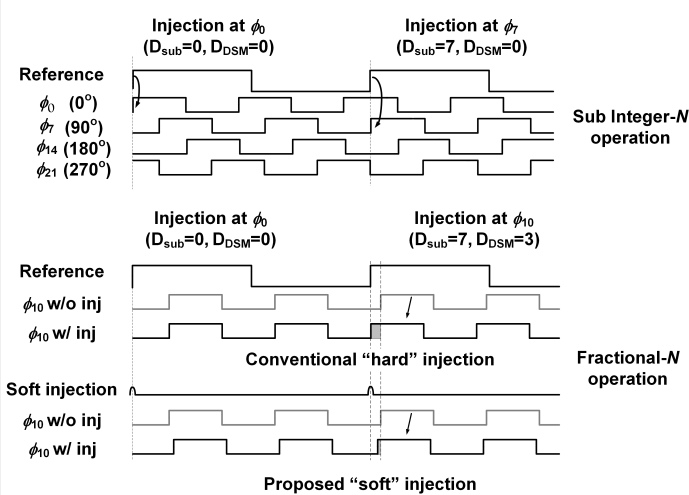


Figure 14.1.3: Locking transients of the oscillator using conventional "hard" injection and the proposed "soft" injection technique.

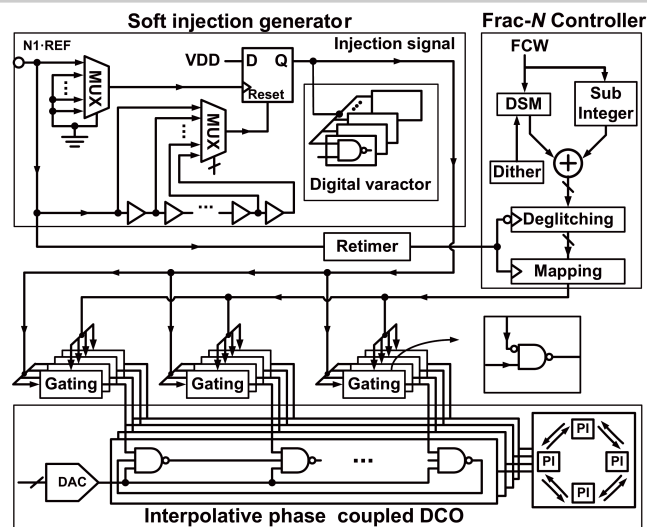


Figure 14.1.4: Block diagram of the fractional-N controller, soft injection generator, and oscillator in the second stage PLL.

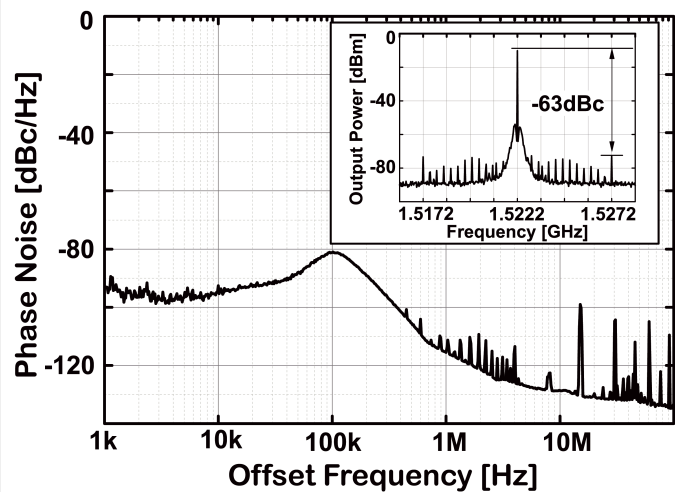


Figure 14.1.5: Measured phase noise and spectrum characteristics at a carrier of 1.5222 GHz.

	This work	[1]	[2]	[4]	[6]
Type	Frac-N	Int-N	Int-N	Frac-N	Frac-N
Freq. [GHz]	0.8-1.7	0.39-1.41	1.5-2.7	1.6-1.9	0.25-1.65
Ref. [MHz]	50-400	40-350	10	50	32
Power [mW]	3 @1.5222GHz	0.78 @0.9GHz	13.7 @1.7GHz	3 @1.7GHz	10.5 @0.58GHz
Area [mm ²]	0.048	0.0066	0.4	0.4	0.16
Integ. Jitter [ps]	3.6	1.7	3.2*	1.4	3.25
FOM [dB]	-224.2	-236.5	-218.6	-232	-221.9
CMOS	65nm	65nm	65nm	65nm	65nm
Topology	Soft Injection locking	Injection locking	TDC-based	DTC-based MDLL	Injection locking
Synthesized?	YES			No	

*RMS jitter

Figure 14.1.6: Performance summary and comparison with state-of-the-art inductor-less PLLs.

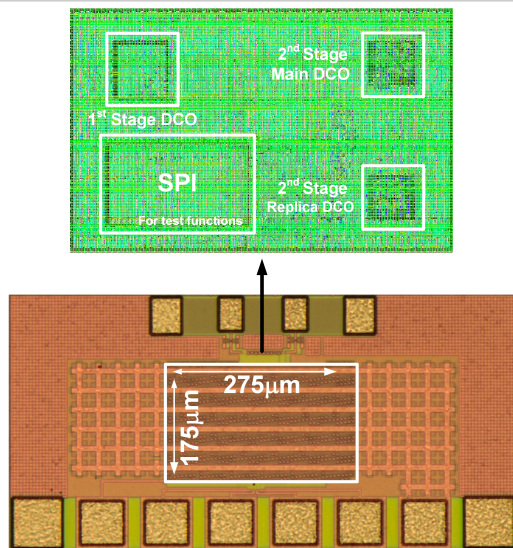


Figure 14.1.7: Die micrograph.