

# An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC

Dongsheng Yang, Wei Deng, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, and Akira Matsuzawa

Dept. Physical Electronics, Tokyo Institute of Technology  
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552 Japan.  
Tel/Fax: +81-3-5734-3764, E-mail: yang@ssc.pe.titech.ac.jp

**Abstract** – This paper presents a small area, low power, fully synthesizable PLL with a current output DAC and an interpolative-phase coupled oscillator using edge injection technique for on-chip clock generation. A prototype PLL is fabricated in a 65nm digital CMOS process, achieves a 1.7-ps integrated jitter at 0.9 GHz and consumes 0.78 mW leading to an FOM of -236.5 dB while only occupying an area of 0.0066 mm<sup>2</sup>. It achieves the best performance-area trade-off.

## I. Introduction

In modern digital systems, phase-locked loops (PLLs) are widely used for on-chip clock generation. Synthesizable PLLs [1-4], taking advantage of process scaling down, have been published recently. TDC-based PLLs [1-3] can be synthesizable while they suffer from larger area, larger jitter and larger power consumption. To achieve a low power, small area, fully synthesizable PLL, this paper presents an all-digital PLL synthesized from only standard digital library, with a current output digital-to-analog converter (DAC) for lowering the power consumption, an interpolative-phase coupled oscillator for alleviating output phase mismatch and a gated edge injection technique for tackling injection pulse width issue [4].

## II. Proposed Synthesizable PLL

Fig. 1 depicts the architecture of proposed synthesizable PLL. In order to tackle the injection timing constraints in the conventional injection-locked PLLs, a dual-loop PLL topology [4] [5] is adopted and it can also track the process voltage temperature (PVT) variations continuously. The counted numbers for two oscillators (Main and Replica) are compared with an external inputted frequency control word (FCW) respectively and generated differences are transferred to a digital loop filter composed of a proportional path and an integral path. A gated edge injection technique is proposed for phase locking in this synthesizable PLL [4].

The proposed oscillator used in both main and replica VCOs is shown in Fig. 2. An interpolative phase coupled oscillator built by three 3-stages oscillators is used to relax the phase mismatch between the outputs generated by the injection and automatic place and route (P&R). The phase imbalance within the ring and between the adjacent rings could be hold with time owing to the feedback and feed-forward property of phase interpolators. In order to cover the required frequency tuning range and maintain high resolution, the oscillator operating with a coarse, a medium and a fine tuning is utilized. The coarse tuning is realized by a standard cell based DAC while the medium tuning is achieved by digitally-controlled NAND gate. The fine tuning circuitry is realized by another type of digitally-controlled varactor using inverters and NAND gates. The digitally-controlled NAND gate introduces a capacitance difference at the inverter output node, changing the rising and falling slope thereby altering the effect on Miller effect. Thus, the capacitance difference at the inverter input node is changed and adopted as the fine tuning. In addition, the phase interpolator is realized by two inverters.

Fig. 3 shows a conceptual diagram of a standard cell based DAC which is binary weighted by 4-bit control word. The proposed current output DAC is constructed by an array of PMOS-current-source and an NMOS current mirror. The PMOS-current-source array is achieved by connecting the outputs of binary weighted NAND gates together, one input of each NAND gate to a digitally-controlled bus and the other input to D4. In order to realize the NMOS current mirror, one input of NAND gate is connected to logic HIGH and the other input to output node.

A gated edge injection technique, illustrated in Fig. 4, is adopted to deal with injection pulse width issue in conventional pulse injection locked PLLs. When injection-window signal is set to logic HIGH, it stops the oscillator and the noisy edge  $V_Y$  is replaced by injection signal with clean edge to reset the accumulated jitter. Then the oscillator works again with clean and aligned edge if injection-window becomes logic LOW. Additionally, the phase replacement and alignment is finished in only one reference cycle.

## III. Measurement Results

The proposed PLL is fabricated in a 65 nm digital CMOS process. Fig. 5 shows the phase noise and output spectrum at 0.9 GHz output measured by a signal source analyzer (Agilent E5052B) and a spectrum analyzer (Agilent E4407B) respectively with 150 MHz as reference frequency. The measured phase noise corresponds to a 1.7-ps jitter when integrated from 10 kHz to 40MHz.

Fig. 6 provides a comparison table between this work and previous synthesizable PLLs. The proposed PLL achieves the comparable performance with state-of-the-art synthesizable PLLs while it occupies only 110  $\mu\text{m} \times 60 \mu\text{m}$  area. The figure of merit (FOM) is -236.5 dB at a 0.9 GHz carrier frequency. The chip die photo is shown in Fig. 7.

## IV. Conclusion

This paper presents a fully synthesized PLL with a current output DAC and an interpolative-phase coupled oscillator based on standard digital library without any modification. The whole design is realized by digital design flows.

## Acknowledgements

This work is partially supported by MIC, SCOPE, MEXT, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc.

## References

- [1] Y. Park and D. D. Wentzloff, "An All-Digital PLL Synthesized from A Digital Standard Cell Library in 65nm CMOS," *IEEE Custom Integrated Circuits Conf.*, pp. 1-4, Sep. 2011.
- [2] W. Kim, J. Park, J. Kim, T. Kim, H. Park, and D. Jeong, "A 0.032mm<sup>2</sup> 3.1mW Synthesized Pixel Clock Generator with 30ps<sub>rms</sub> Integrated Jitter and 10-to-630MHz DCO Tuning Range," *ISSCC Dig. Tech. Papers*, pp. 250-251, Feb. 2013.
- [3] M. Faisal and D.D. Wentzloff, "An Automatically Placed-and-Routed ADPLL for The MedRadio Band using PWM to Enhance DCO Resolution," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 115-118, Jun.

2013.

[4] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, "A 0.0066mm<sup>2</sup> 780μW Fully Synthesizable PLL with A Current-Output DAC and An Interpolative Phase-Coupled Oscillator using Edge-Injection Technique," *ISSCC Dig. Tech. Papers*, pp. 266-267, Feb. 2014.

[5] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.022mm<sup>2</sup> 970μW Dual-Loop Injection-Locked PLL with -243 dB FOM using Synthesizable All-Digital PVT Calibration Circuits," *ISSCC Dig. Tech. Papers*, pp. 248-249, Feb. 2013.

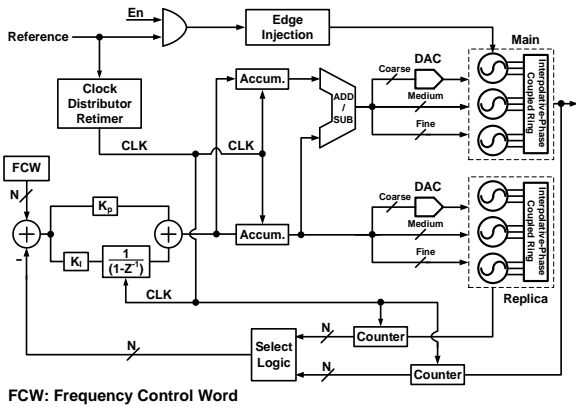


Fig. 1. Block diagram of the proposed fully synthesizable PLL with a DAC and phase-coupled oscillator.

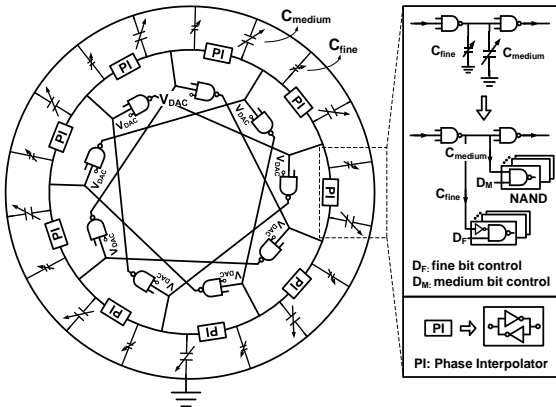


Fig. 2. Block diagram of the phase-coupled oscillator.

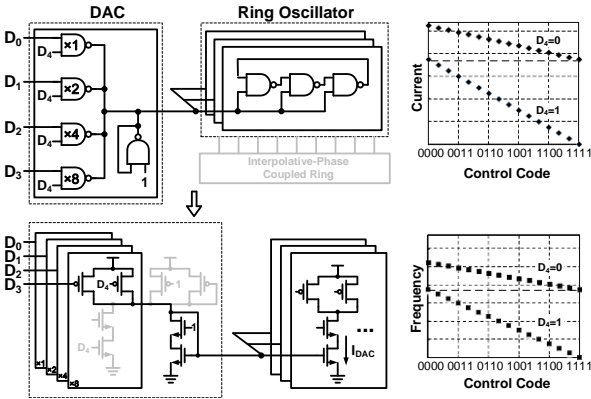


Fig. 3. Conceptual diagram of the synthesizable DAC with a current-linear output.

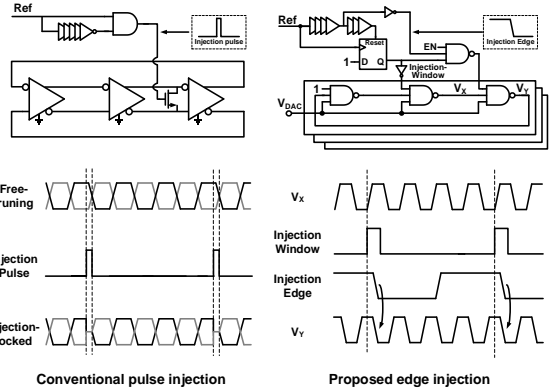


Fig. 4. Block diagram and locking transient of the conventional pulse injection and proposed edge injection.

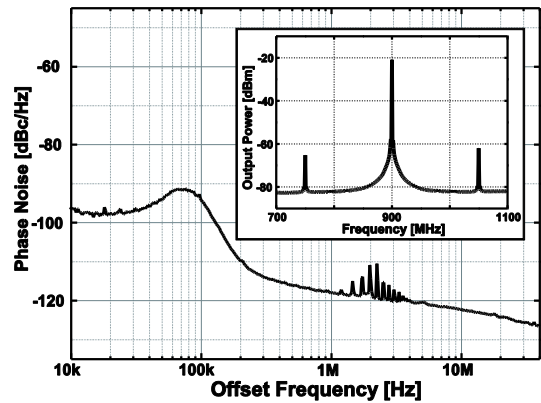


Fig. 5. Measured phase noise and spectrum characteristics at a carrier of 0.9GHz.

	This work	[1]	[2]	[3]
Freq. [GHz]	0.39-1.41	1.5-2.7	0.25-1.65	0.4-0.46
Ref. [MHz]	40-350	10	25	40.3
Power [mW]	0.78 @900 MHz	13.7 @2.5 GHz	3.1 @250MHz	2.1 @403MHz
Area [mm <sup>2</sup> ]	<b>0.0066</b>	0.042	0.032	0.1
Normalized Area	1	6.36	4.84	15.15
Integ. Jitter [ps]	1.7	N.A.	30	N.A.
Jitter RMS [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	<b>-236.5</b>	-218.6*	-205.5	-214*
CMOS Technology	65nm	65nm	28nm	65nm
Topology	Injection lock based	TDC-based	TDC-based	TDC-based

Fig. 6. Performance summary and comparison with state-of-the-art synthesized PLLs.

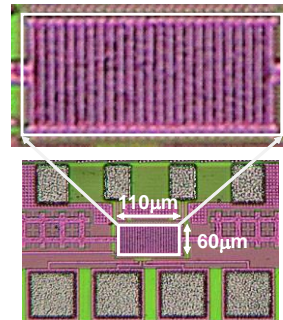


Fig. 7. Chip Micrograph.