A 58.3-to-65.4 GHz 34.2 mW Sub-Harmonically Injection-Locked PLL with a Sub-Sampling Phase Detection

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Abstract – This paper presents a low power and low noise sub-harmonically injection-locked PLL using a 20GHz sub-sampling PLL (SS-PLL) and a quadrature injection locked oscillator (QILO). Lower in-band phase noise and out-of-band phase noise have been achieved through the sub-sampling phase detection and sub-harmonic injection techniques, respectively. Implemented in a 65nm CMOS, this work can support all 60GHz channels and achieves a phase noise of -115dBc/Hz at 10MHz offset while consuming 20.2mW and 14mW from the 20GHz SS-PLL and the QILO, respectively.

I. Introduction

Fig. 1 shows the simplified block diagram of 60GHz direct conversion transceiver where phase noise of synthesizer at in-band and out-of-band could sets a limit on achievable modulation scheme. From recently reported 60GHz PLLs, the PLL based on sub-harmonic QILO is preferred due to best out-of-band phase noise [2]. However, since it should be able to generate standard four channels as well as support channel bonding to boost data rate while supporting standard 36/40MHz reference, this results in large divide ratio (N) in an integer-N PLL feedback leading to high in-band phase noise as PFD/CP noise is multiplied by N^2 [2]. Thus, this paper proposes a technique to suppress in-band noise through sub-sampling phase detection resulting less divide ratio while maintaining good out-of-band phase noise using sub-harmonic injection locking technique [5].

II. Proposed 60GHz PLL Architecture

The proposed synthesizer includes a sub-harmonic 20GHz SS-PLL and a 60GHz QILO as shown in Fig.2. The 20GHz PLL can perform both classical PFD/CP mode (E_n=0) and sub-sampling mode (E_n=1). For a PFD/CP mode, E_n is set to 0. The sub-sampling loop is disabled as CP_1 is off and PFD in lower loop works without any dead zone. A divide-by-2 divider is placed after reference clock to support channel bonding but at an expense of lower reference clock. "SEL_1" bit of MUX_1 can control corresponding division ratio of input 36/40MHz reference clocks. Due to the limited acquisition range of sub-sampling phase detector (SSPD), a frequency-locked loop (FLL) is necessary. In this work, for sub-sampling mode, E_n is set to 1, a dead zone of PFD is created. PFD controls CP_2 until the signal is close to lock working as an FLL. Then, the SSPD samples the divider output with 18MHz reference clock converting phase error into voltage variation as shown in Fig.3. A wave shaper is utilized to relax mismatch of differential signals. Current output from CP_1 controls VCO in the locked state with significantly less N ratio. The sub-sampling mode bypasses a divide-by-60 ratio and an in-band suppression in the feedback loop is calculated to be approximately 15dB when sampled by the divided reference clock.

In this work, a class-C VCO which theoretically has higher DC-RF current conversion efficiency comparing to Class-B VCO are utilized as shown in Fig.4. Cross-coupled capacitors are used in 20-GHz buffer to help cancel parasitic gate-to-drain capacitances [1].

III. Measurement Result

The proposed 60GHz frequency synthesizer is implemented in a standard 65nm CMOS process. The 60GHz QILO consumes an average power of 14mW from 1.2V supply. It can generate free-running frequencies from 58.3-65.4GHz. Fig.5. shows the measured phase noise characteristics of 20GHz SS-PLL at carrier frequency of 20.88GHz, 60GHz QILO locked to 20GHz PFD/CP PLL, and 60GHz QILO locked to 20GHz SS-PLL both at a carrier frequency of 62.64GHz. In the sub-sampling mode, the out-of-band phase noise of 60GHz QILO locked to 20GHz SS-PLL is maintained at -115dBc/Hz at 10MHz offset, where its in-band phase noise shows a 15dB reduction at 100 kHz offset comparing to the case where 60GHz QILO locked to conventional 20GHz PFD/CP PLL. The calibrated output power of 20GHz PLL is approximately -4 dBm. The power consumption of the 20GHz SS-PLL is 20.2mW from 10.6mW of the 20GHz VCO and its buffer, 4.8mW of the ILFD and 4.8mW of digital circuits from 1.2V supply. This is about 3 times power reduction compared to [2]. Table I summarizes the comparison of the proposed work with the state-of-the-art 60GHz PLLs. Sub-harmonic injection method shows the lowest out-of-band phase noise at 10MHz offset comparing to [3]-[4]. However, due to the use of relatively lower REF clock, the work in [2] and PFD/CP mode of this work have higher in-band phase noise [4]. The sub-sampling loop of the proposed work successfully suppresses phase noise to -69dBc at 10kHz offset [5]. The chip photos are shown in Fig.6 where the 20GHz SS-PLL and QILO occupy an area of 700μm×800μm and 1000μm×600μm including PADs, respectively.

IV. Conclusion

This paper presents 60GHz frequency synthesizer using 20GHz SS-PLL and 60GHz QILO. With careful design, it can support various 60GHz standards while achieving low power and phase noise.

Acknowledgements

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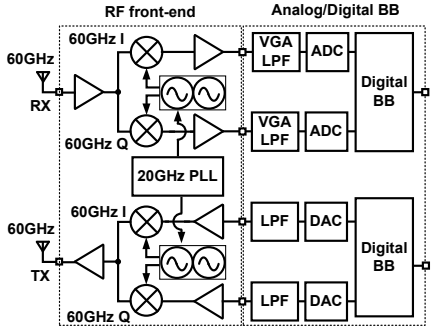

Fig.1. Block diagram of the 60GHz transceiver system (©2014 IEEE [5]).

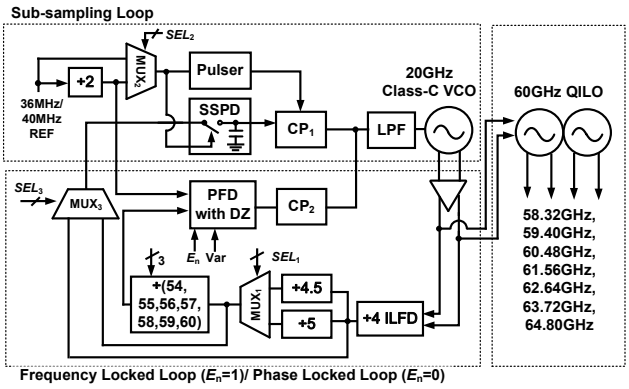

Fig.2. Proposed architecture for 60GHz sub-harmonic injection-locked sub-sampling quadrature frequency synthesizer (©2014 IEEE [5]).

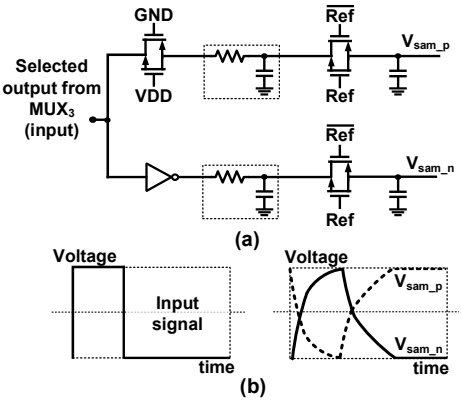

Fig.3. (a) Schematic of sampling switches and (b) waveforms of sampled outputs (©2014 IEEE [5]).

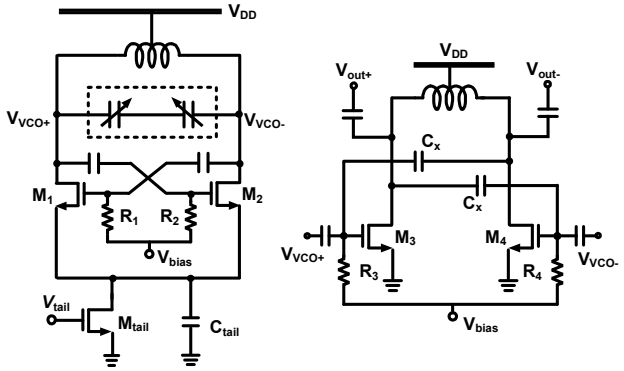

Fig.4. Schematic of (a) a 20-GHz Class-C VCO and (b) a 20-GHz capacitive-cross-coupled buffer (©2014 IEEE [5]).

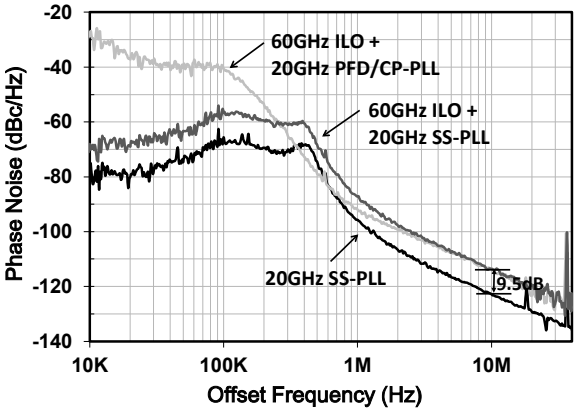

Fig.5. Measured phase noise at 62.64 GHz (©2014 IEEE [5]).

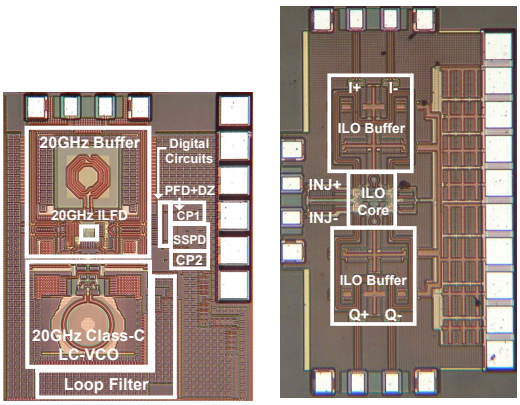

Fig.6. Chip Micrograph (©2014 IEEE [5]).

TABLE I PERFORMANCE COMPARISON BETWEEN THE-STATE-OF-THE-ART 60GHZ PLLS (©2014 IEEE [5])

	REF (MHz)	Freq. (GHz)	PN(dBc/Hz)*	Features	Power (mW)
[4]	100	56.0-62.0	-71 /-109	60GHz AD-PLL	48
[3]	40	53.8-63.3	-89 /-107	60GHz SS-QPLL	42
[2]	18/20	58.1-65.0	-40 /-117	20GHz PLL + 60GHz QILO	72
This (CP)	18/20	58.3-65.4	-40 /-115	20GHz PLL + 60GHz QILO	32.8
This (SS)	**18/20**	58.3-65.4	**-69 /-115**	**20GHz SS-PLL** + 60GHz QILO	**34.2**

**Phase noise (PN) comparison at 10 kHz and 10 MHz offset*