A 20GHz Class-C VCO Using Noise Sensitivity Mitigation Technique

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Outline

- **Background**
- **Class-C VCO**
- **PN Degradation on Class-C VCO**
  - **AM-PM Conversion**
  - **Parasitic Cap Variation**
- **Proposed AM-PM Conversion Cancellation**
  - C_{GS} **curve**
  - C_{SB} **curve**
- **Conclusion**

Background

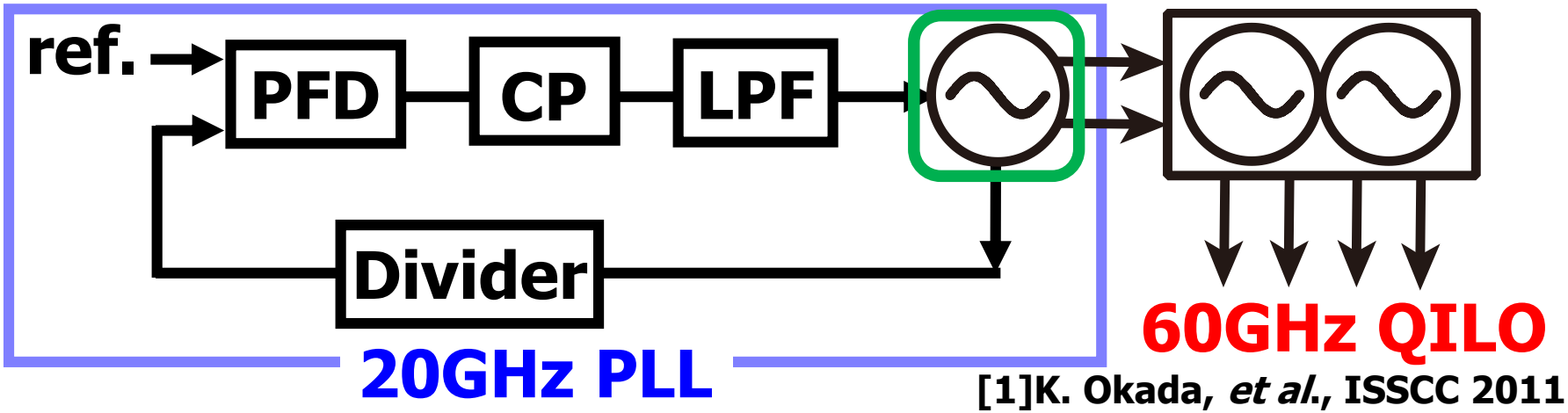
·60GHz CMOS Transceiver IC

→ Local Oscillator using Injection-Locking

☺ Lower phase noise than direct 60GHz generation

·20GHz VCO Requirement

→ 1. Quite low noise 2. High power efficiency



[1]K. Okada, *et al.*, ISSCC 2011

VCO Performance

- **Phase Noise Theory in LC-Tank Oscillator**

$$\mathrm{PN} = 10\log_{10}\left\{\frac{P_{\mathrm{noise}}}{P_{\mathrm{sig}}}\right\}$$

$$= 10\log_{10}\left\{\frac{2F\mathrm{k_B}T}{P_{\mathrm{sig}}} \cdot \left(\frac{\omega_0}{2Q\omega_{\mathrm{offset}}}\right)^2\right\}$$

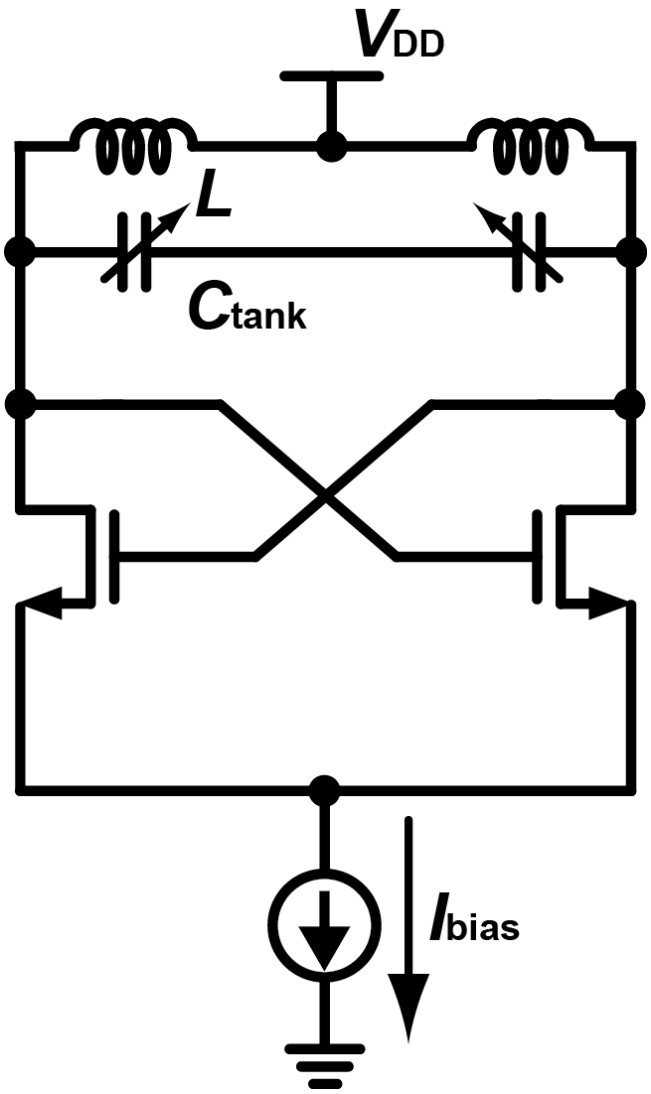
→ should maximize

- **Power Efficiency in LC-Tank Oscillator**

$$\mathrm{PE} = \frac{P_{\mathrm{sig}}}{P_{\mathrm{DC}}} = \frac{I_{\mathrm{sig}}}{I_{\mathrm{DC}}} \cdot \frac{V_{\mathrm{sig}}}{V_{\mathrm{DC}}}$$

→ should be close to 1

LC-based VCO

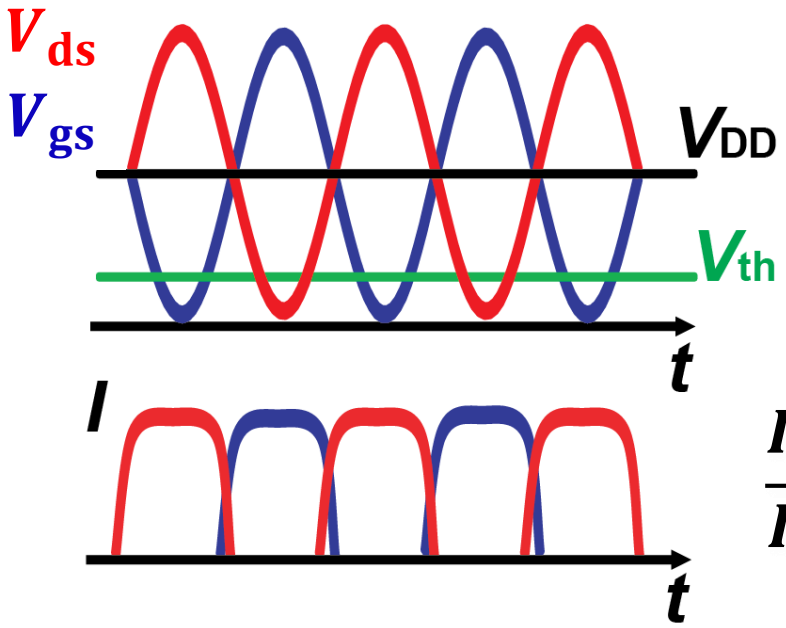


☺ **High Spectral Purity**

→ **High Q-factor**

☹ **Low Power Efficiency**

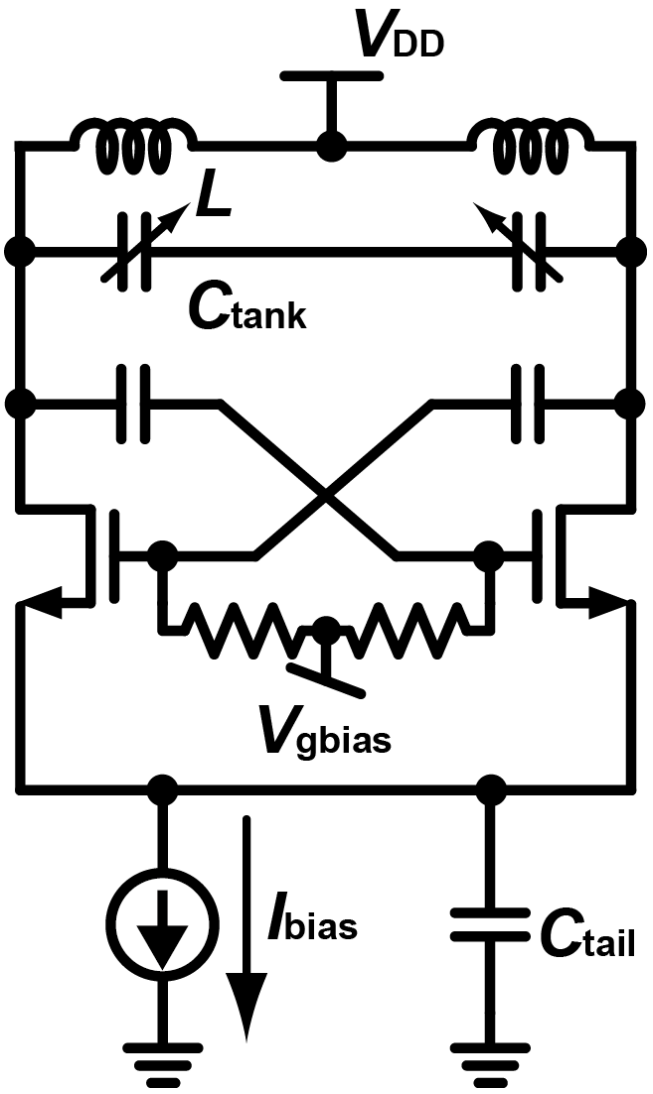
→ **Square current waveform**



$$\frac{I_{sig}}{I_{DC}} = \frac{2}{\pi}$$

Class-C VCO[2]

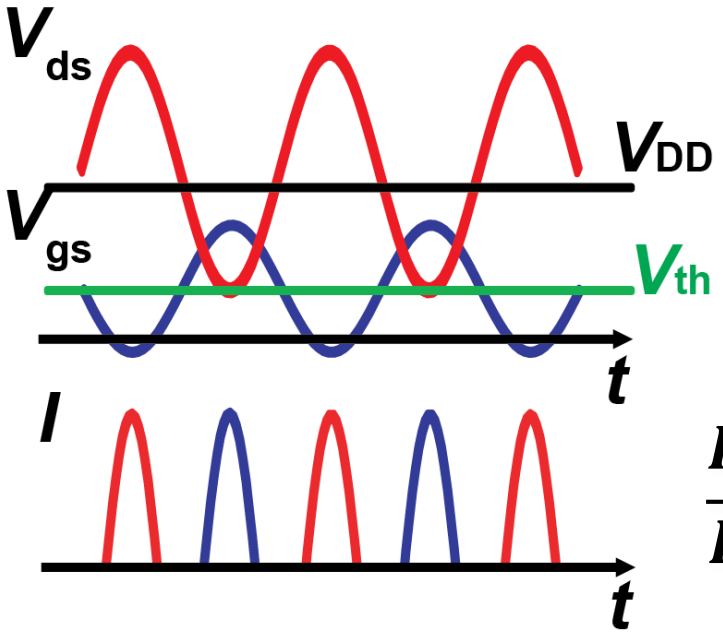
[2] A. Mazzanti, et al., JSSC 2008



☺ **High Current Efficiency**

→ **Sinusoidal waveform**

Tr keeps in saturation region



$$\frac{I_{sig}}{I_{DC}} = 1$$

Class-C VCO[2]

☹ **Maximum Amplitude is limited**

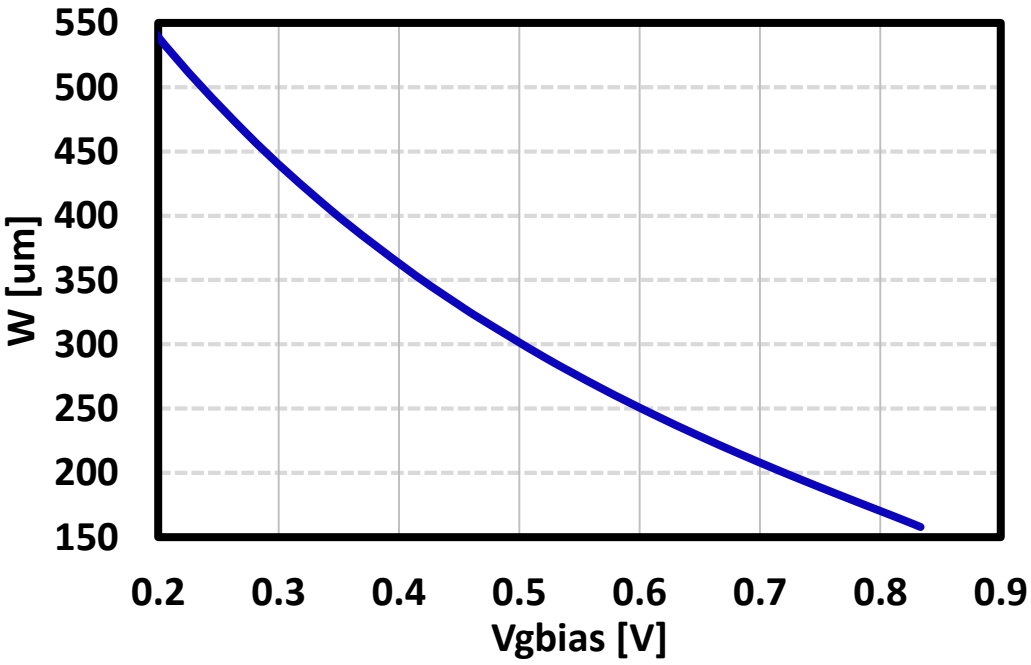
$$V_{sig} < \frac{V_{DD} + V_{TH} - V_{GBIAS}}{2}$$

$\frac{V_{sig}}{V_{DC}}$ **should be close to 1**

→ **Maximize** V_{sig}

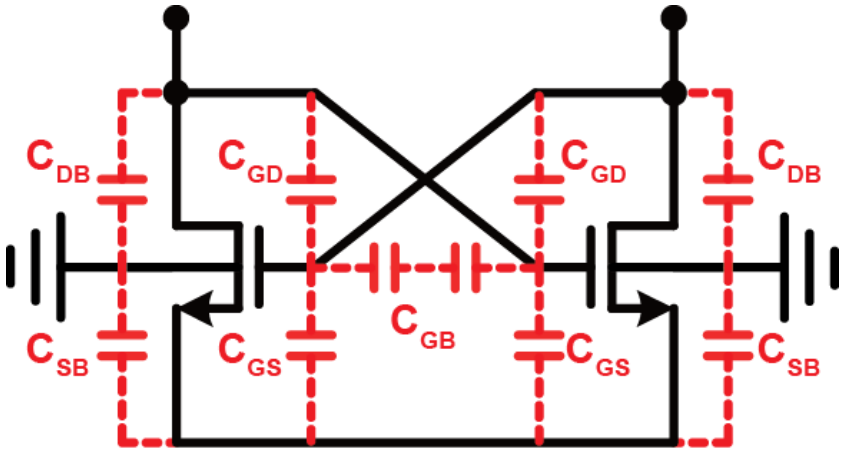
→ **smaller** V_{GBIAS}

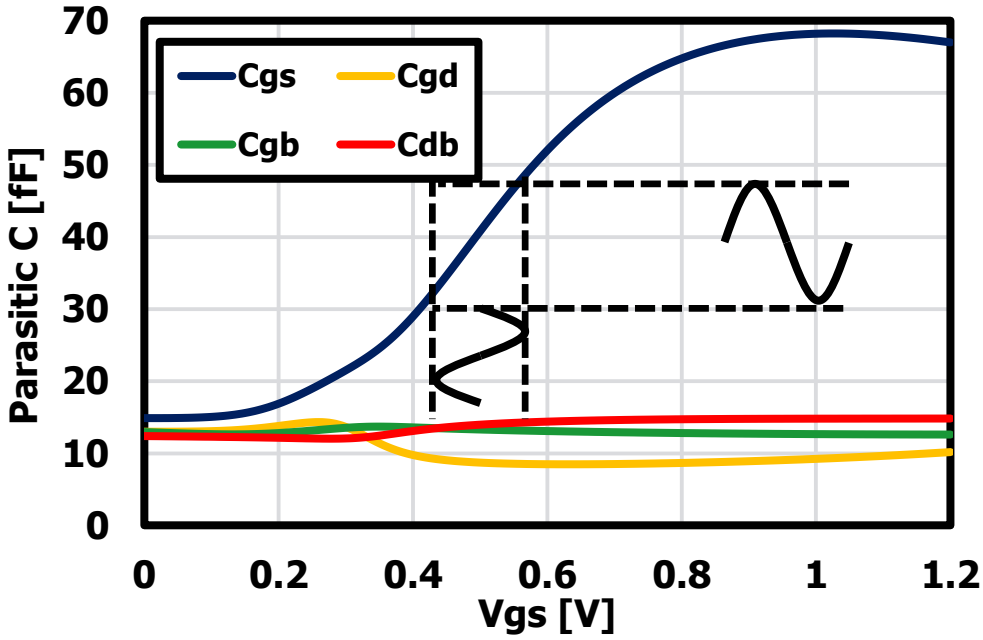
→ **larger Tr is necessary for robust oscillation**



Cross-Coupled Pair

☹ Non-Negligible Parasitic Capacitances





$$\frac{\partial C_{\mathrm{CCTr}}}{\partial V_{\mathrm{GS}}} \propto \frac{\partial C_{\mathrm{GS}}}{\partial V_{\mathrm{GS}}}$$

C_{GS} causes random frequency variation

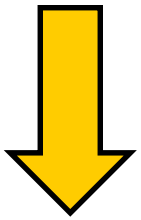
→ AM-PM Conversion like a varactor

V_{GBIAS} noise

·Noise Sources

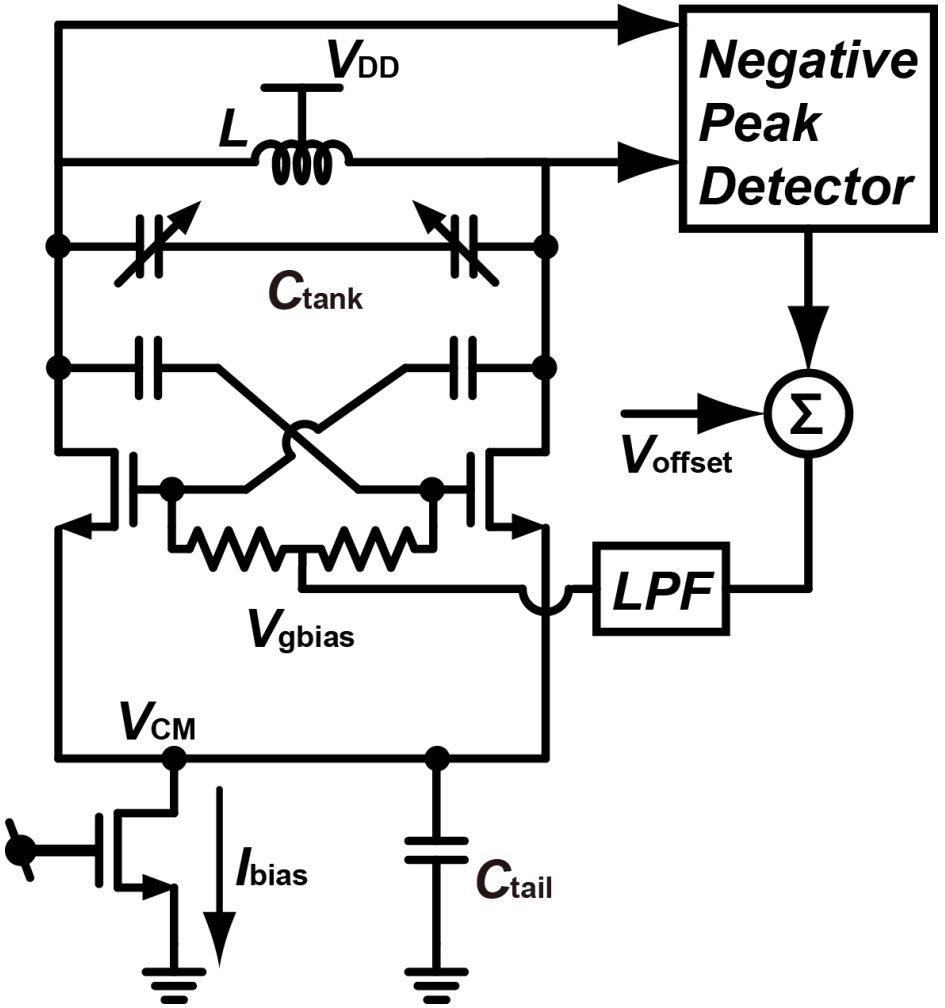
- Resistors for DC-bias
- Adaptive Bias Circuits[3]

→ ensure robust start-up



large V_{GBIAS} variation

$$\Delta f = \frac{\partial f}{\partial V_{GBIAS}} \cdot \Delta V_{GBIAS}$$

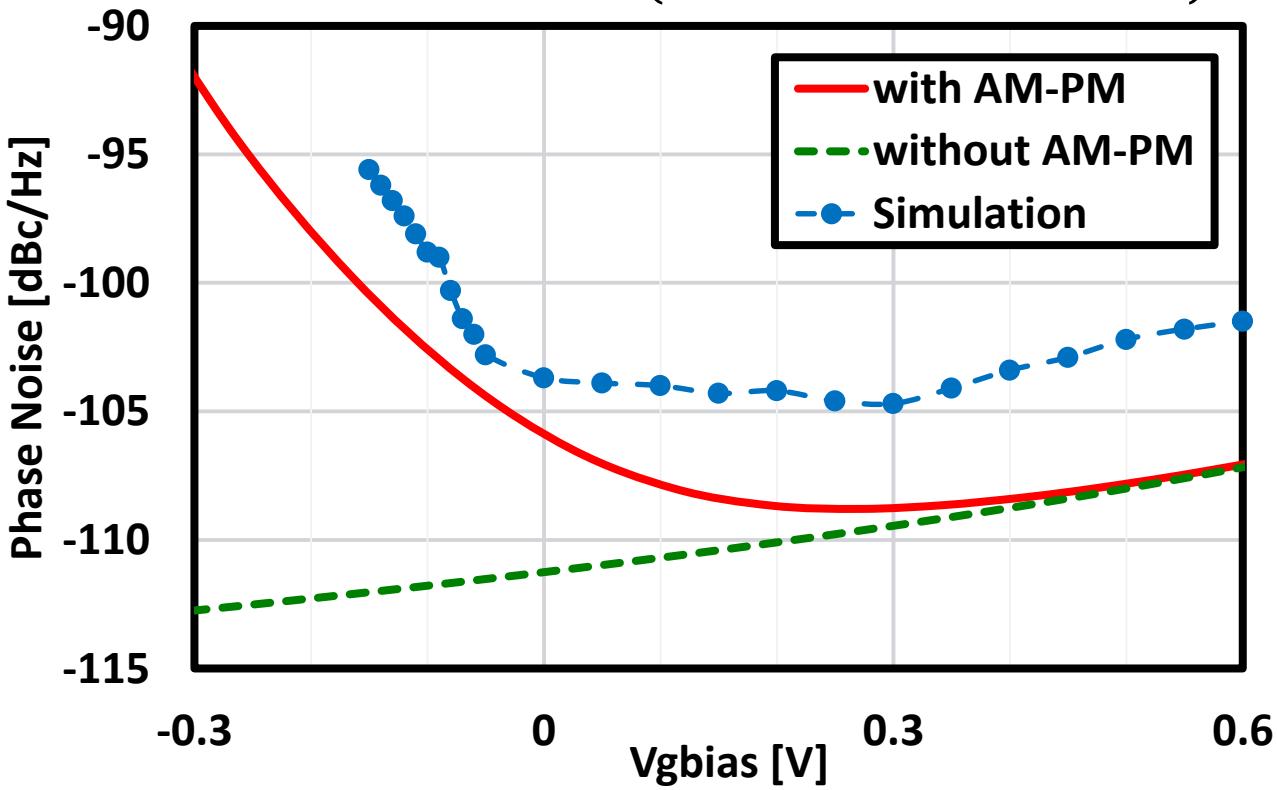


[3] W.Deng, *et al.*, JSSC 2013

AM-PM Conversion

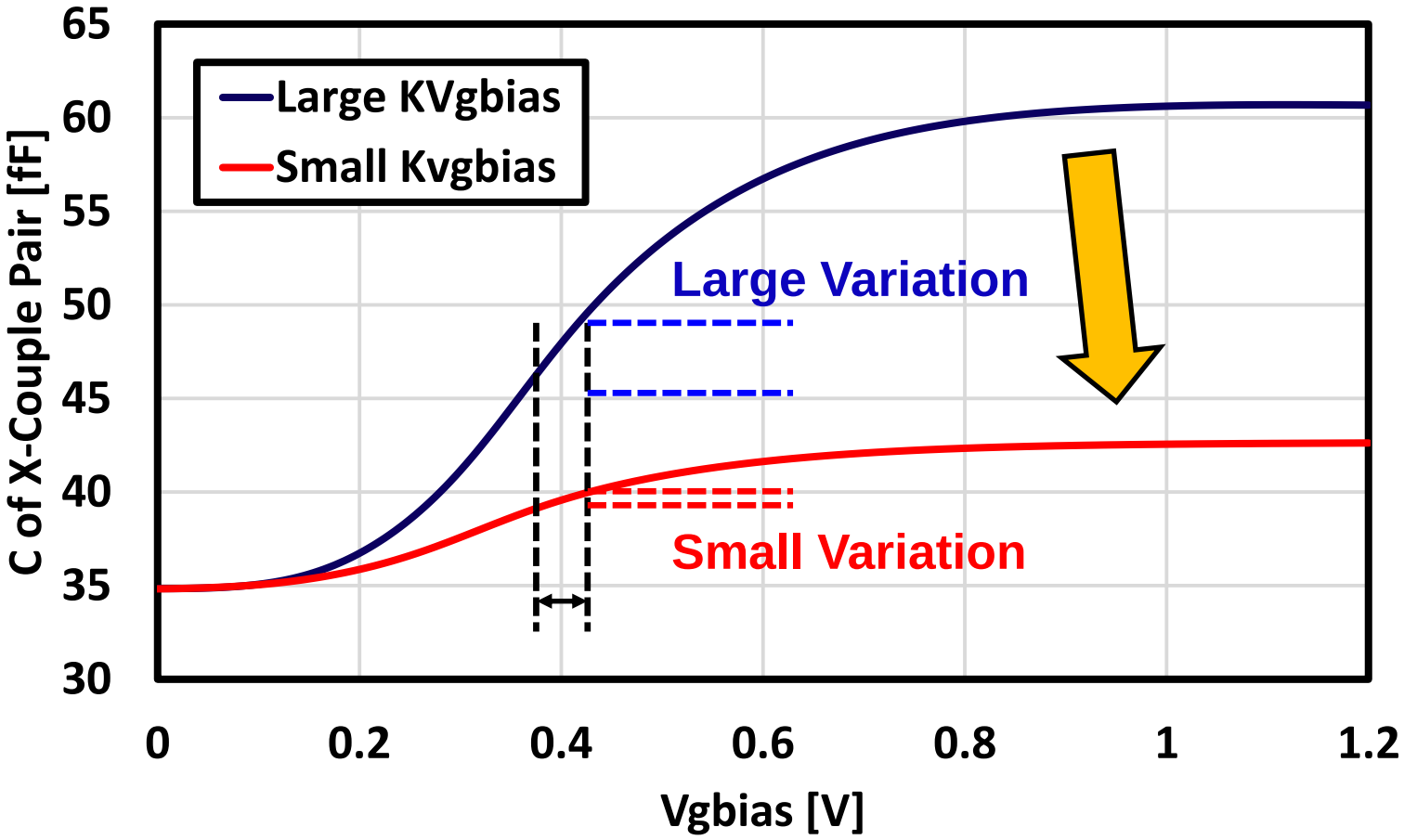
$$K_{V_{GBIAS}} = \frac{\partial \omega_0}{\partial V_{GBIAS}} = \frac{\partial \omega_0}{\partial C} \cdot \frac{\partial C}{\partial V_{GBIAS}} = -\frac{\omega_0}{C} \cdot \frac{1}{4} \frac{\partial C_{GS}}{\partial V_{GBIAS}}$$

$$PN_{AM-PM} = 10\log_{10}\left\{\left(\frac{V_{noise} \cdot K_{V_{GBIAS}}}{2\omega_{offset}}\right)^2\right\}$$



Design Concept

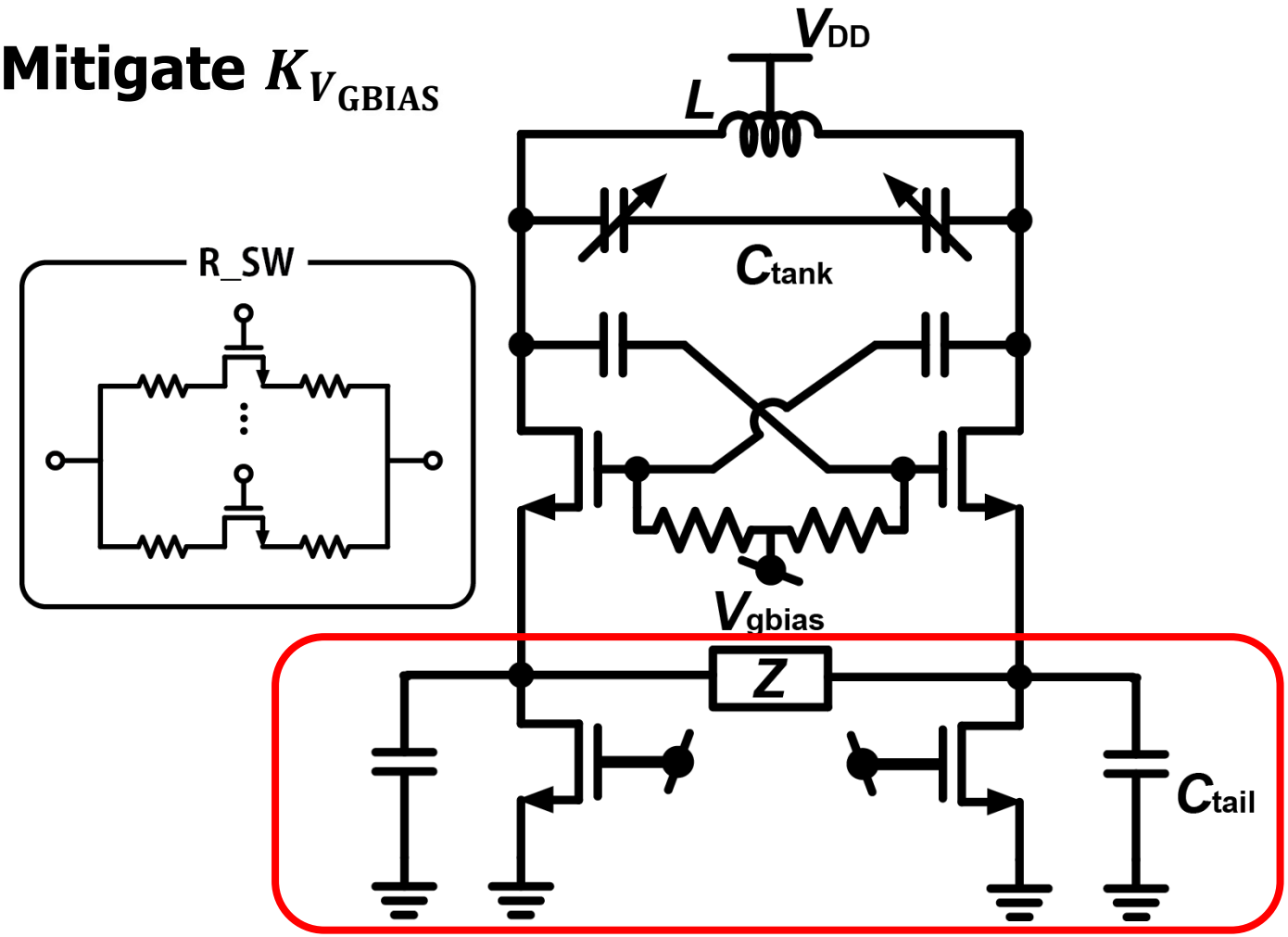
Is it possible to mitigate $K_{V_{GBIAS}}$ around V_{TH}?



Proposed Circuit

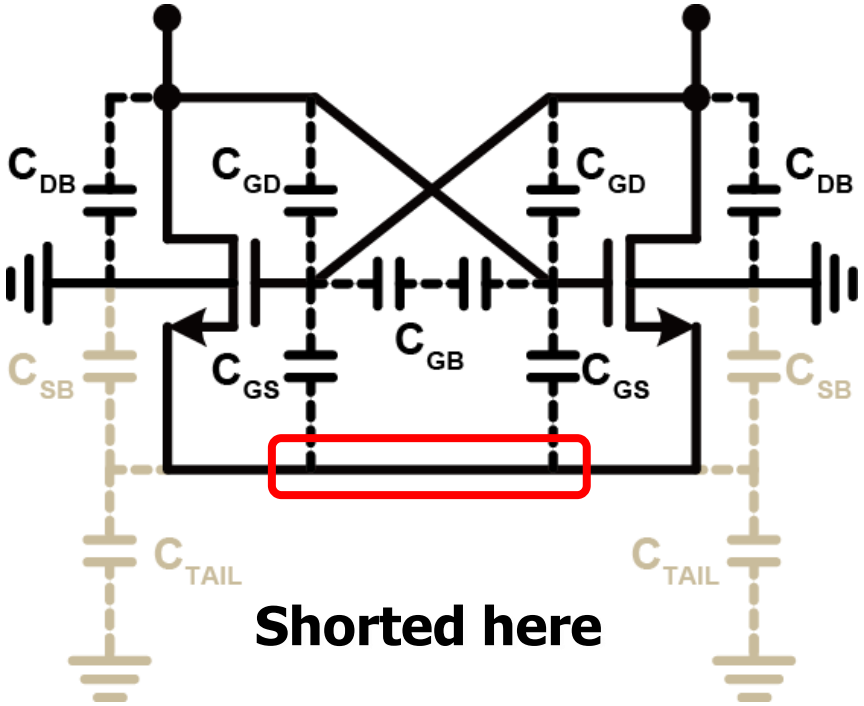
- **Resistive Joint on 2 legs of Cross-Coupled Pair**

☺ **Enable to Mitigate $K_{V_{GBIAS}}$**

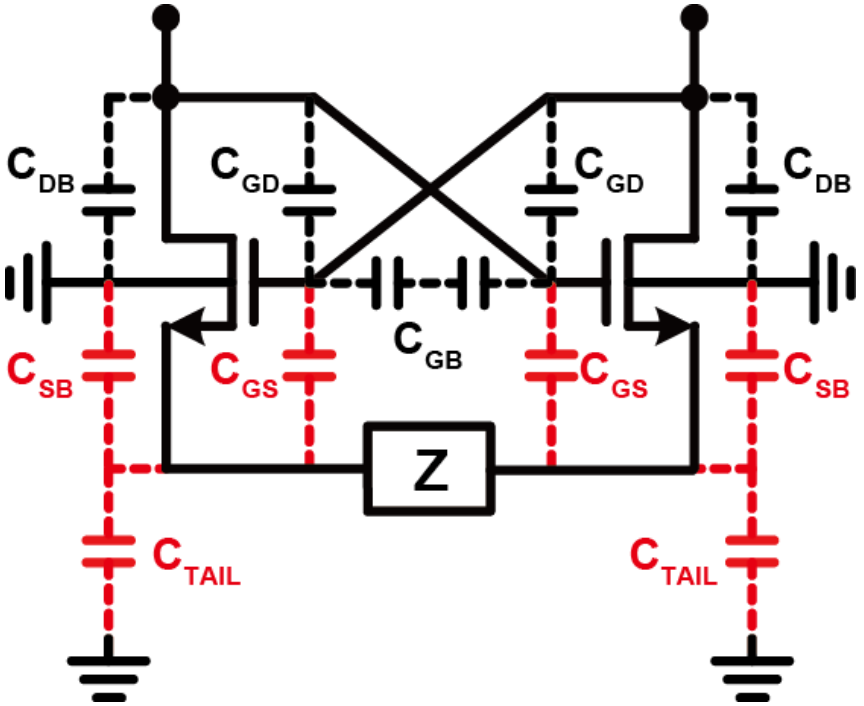


Mechanism

Conventional

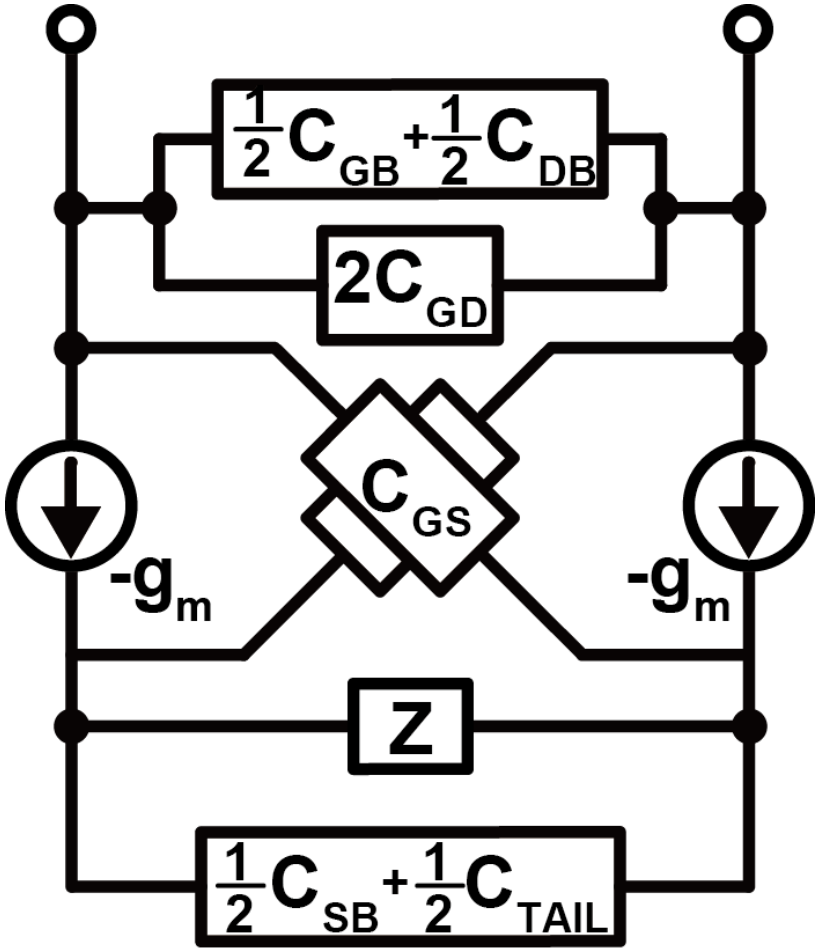


Proposed



Z, C_{SB} and C_{TAIL} have to be taken in consideration

Mechanism



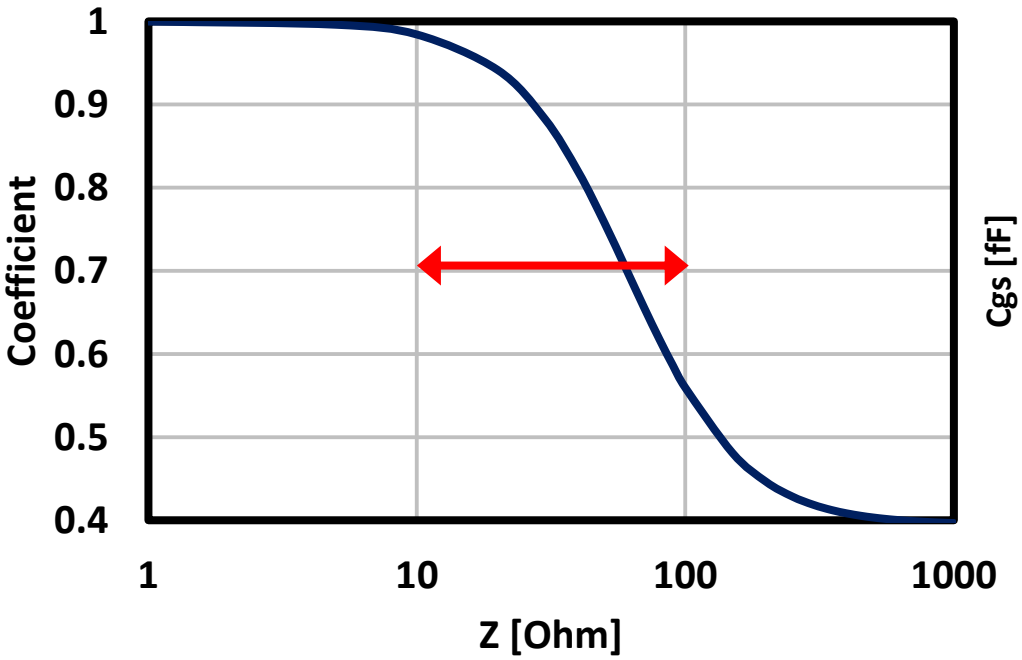
Independent of Z
C_{GD}, C_{DB}, C_{GB}

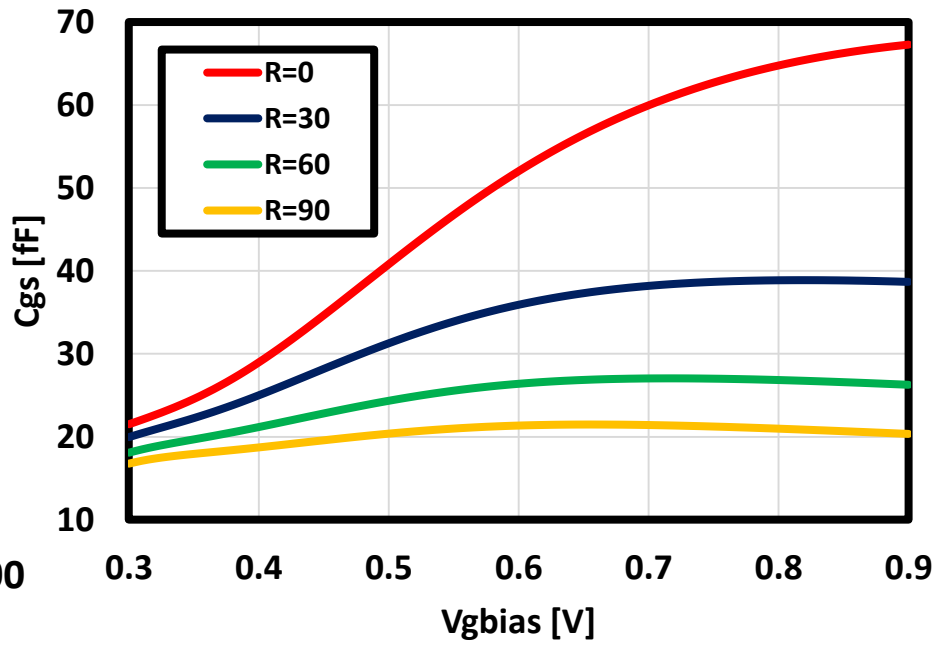
dependent on Z
C_{GS}, C_{SB}

C_{GS}, C_{SB} contribution should be re-considered

Mechanism-C_{GS}

$$\frac{C_{GS\_prop}}{C_{GS\_conv}} = 1 - \frac{g_m{}^2 + \omega^2 C_{GS} \cdot (C_{GS} + C_{TAIL})}{\left(\frac{1}{Z}\right)^2 + \omega^2 \cdot (C_{GS} + C_{TAIL})^2}$$





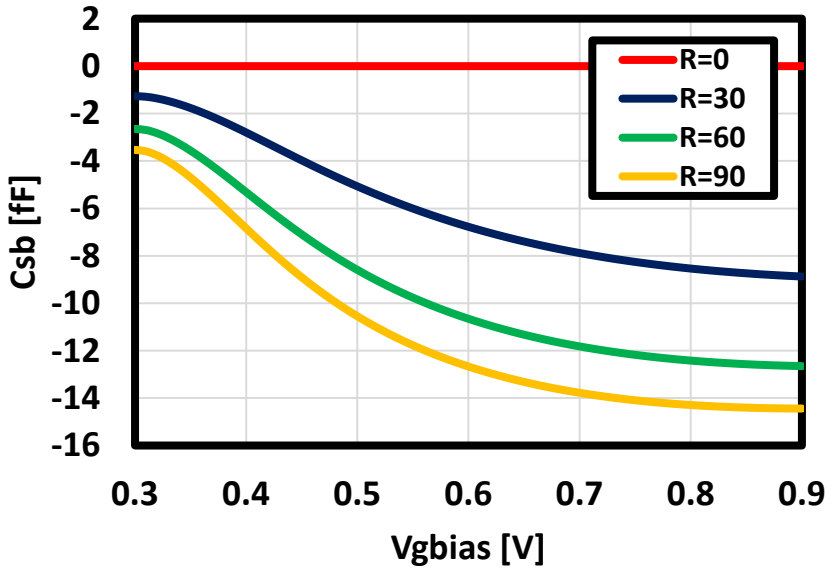
C_{GS} steep can be more moderate

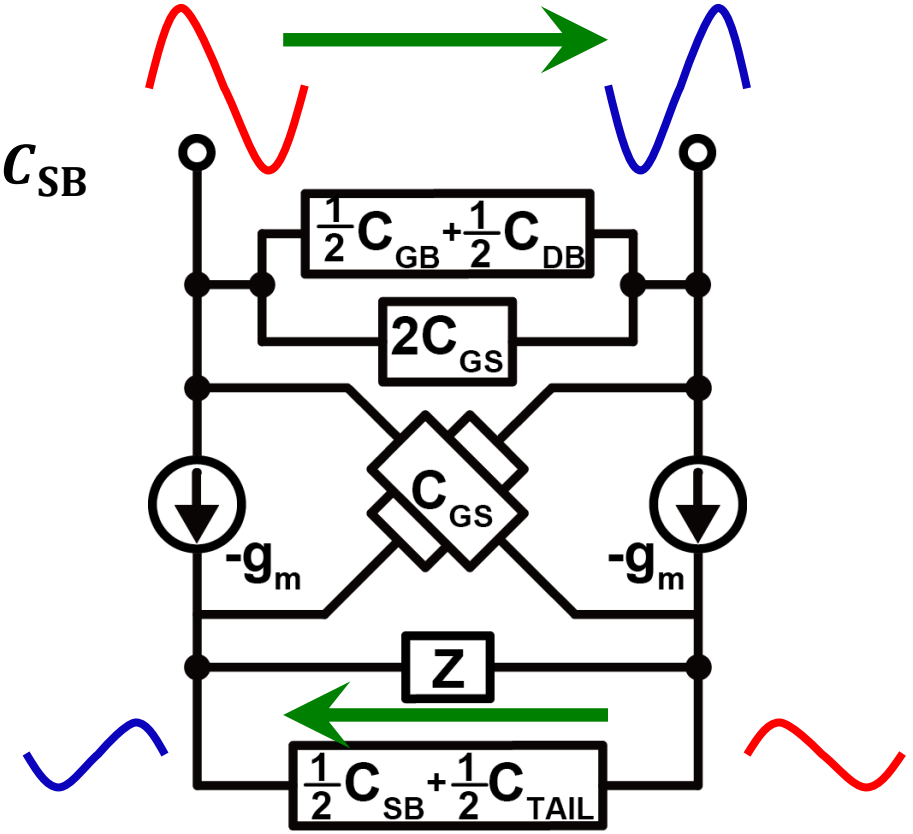
Mechanism-C_{SB}

C_{SB} can be seen as negative cap[4]

→ Inversion from gate to drain cross connection

$$\frac{-g_m{}^2}{\left(\frac{1}{Z}+g_m\right)^2+\omega^2\cdot(C_{GS}+C_{TAIL})^2}\cdot C_{SB}$$



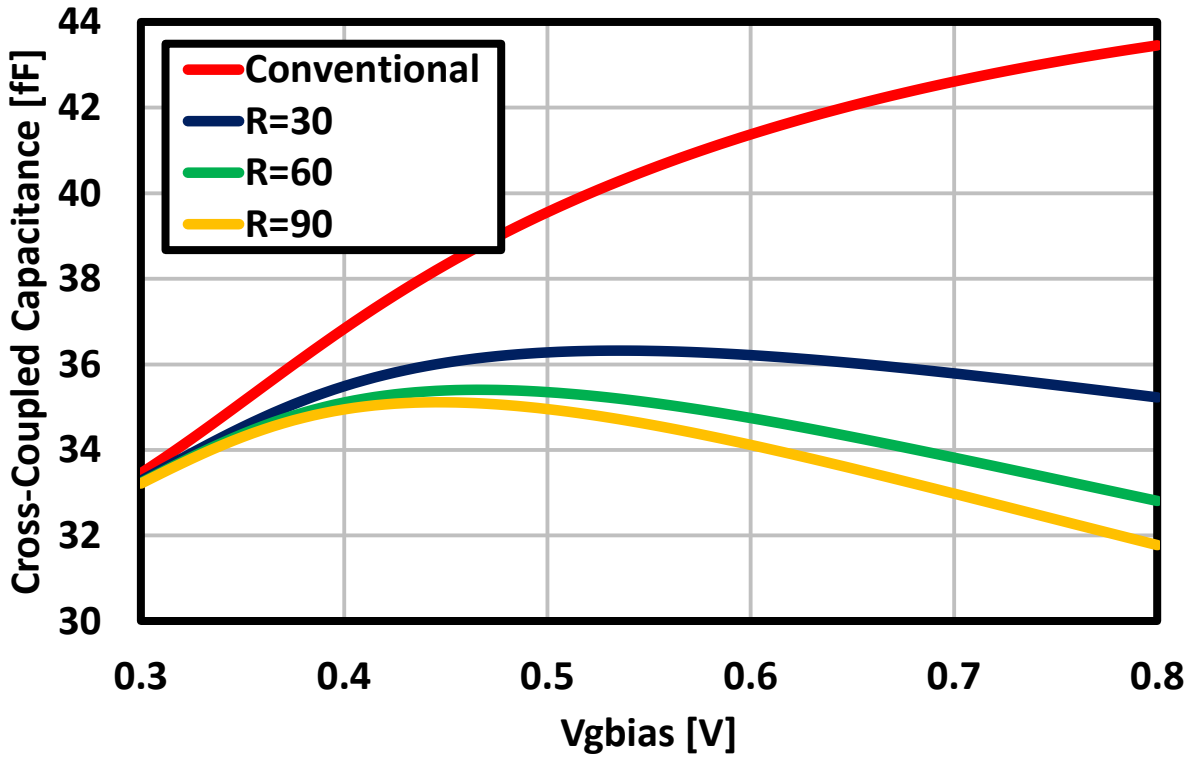


[4] L. Fanori, et al., JSSC 2010

Dependence to V_{GBIAS}

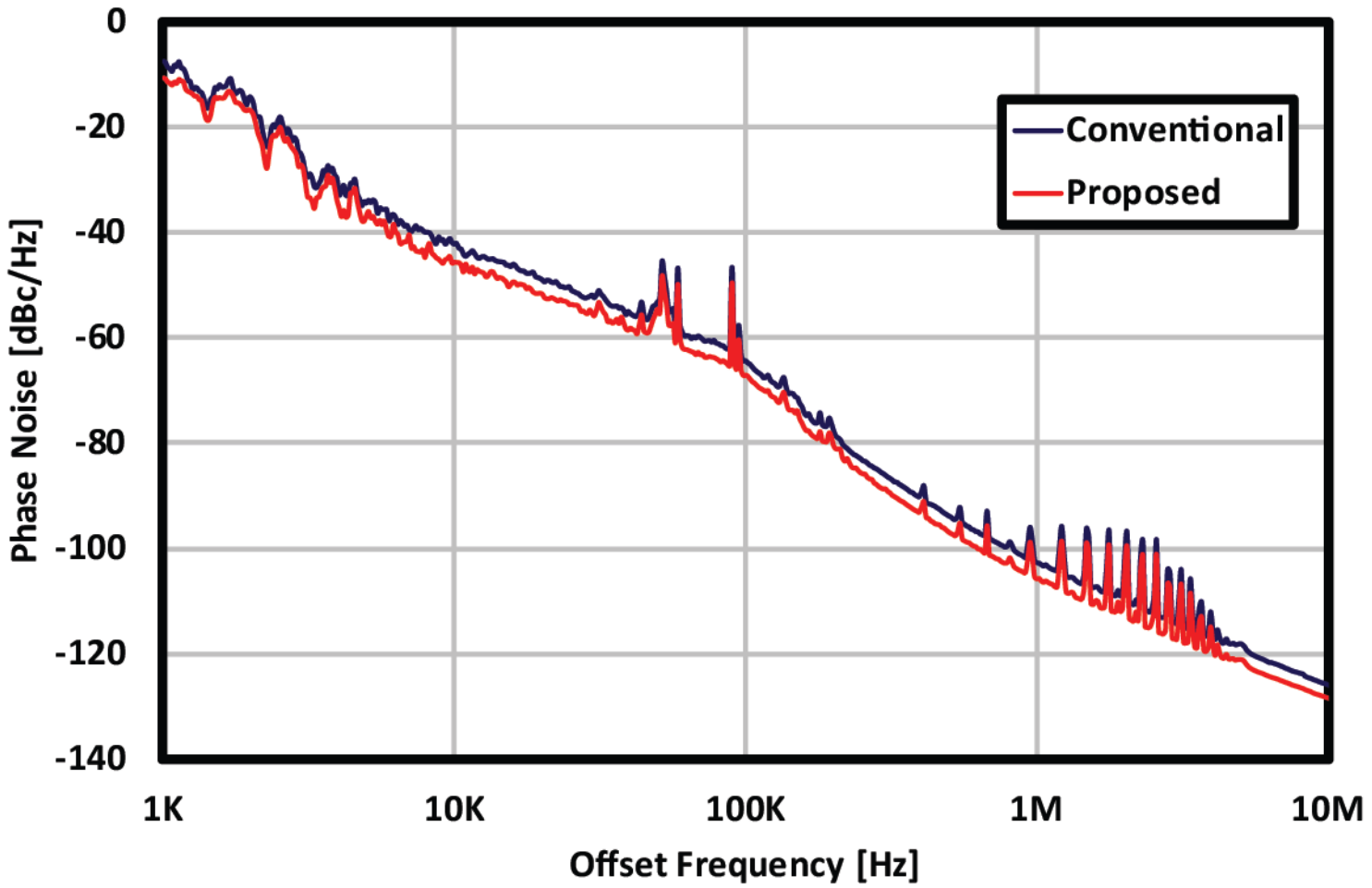
- Z make C_{GS} steep more moderate
- C_{SB} generate negative steep

➡ **Frequency Sensitivity Zero point**



Measured Phase Noise

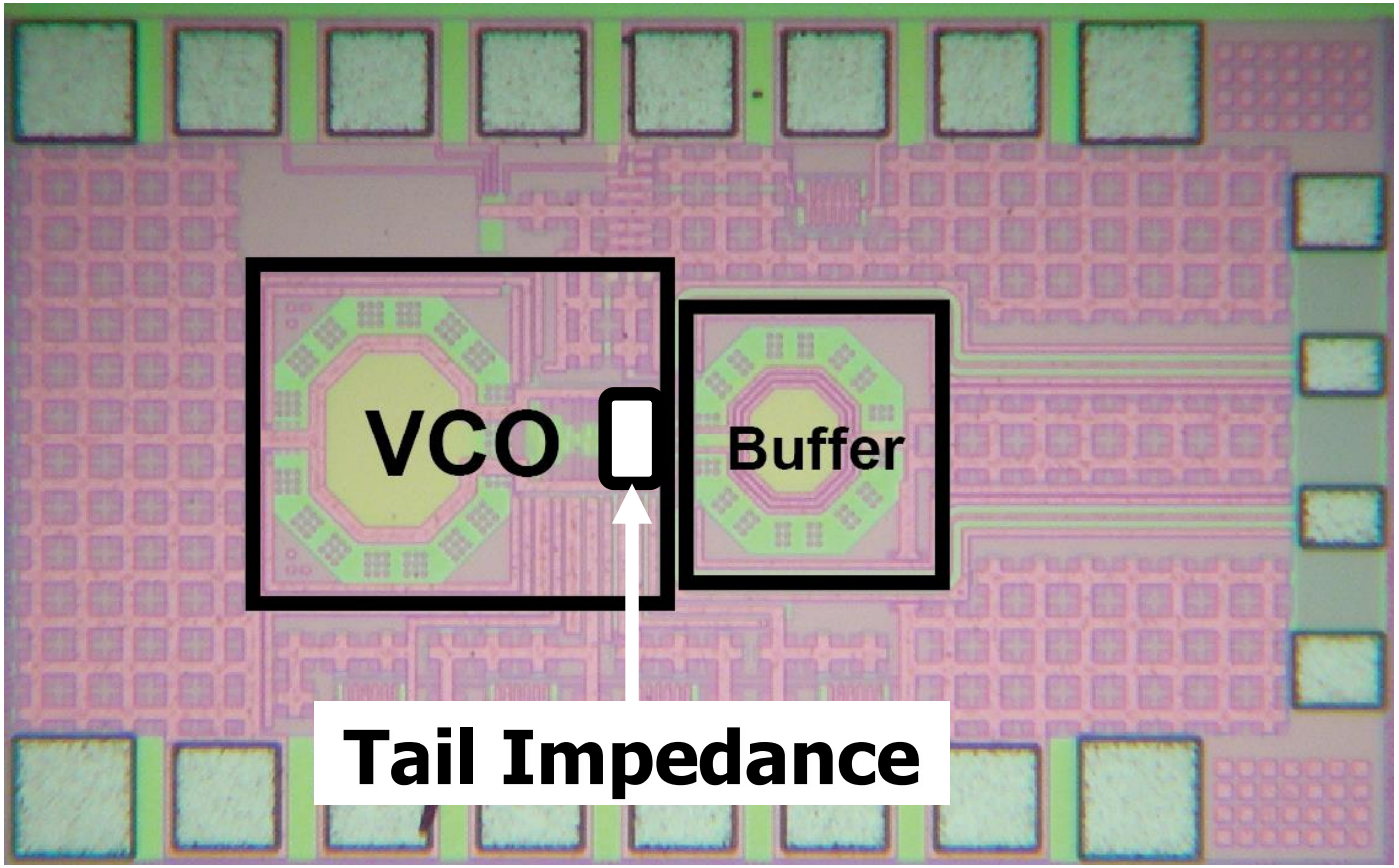
Phase Noise improves 3dB when Z = 60Ω.



Chip Die Photo

65nm CMOS Process

VCO Core : 0.057[mm^2]



20GHz band Comparison

Ref	PN@1MHz [dBc/Hz]	Freq [GHz]	Power [mW]	FoM [dBc/Hz]	Topology (LC-only)
[5]	-101	26.7	21	-176.3	push-push
[6]	-98	18.7	6	-176	PMOS
[7]	-112	19	200	-174.5	Colpitts
[8]	-106	17.9 - 21.2	19.2	-179	Tail Capacitive Feedback
This Work	-105.5	19.3 - 22.4	8.7	-182.4	Class-C with NSM

$$\mathrm{FoM} = \mathrm{PN} - 20\log_{10}\left(\frac{f_{\mathrm{center}}}{f_{offset}}\right) + 10\log_{10}\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right)$$

Conclusion

- **AM-PM Conversion on the cross-coupled pair can be cancelled in proposed circuit.**
- **It improve phase noise performance by 3dB and achieve best Figure of Merit among 20GHz Oscillators.**

References-1

[1] K. Okada, et al., "A 60 GHz 6QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," in 2011 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 160–162.

[2] A. Mazzanti, et al., "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," IEEE Journal of Solid-State Circuits, vol.43, No.12, pp.2716-2729 , Dec. 2008.

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[4] L. Fanori, et al., "Capacitive Degeneration in LC-Tank Oscillator for DCO Fine-Frequency Tuning," IEEE Journal of Solid-State Circuits, vol.45, no.12, pp.2737-2745, Dec. 2010.

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[5] R. Molave, et al., " A 27-GHz Low-Power Push-Push LC VCO with Wide Tuning Range in 65nm CMOS," IEEE Int. Symp. Circuits and Systems, May 2011, pp.1141-1144.

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[7] W. Wang, et al., "A 20GHz VCO and Frequency Doubler for W-band FMCW Radar Applications," IEEE Silicon Monolithic Integrated Circuits in RF Systems, Jan. 2014, pp.104-106.

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