A 20GHz Class-C VCO Using Noise Sensitivity Mitigation Technique

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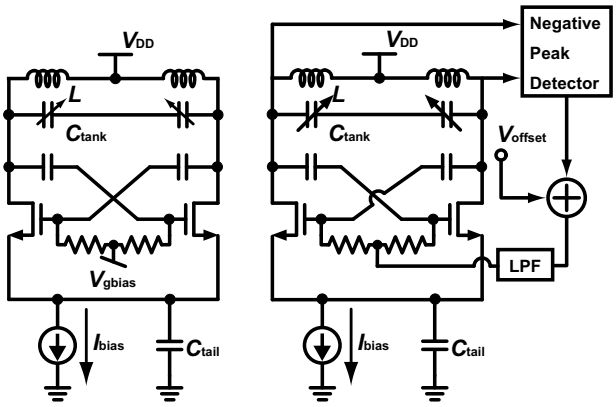
***Abstract*— This paper presents a Class-C VCO with noise sensitivity mitigation technique. Class-C VCO has a large parasitic capacitances between gate and source nodes and this capacitance variation causes a large frequency sensitivity to noise voltage. As a consequence, the noise from gate node become the largest noise contributor. Proposed technique can control this sensitivity by tuning the tail impedance. A 65nm CMOS prototype of the VCO demonstrates oscillation frequency from 19.35 to 22.36 GHz, the phase noise of -105.8 dBc/Hz at 1MHz offset with power dissipation of 8.7mW and Figure-of-Merit of -182.4 dBc/Hz.**

I. Introduction

Oscillators are key components for most of the modern electrical devices. Their output noise which randomly appears in phase is a main performance limiter of a communication systems. Reducing power dissipation has become a crucial design requirement for mobile devices that are not constantly connected to a power source. For both achievement, Class-C VCO [1] in Fig.1(a) is the promising in terms of the effective impulse sensitivity function (ISF). Further Class-C VCO can allocate almost all power to the fundamental frequency component and other harmonic can be negligible. However the necessity to keep the transistors in saturation region for perfect Class-C operation limits the swing magnitude and also causes the start-up difficulty. One breakthrough of this issue is the additional adaptive biasing circuits [2], [3] in Fig.1(b) to operate after oscillation. These circuits initially set high gate voltage for robust start-up and shift to low gate voltage for power reduction after oscillation started. However phase noise performance deteriorates with decreasing the gate voltage because of a quite large cross coupled transistors to provide large trans-conductance during small conduction time.

This paper presents a phase noise degradation mechanism of Class-C VCO and proposes new technique to improve phase noise performance. The detail of relevancy between noise sensitivity and transistor size are investigated in Section II. In next Section, the details of proposed technique and the measurement results are presented.



(a) Class-C VCO (b) adaptive biased Class-C VCO

Fig. 1. The circuit schematics of Class-C VCOs

II. Investigation of Phase Noise Degratation

Several phase noise theories have already been reported and one of a degradation mechanisms is AM-PM conversion on varactor. VCO gain (K_{VCO}) amplifies noises from the charge pump and this effect becomes so crucial with large K_{VCO}. Equation (1) shows quantification of the phase noise degradation by AM-PM conversion.

$$\mathscr{L}(\omega_{\mathrm{offset}}, K_{\mathrm{VCO}}) = 10\log_{10}\left(\frac{K_{\mathrm{VCO}}V_{\mathrm{m}}}{2\omega_{\mathrm{offset}}}\right)^2 \tag{1}$$

where V_{m} is the noise voltage and ω_{offset} is the offset frequency.

A same phenomenon can be observed in gate bias nodes in Class-C VCO. The shift of gate-bias voltage causes frequency shift because parasitic capacitances of the cross-coupled pairs also shift. Here this frequency shift ratio is defined as $K_{\mathrm{V_{GBIAS}}}$.

$$K_{\mathrm{VGBIAS}} = \frac{\partial\omega}{\partial V} = -\frac{\omega_0}{2C}\frac{\partial C_{\mathrm{CCTr}}}{\partial V} \tag{2}$$

where ω_0 is the oscillation frequency and C_{CCTr} is the capacitance of the cross-coupled pairs.

The cross coupled transistors have 4 large parasitic capacitances C_{GS}, C_{GB}, C_{GD} and C_{DB} and we neglect C_{DS} and C_{SB} which are quite smaller than 4 others. This is because a tail transistor of Class-C VCO should be large enough to operate in linear region and the drain voltage of a tail transistors is almost similar to ground potential. Assuming the back gate of transistors is connected to ground, C_{SB} can be negligible. C_{GS}, C_{GB} and C_{DB} are connected serially and only C_{GD} is connected parallel as shown in Fig. 2.

$$C_{CCTr} = \frac{1}{2}C_{GS} + \frac{1}{2}C_{GB} + \frac{1}{2}C_{DB} + 2C_{GD} \tag{3}$$

In Class-C VCO, DC-cut capacitors C_{DC} should be taken into consideration. However C_{DC} are large enough to guarantee large amplitude and we can suppose C_{DC} $>>$ C_{GS} $>$ C_{GD}, C_{GB}, C_{DB}. As a consequence, Equation (3) can also be applied in Class-C VCO. Among these capacitances, the only C_{GS} largely change between off-region and saturation region as shown in Fig. 3. Equation (4) shows the only C_{GS} dominantly affect the capacitance slope of C_{CCTr}.

$$\frac{\partial C_{CCTr}}{\partial V_{GBIAS}} = \frac{1}{2}\frac{\partial C_{GS}}{\partial V_{GBIAS}} \tag{4}$$

Further C_{GS} is expressed as equation (5). The capacitance gap between saturation and off region become larger with increasing size of transistor. Driving with lower gate voltage requires larger width transistor for robust oscillation and a noise sensitivity to the gate noise largely increase in this case.

$$C_{GS} = \begin{cases} \frac{2}{3}WLC_{OX} & (V_{GS} > V_{TH}) \\ WL_{OV}C_{OX} & (V_{GS} < V_{TH}) \end{cases} \tag{5}$$

where W, L is the width and length of the transistors, C_{OX} is the oxidative capacitance, L_{OV} is the length of diffusion overlap and V_{TH} is the threshold voltage.

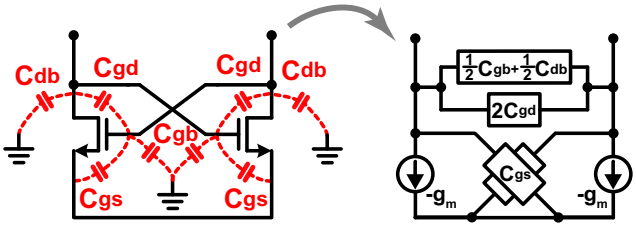


Fig. 2. The contribution of parasitic capacitance

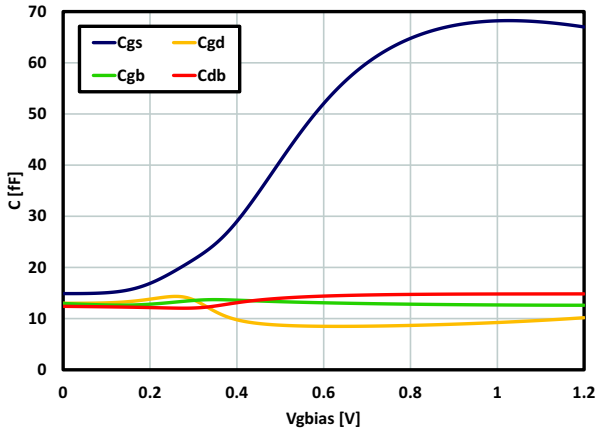


Fig. 3. The voltage dependences of each parasitic capacitances

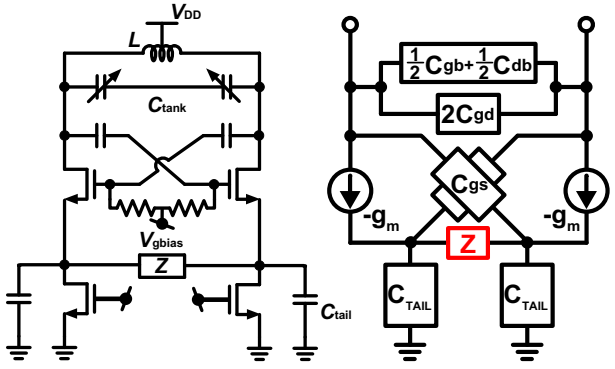
III. Proposed Sensitivity Mitigation Technique

As we discussed in the previous section, shift of the C_{GS} has to be minimized. Fig.4(a) shows the proposed circuit schematic which has the additional impedance between the drain nodes of tail transistors. The effect of C_{GS} to total capacitance changes according to the Z because only C_{GS} is connected to the drain node of the tail transistors. Further C_{TAIL} cannot be negligible in proposed circuits because each drain nodes are not directly connected. Equation (6) shows the coefficient of C_{GS} will be replaced and C_{GS} slope can be controlled by tuning a tail impedance.

$$C'_{GS} = \left\{1 - \frac{g_m Z + \omega^2 C_{GS}(C_{GS} + C_{TAIL})Z^2}{1 + \omega^2 (C_{GS} + C_{TAIL})^2 Z^2}\right\} C_{GS} \tag{6}$$

where Z is the tail impedance, g_m is the transconductance of the cross coupled pairs and C_{TAIL} is the capacitance connected to the drain of tail transistors.

This impedance block is composed of 4 bit switch resistors and can be tuned from 5 ohm to 1000 ohm. The coefficient can largely change when Z is between 10 and 100. Even if only C_{GS} slope become flat, the total slope cannot be flat because the characteristics of other parasitic capacitances become dominant in this case. We have to cancel each parasitic capacitance characteristics by tuning the coefficient of C_{GS}. Fig.5 shows the characteristics of the cross-coupled pairs capacitance in proposed circuits. When Z is 60, the total noise sensitivity can be almost zero. Fig.6 shows the measurement results of this circuits. Compared to conventional Class-C VCO, the proposed method improves 3 dBc/Hz on 1MHz offset frequency.



(a) Schematic (b) Parasitic Cap

Fig. 4. Proposed Class-C VCO

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH RECENTLY REPORTED 20 GHZ LC OSCILLATORS.

Ref.	PhaseNoise[dBc/Hz]	Frequency [GHz]	Power [mW]	FoM [dBc/Hz]	Technology	Topology
[4]	-101@1MHz	26.7	21	-176.3	65nm CMOS	push-push
[5]	-98@1MHz	18.7	6	-176	65nm CMOS	PMOS
[6]	-112@1MHz	19	200	-174.5	0.13um BiCMOS	Colpitts
[7]	-106@1MHz	17.9 - 21.2	19.2	-179	65nm CMOS	Tail Capacitive Feedback
This work w/o NSM	-102.4@1MHz	19.3 - 22.4	8.9	-179	65nm CMOS	Class-C
This work w. NSM	-105.8@1MHz	19.3 - 22.4	8.7	-182.4	65nm CMOS	Class-C with NSM

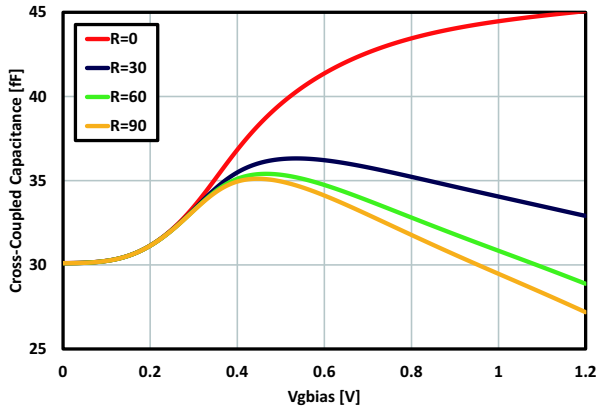


Fig. 5. The capacitance characteristics of the cross coupled pairs in proposed circuits

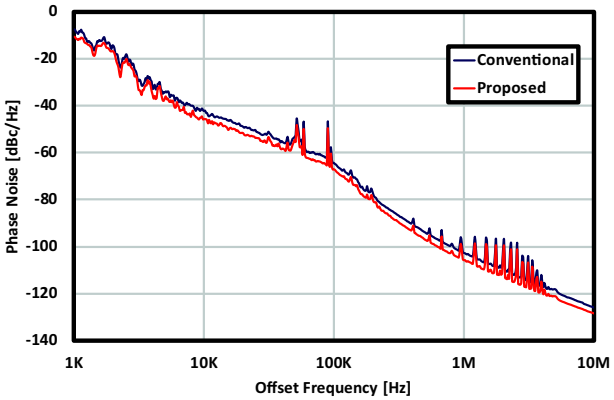


Fig. 6. Phase Noise Comparison

IV. CONCLUSION

The mechanism of phase noise degradation in class-C VCO with low gate voltage is a high frequency sensitivity to gate noises. Especially the shift characteristics of C_{GS} is quite sharp around V_{TH} and capacitance of the cross-coupled pairs also have similar characteristics. The proposed approach which tunes the tail impedance can control this frequency sensitivity and the noise effects from the bias resistors and adaptive biasing circuits can be mitigated. The phase noise performance is improved 3dBc/Hz while consuming only 8.7mW with the area occupation 0.057 mm^2, and the best Figure of Merit in 20GHz band is achieved.

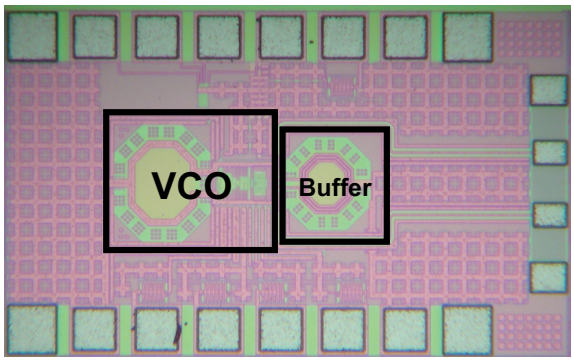


Fig. 7. Chip Photograph

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