Digitally Assisted Wireless Transceivers and Synthesizers

Kenichi Okada

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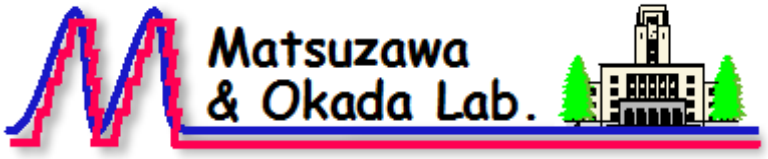
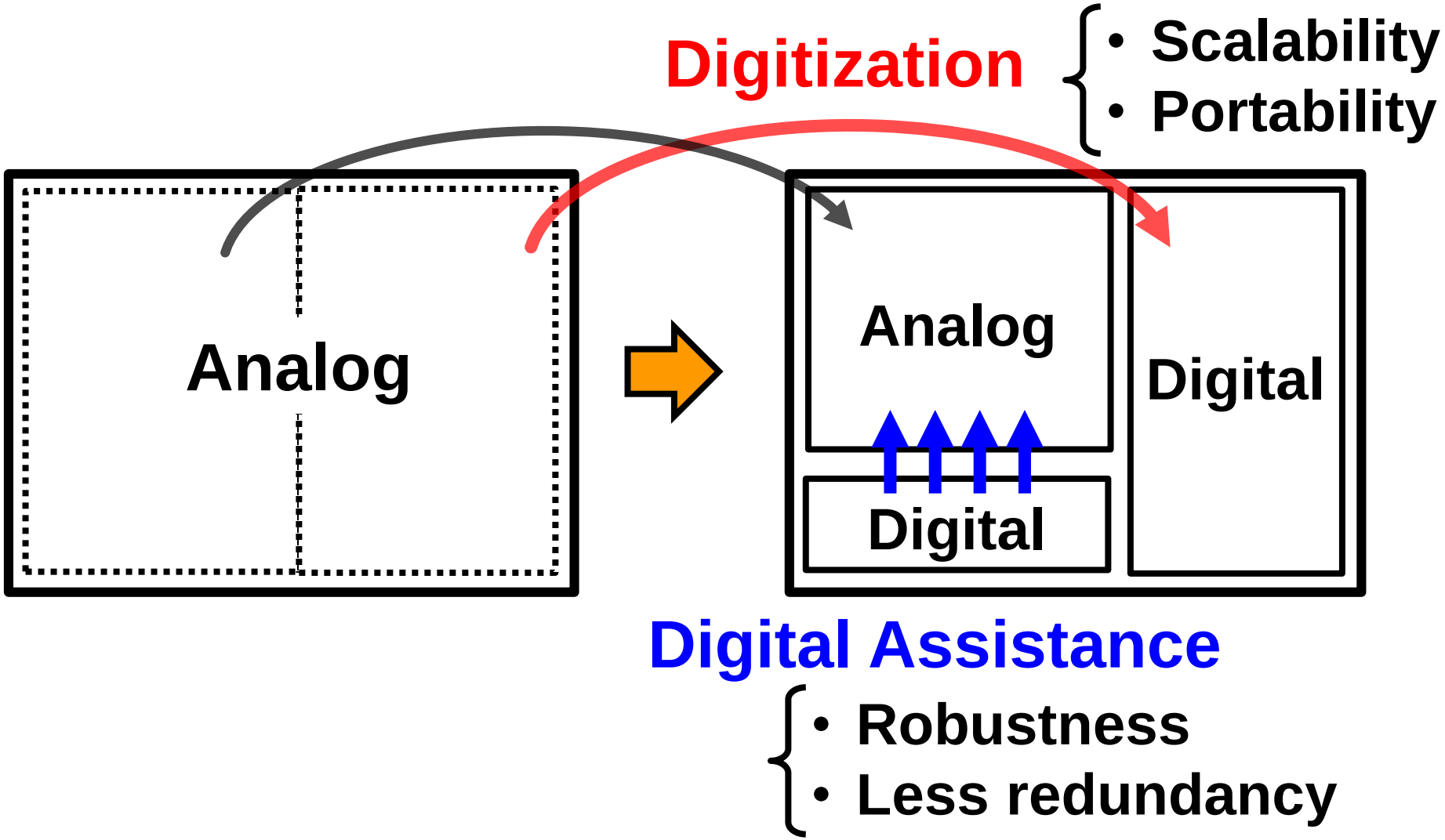


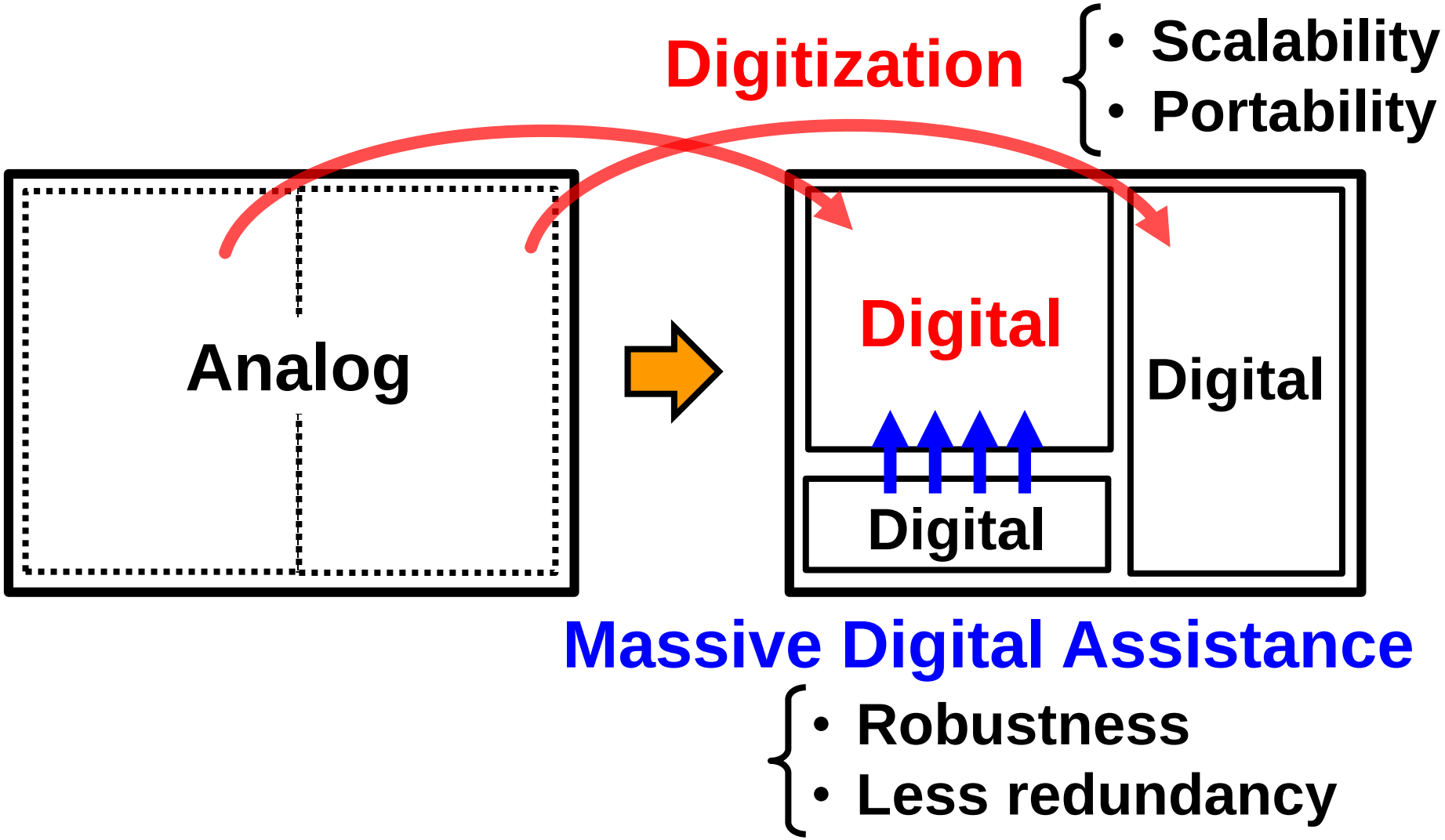
Outline

- Analog to Digital
  - Digitization of Wireless TRX
- Digital Assistance
  - Wireless Transceiver
  - Frequency Synthesizer
- Future Analog Design
  - Synthesizable Analog

Analog to Digital



Further Digitization



Case Study

Partially replaced by pure digital-domain "calculation"

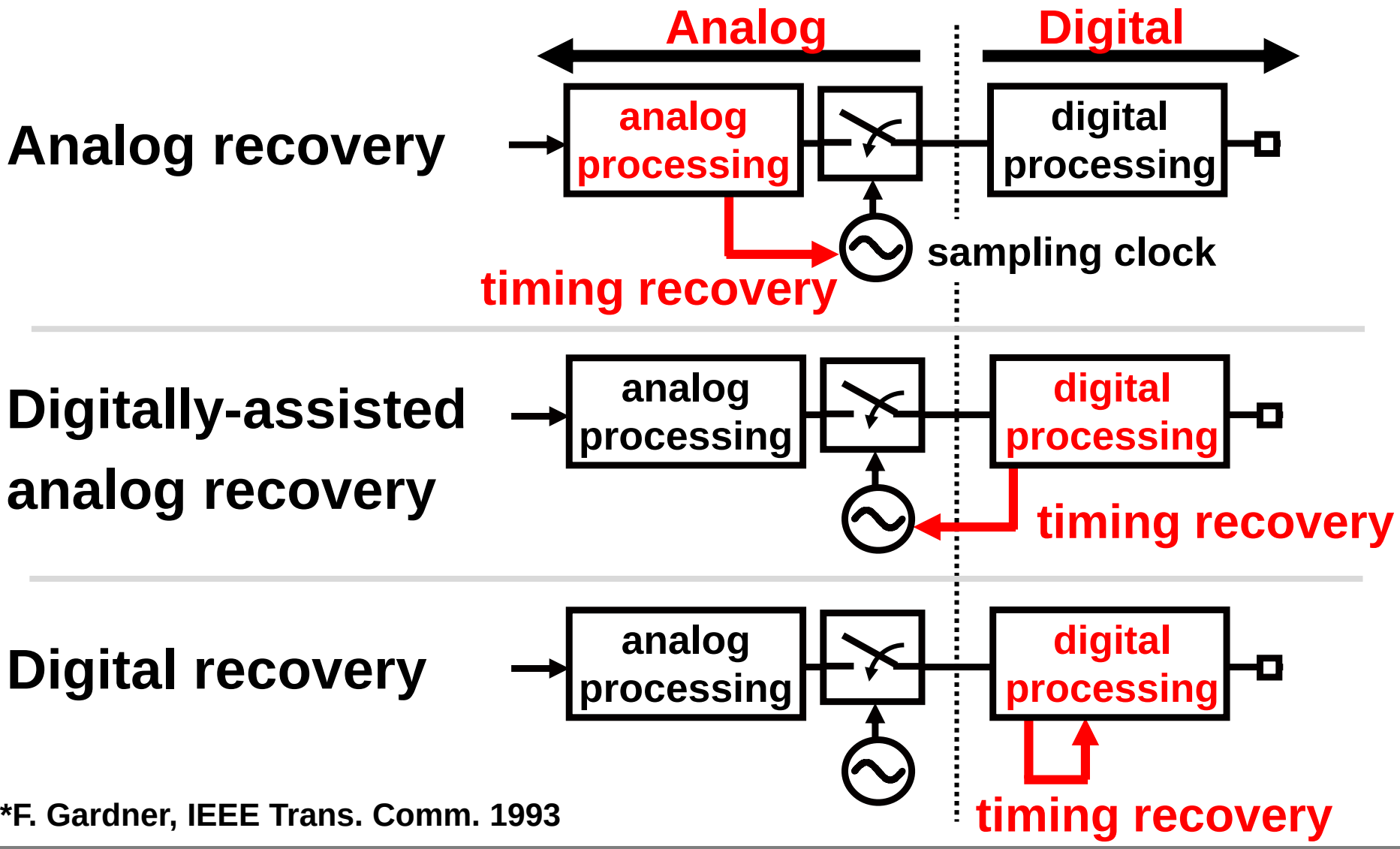
(NOT time-domain analog processing)

- **Filter: LPF in AD-PLL, LPF in wireless TX**
- **Equalizer: FIR in wireless, OFDM**
- **PLL: carrier and timing recovery in wireless RX**
- **Mixer: Low-IF transceiver**

Only analog-domain

- **Oscillator: Clock generation**
- **Data converter: V-to-D, D-to-V, D-to-I, C-to-D,..**
- **Analog amplifier: voltage-to-voltage**

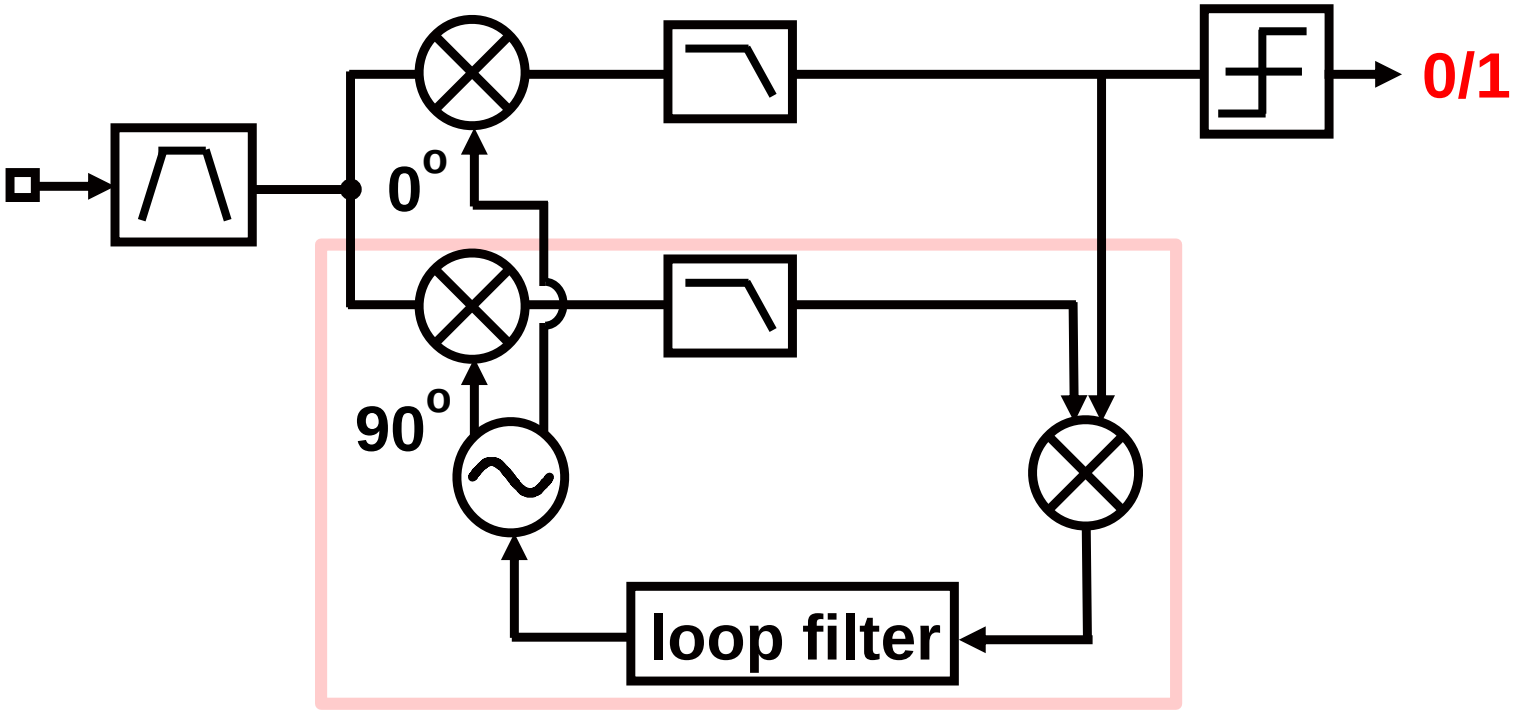
History of Timing Recovery



*F. Gardner, IEEE Trans. Comm. 1993

Analog Demodulator

Costas-loop for BPSK

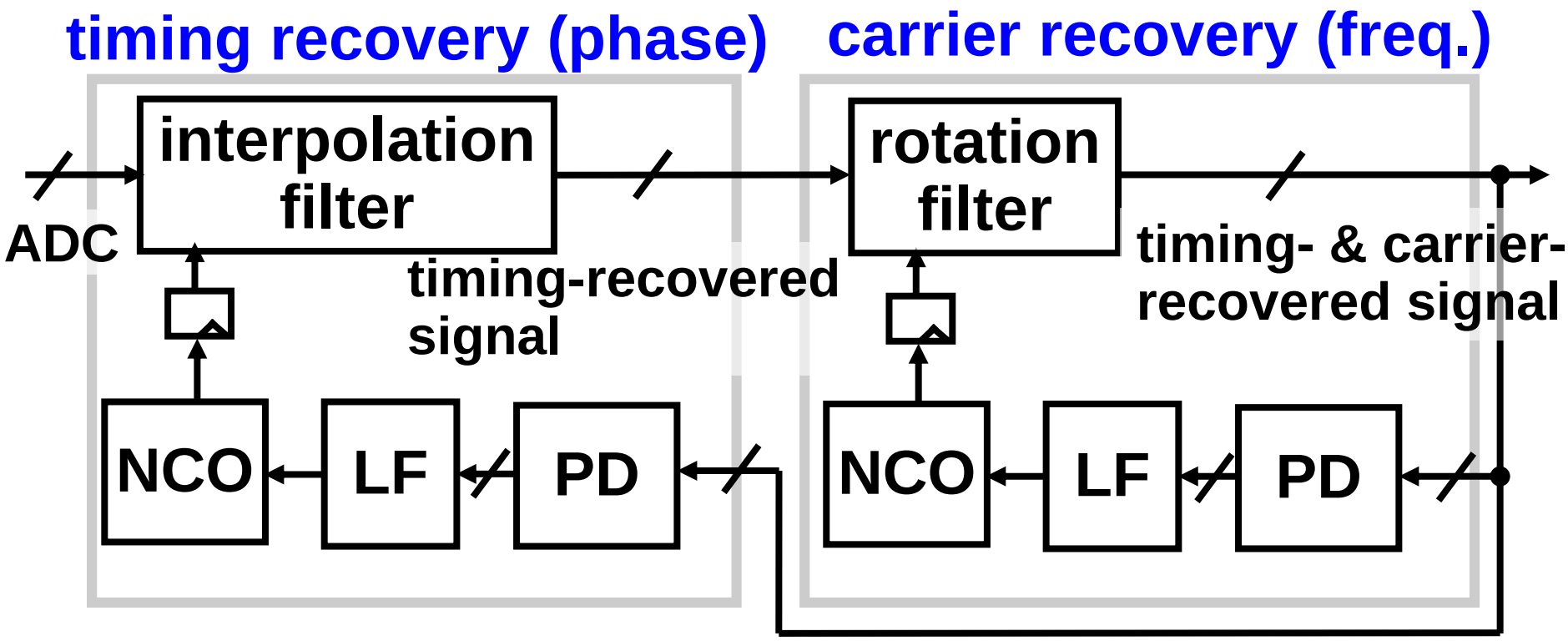


timing recovery loop (carrier & phase)

*H. Suzuki, *et al*., IEEE Trans. VT 1985

Digital Carrier and Timing Recovery

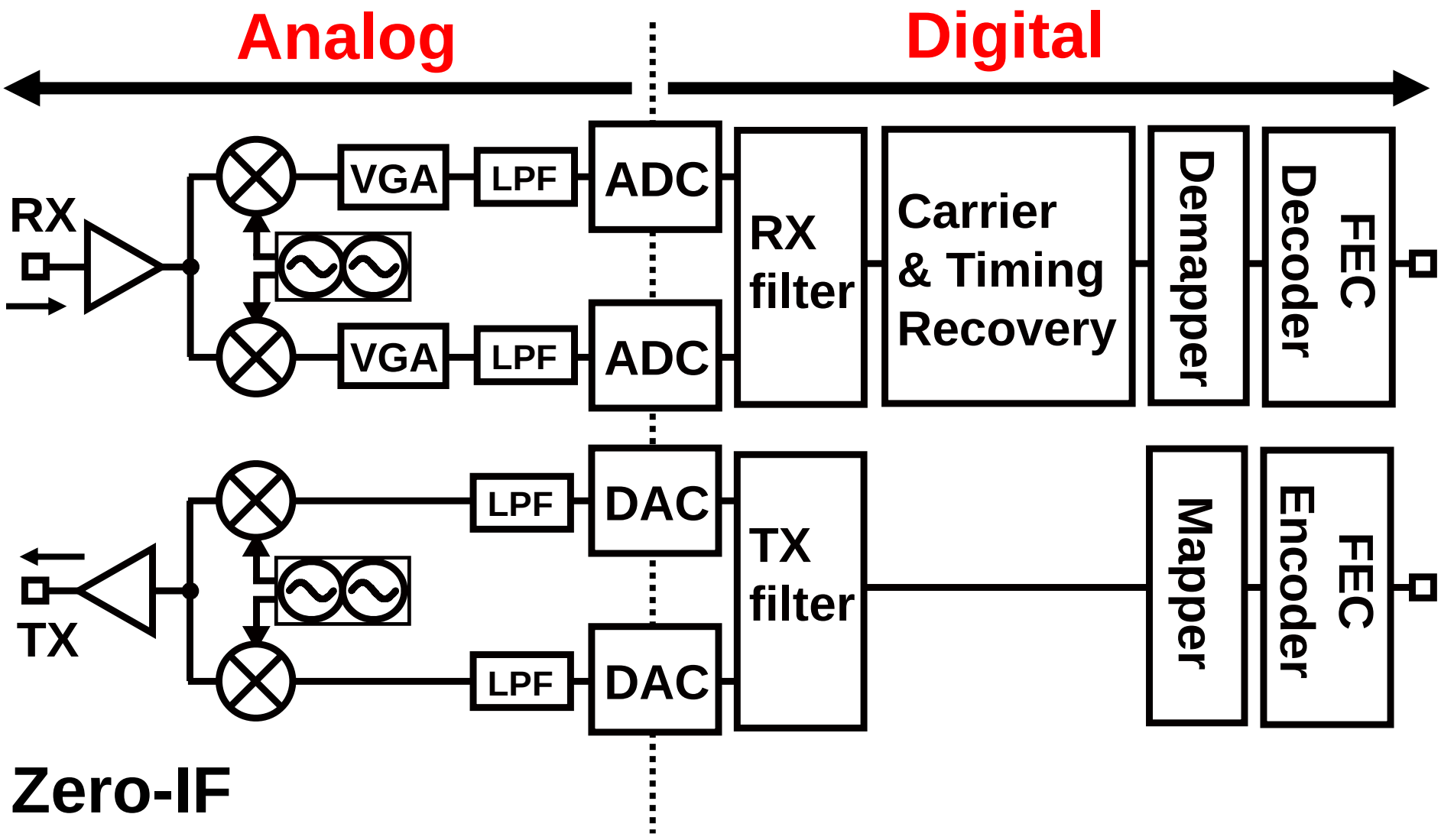
Everything is implemented in digital domain.



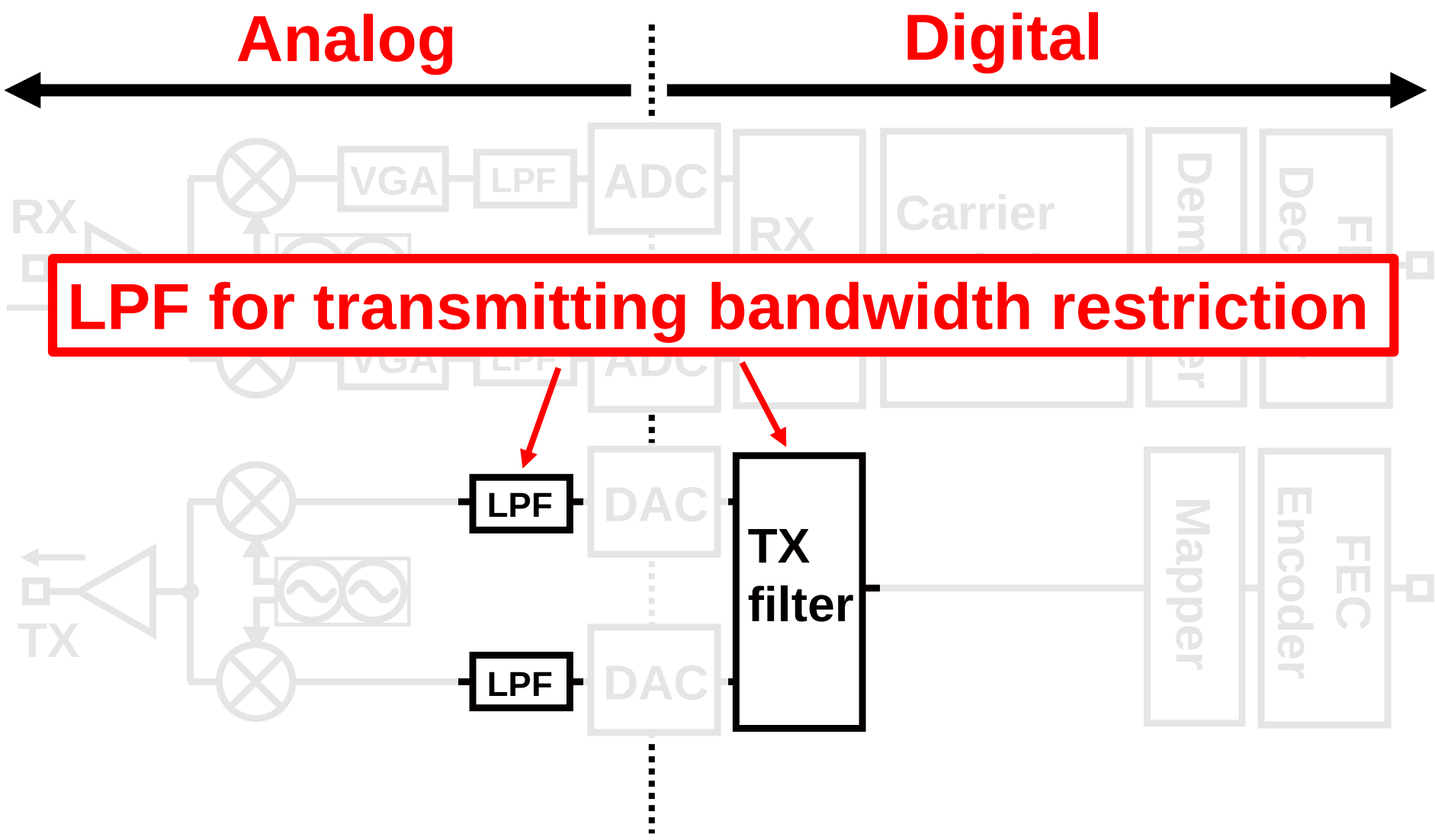
NCO: Number-Controlled Oscillator
LF: Loop Filter
PD: Phase Detector

*F. Gardner, IEEE Trans. Comm. 1993

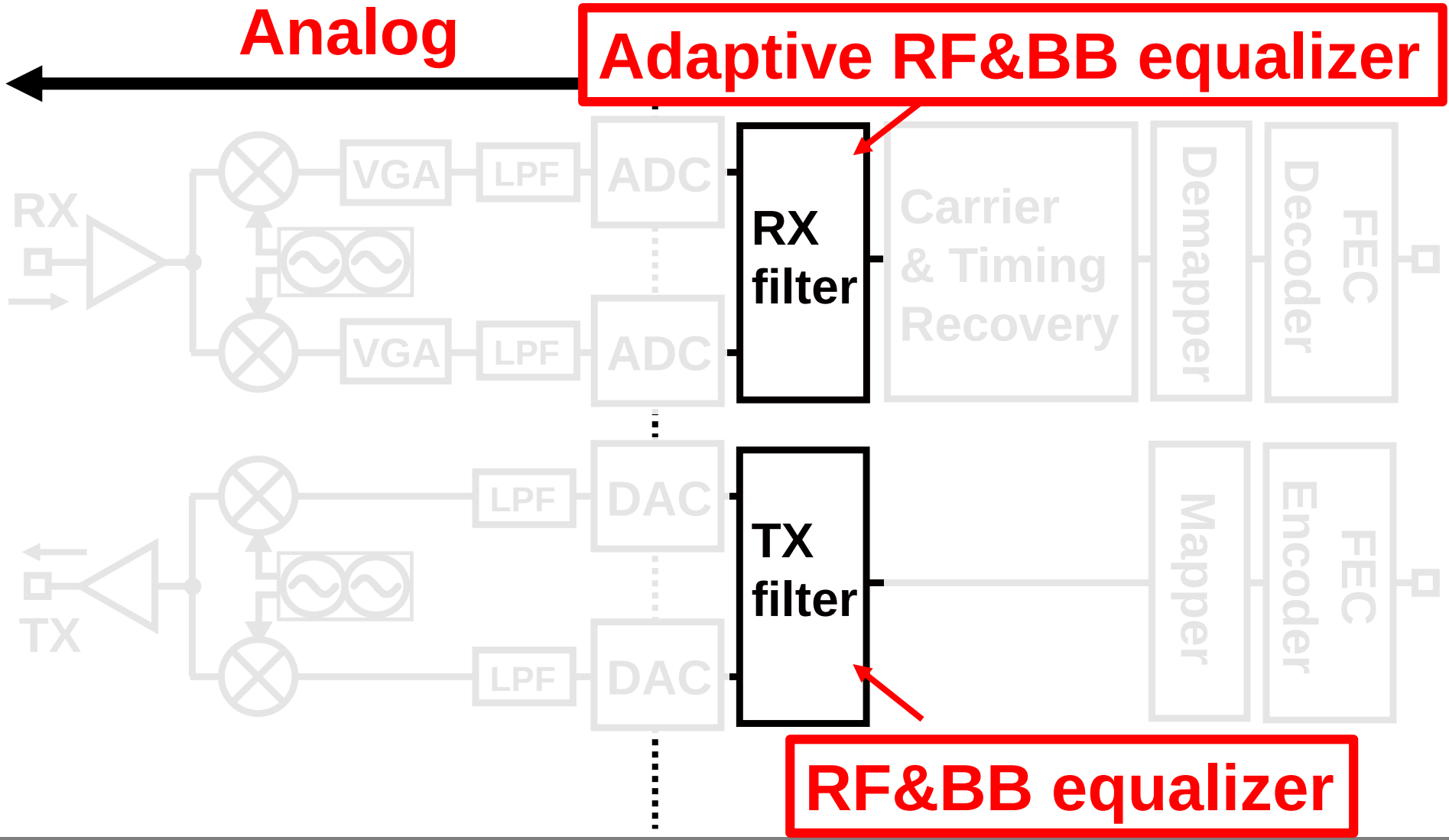
Recent Digital Transceiver



Digital LPF in Wireless

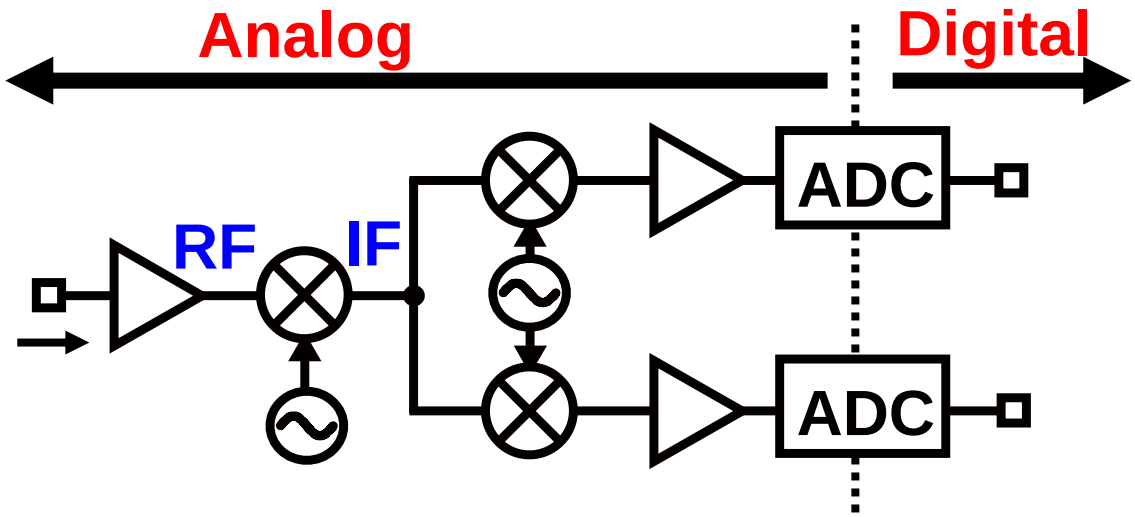


Digital Equalizers in Wireless



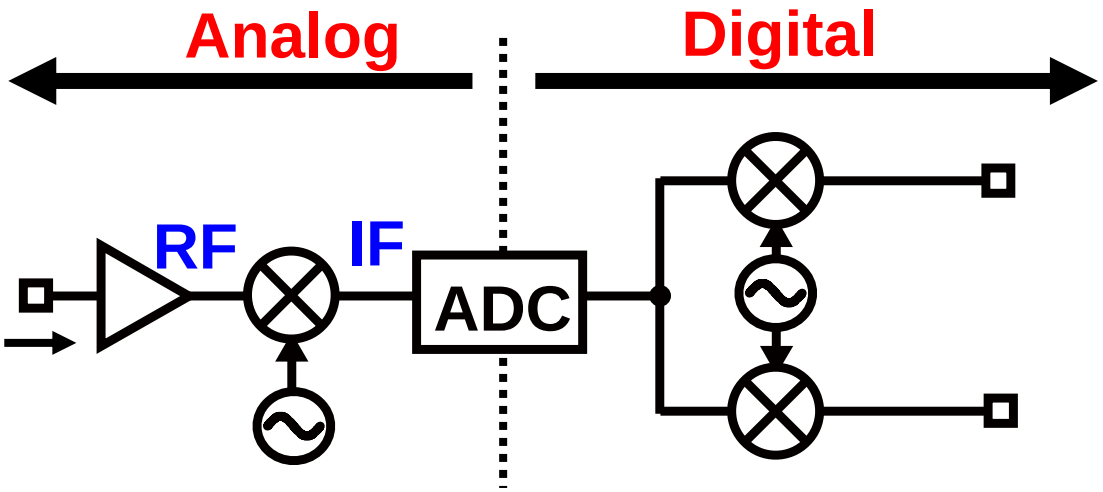
Digitization of IF Mixer

Hetero-dyne RX



Low-IF RX

- Very common for BT
- 1/f noise
- Overhead for ADC



Aim of This Talk

- **Digitization**
  - **Wireless transceiver is a good example of digitized analog circuit. (for hinting)**
- **Digital assistance**
  - **Digital calibration/compensation is implemented in a system level to satisfy complicated requirements for wireless system.**
  - **Mutual re-use of TX and RX for calibration**
- **Digitally-designed analog**
  - **Toward "Synthesizable Analog Circuit"**

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Impairments in Wireless Transceiver

Mismatch in differential block

- **DC offset in RX**
- **IIP2 in RX**
- **LO leakage in TX**

Mismatch btw I and Q blocks

- **Image signal**
- **Analog filter BW (LPF)**

Non-linearity

- **IMD in PA**

PVT variation

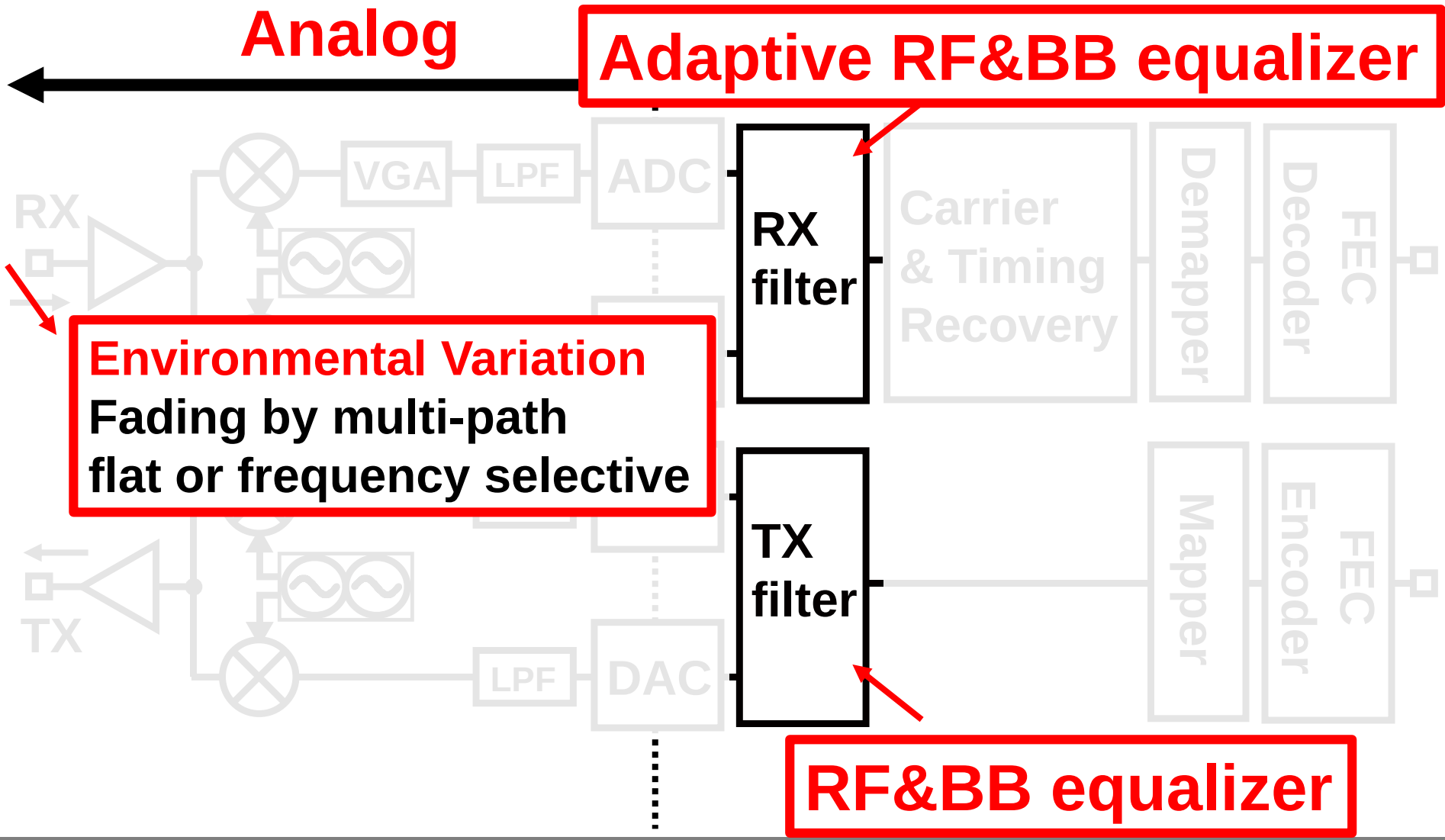
- **Gain control**
- **Power control**
- **VCO LC tank**
- **ILFD/ILO**

Environmental variation

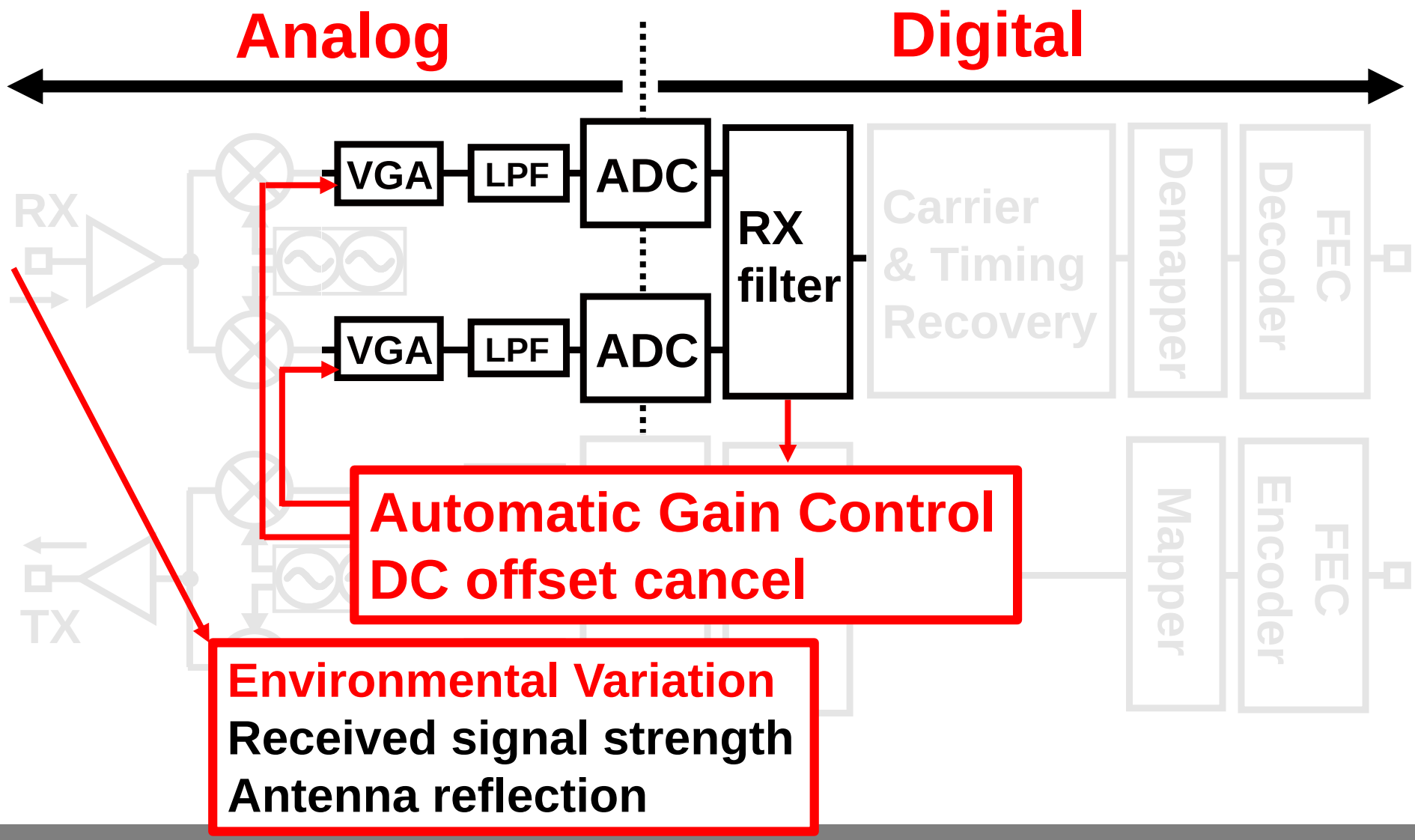
- **TX-to-RX distance**
- **Fading**
- **Antenna reflection**

***A. Jerng, "Digital Calibration for RF Transceivers," ISSCC 2012, Tutorial 9**

Digital Equalizers



Automatic Gain Control (AGC)



I/Q Mismatch

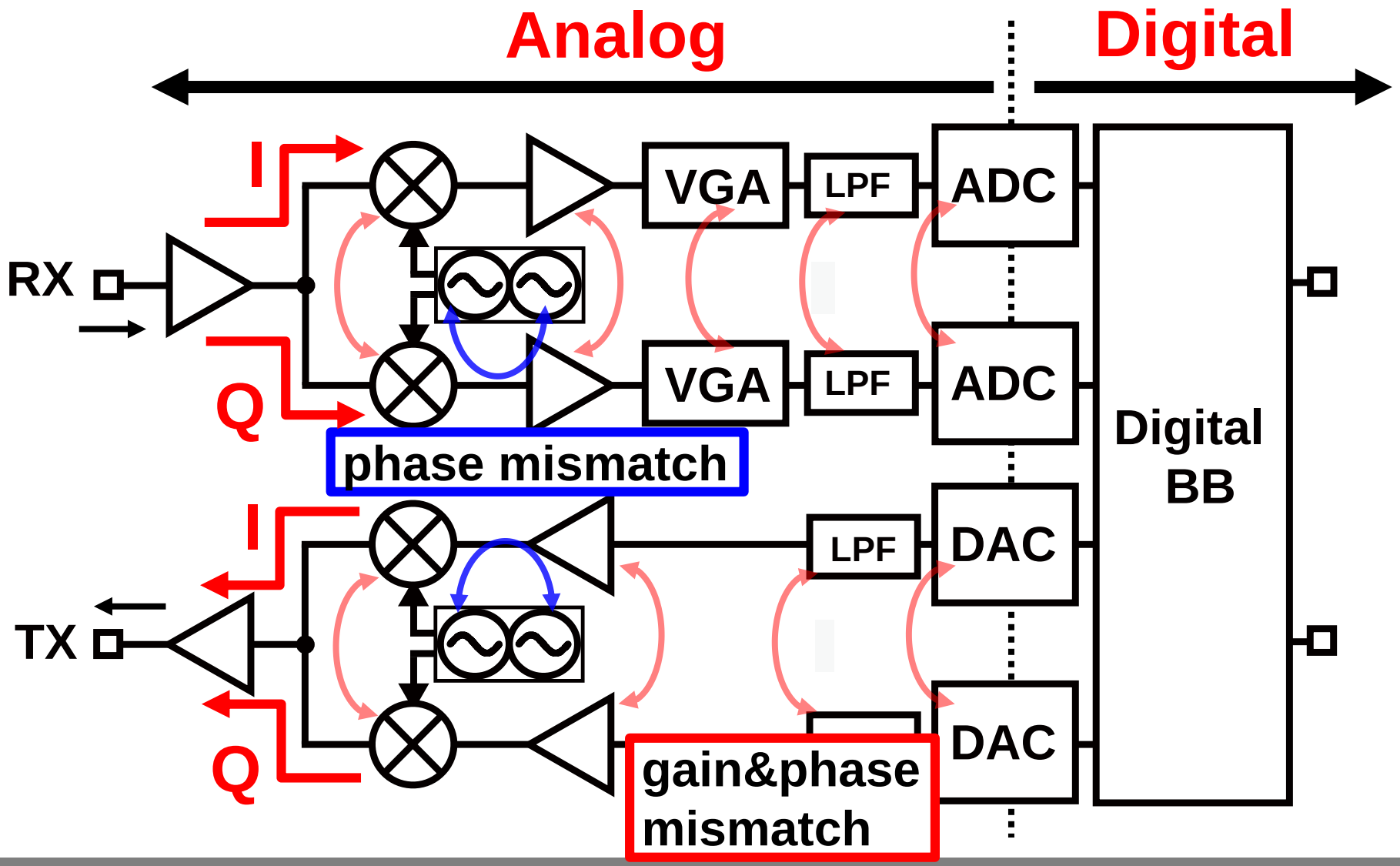

Analog
Digital
I
Q
RX
VGA
LPF
ADC
VGA
LPF
ADC
phase mismatch
Digital
BB
I
Q
TX
LPF
DAC
DAC
gain&phase
mismatch

Image Rejection Ratio (IMRR)

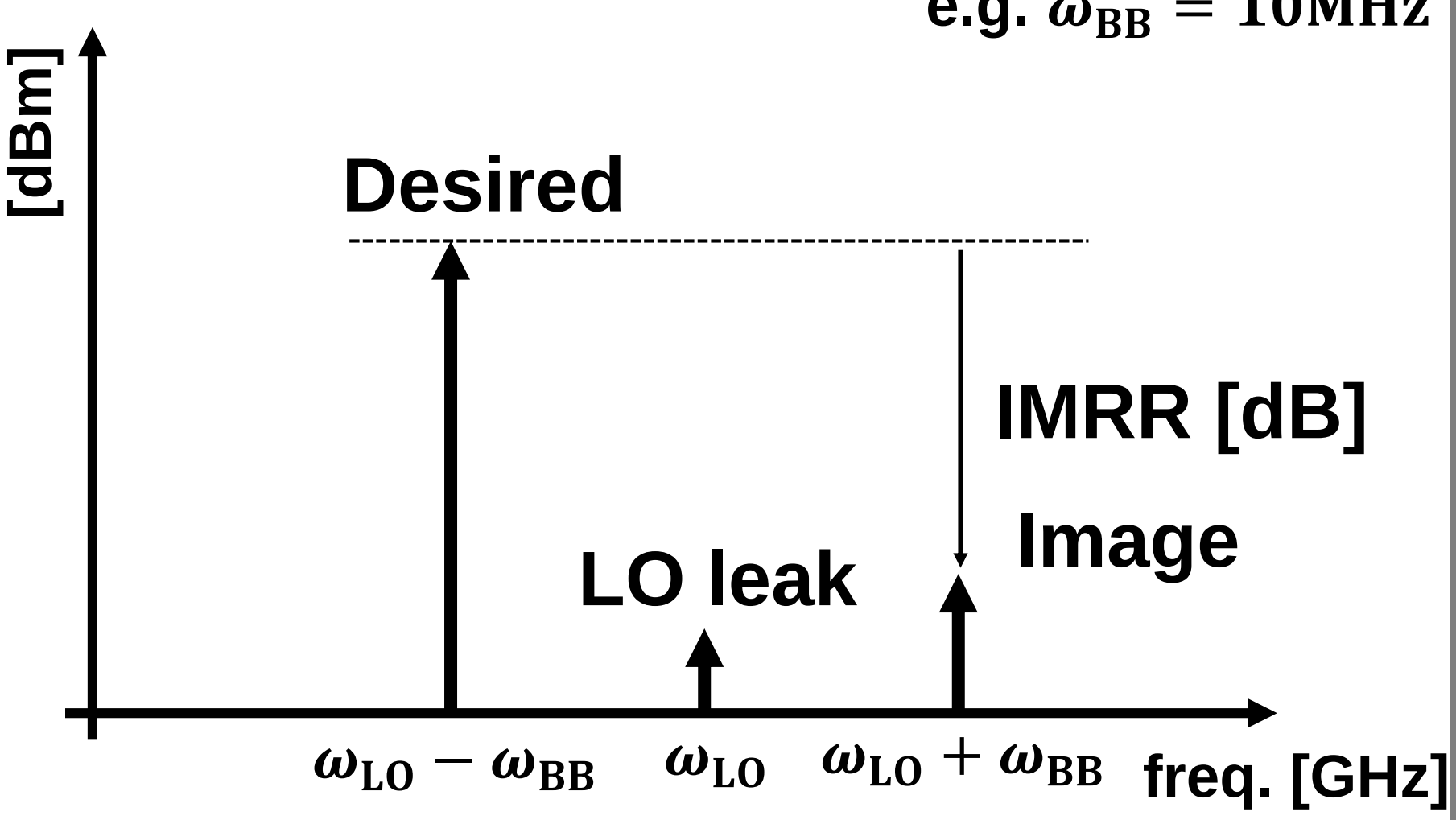


Image for Modulated Sig.

I/Q mismatch degrades SNR.

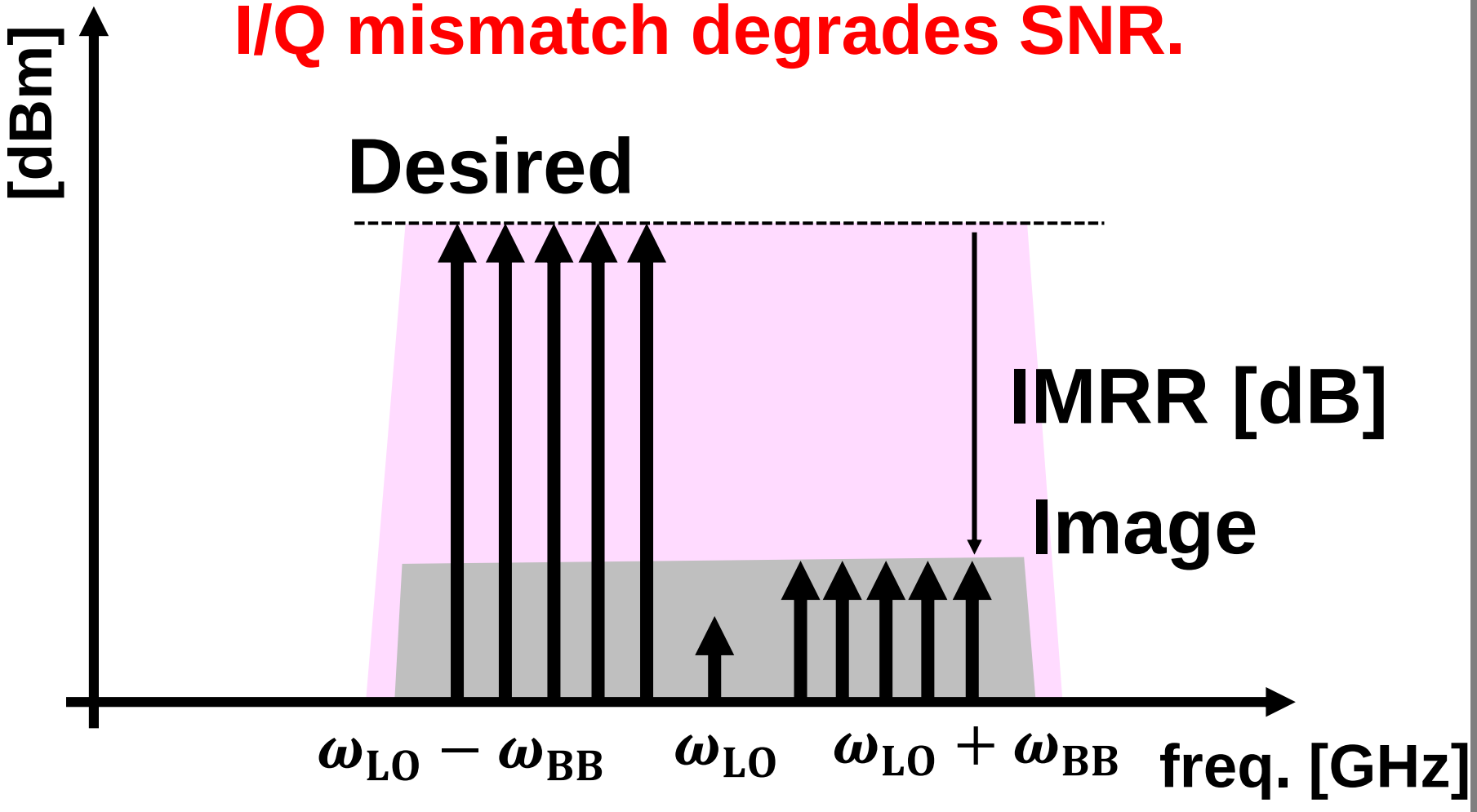
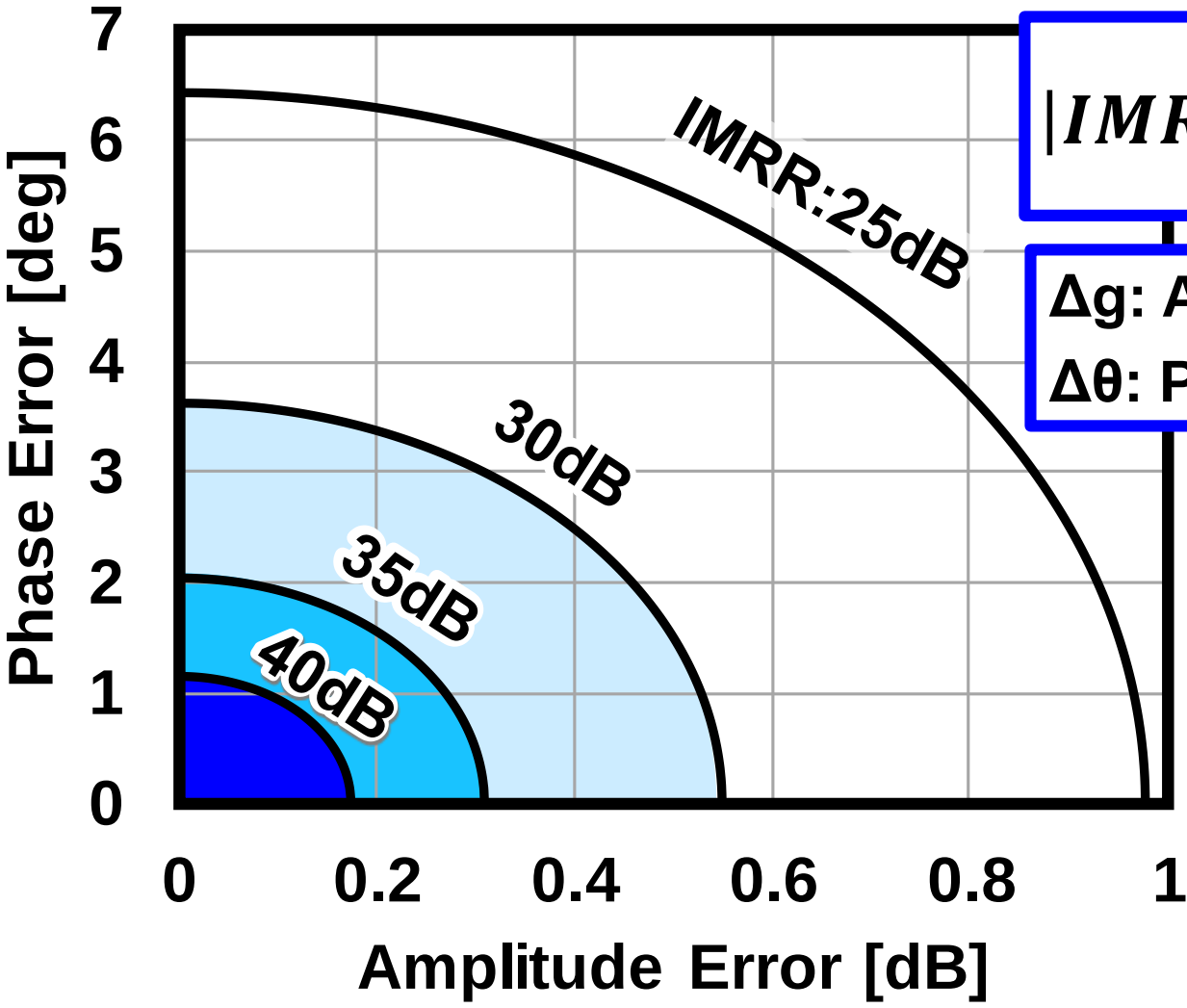


Image Rejection Ratio (IMRR)



$$|IMRR| \approx \left|\frac{\Delta g^2 + \Delta\theta^2}{4}\right|$$

Δg: Amplitude error ratio

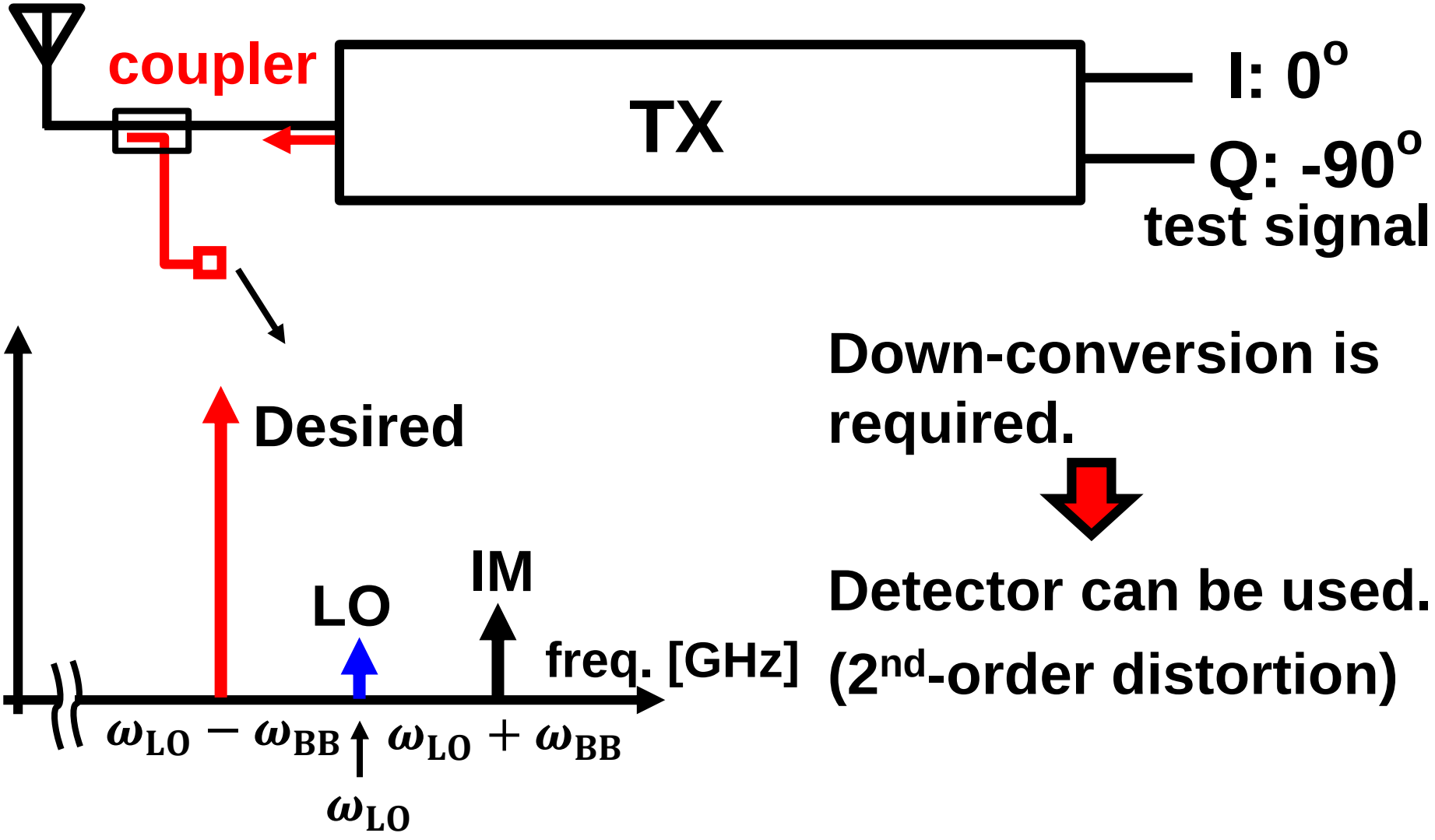
Δθ: Phase error

Target:

0.2dB, 1.0degree

for IMRR of 35dB

TX IMRR Calibration

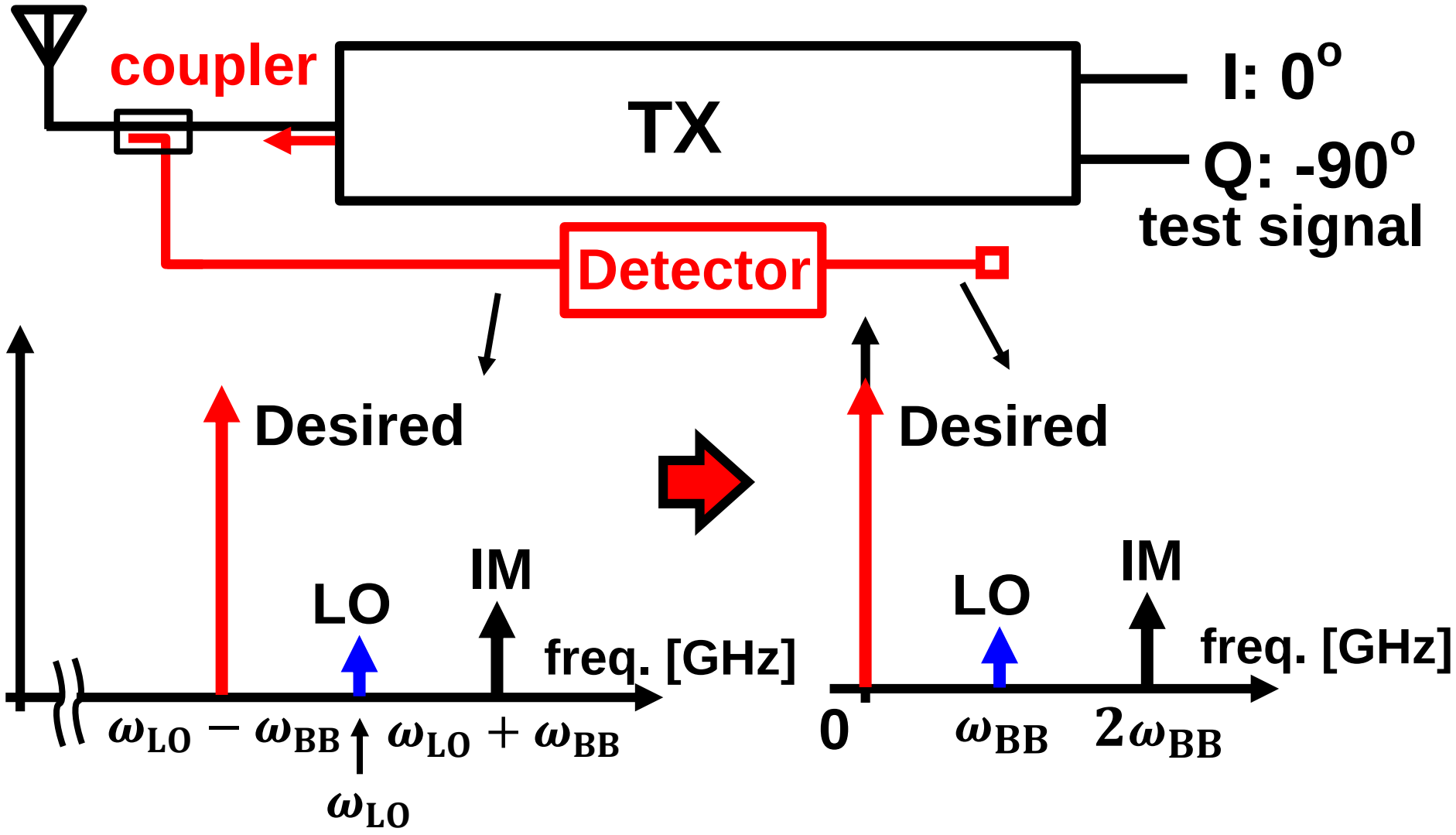


Down-conversion is required.

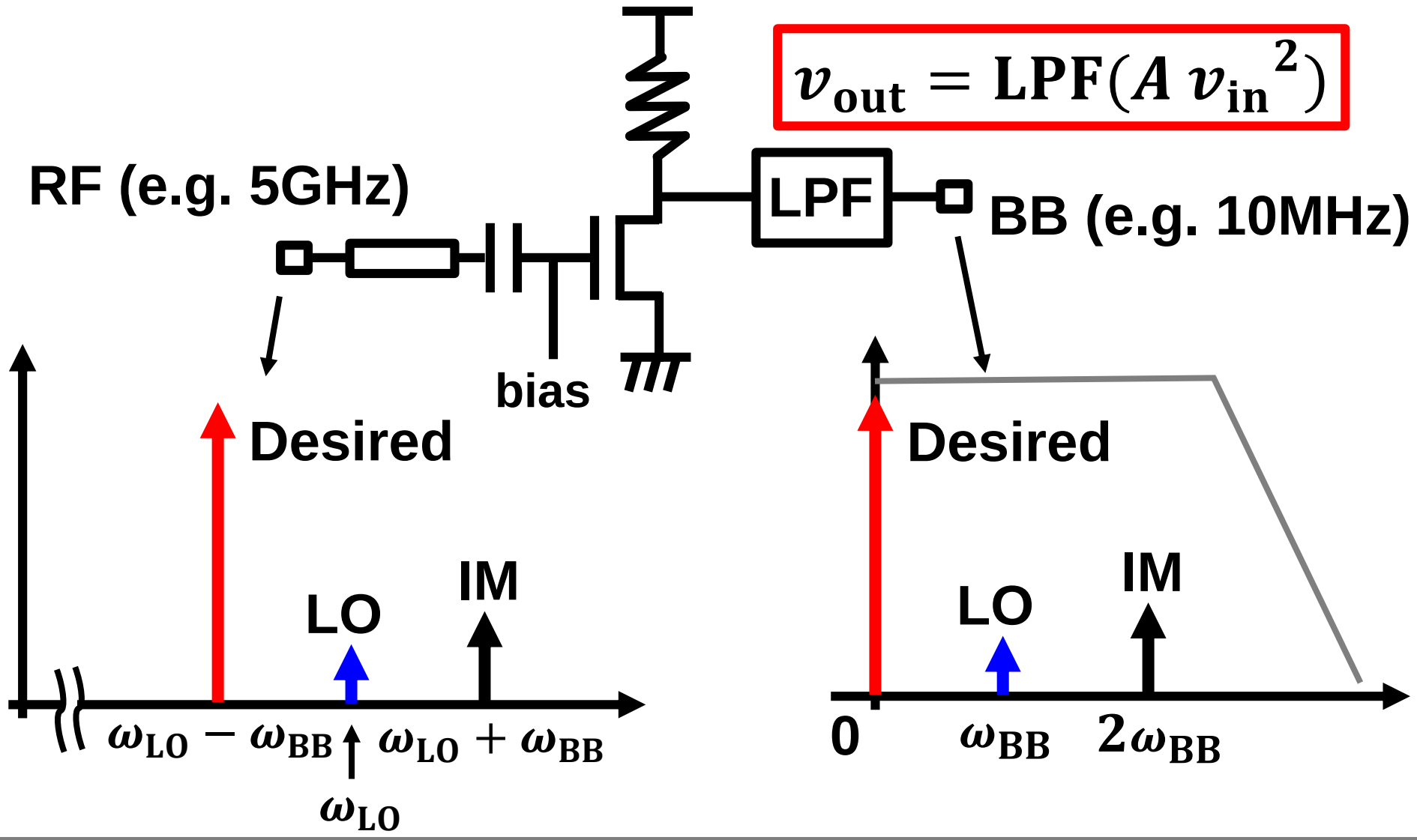
Detector can be used.

(2nd-order distortion)

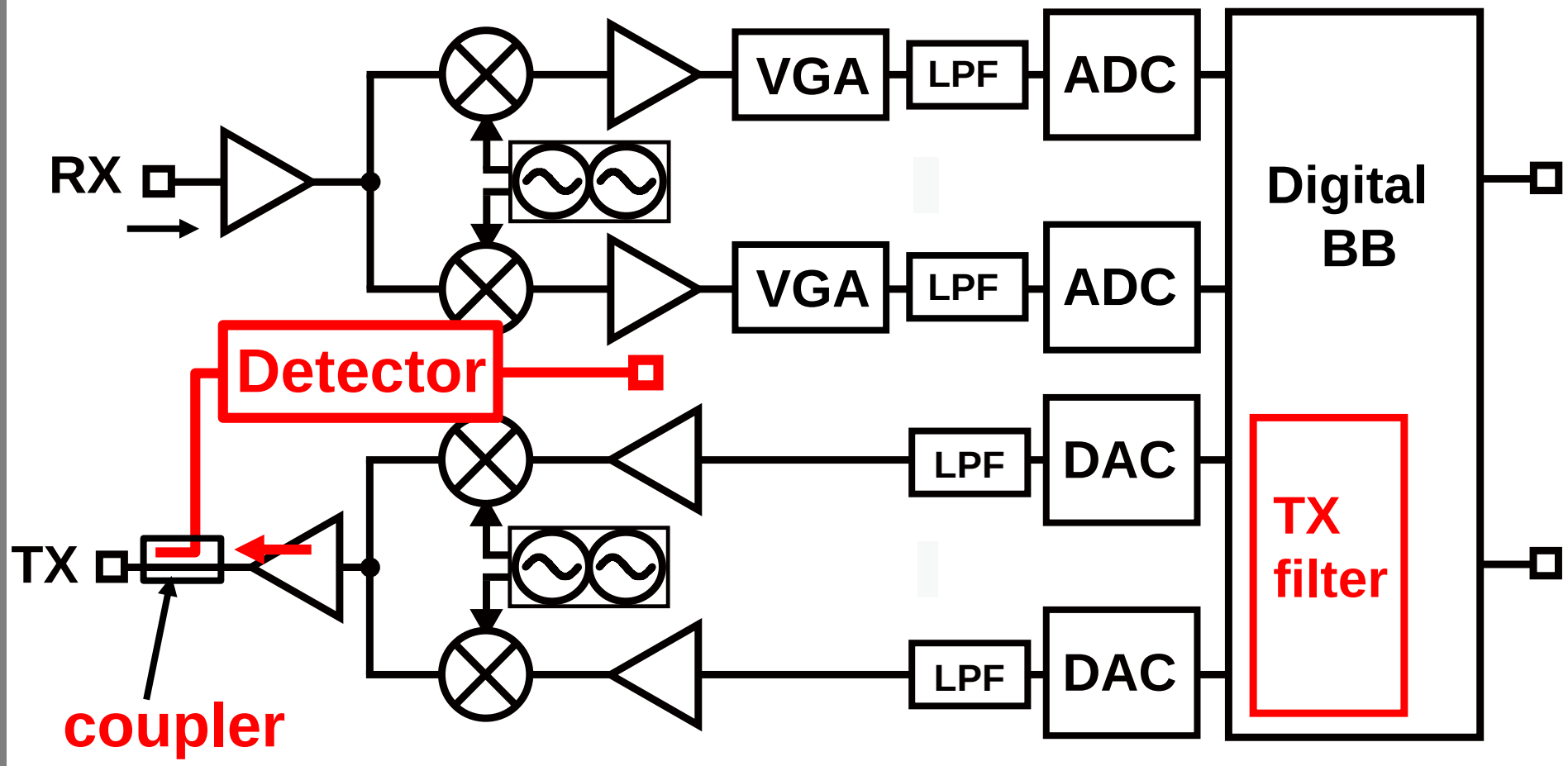
TX IMRR Calibration



Detector

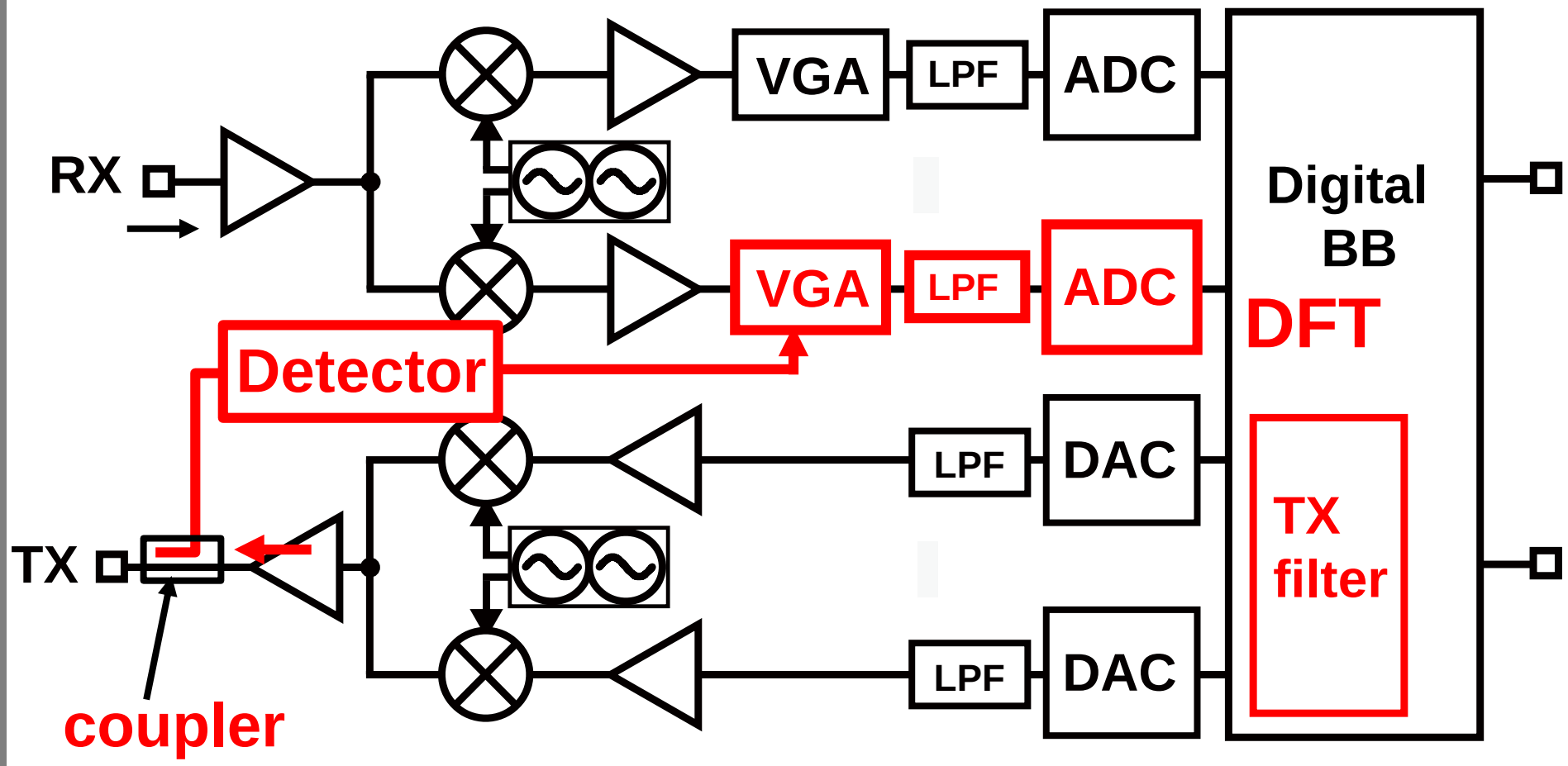

$v_{out} = \mathrm{LPF}(A\, v_{in}^{\,2})$
RF (e.g. 5GHz)
LPF
BB (e.g. 10MHz)
bias
Desired
LO
IM
$\omega_{LO} - \omega_{BB}$
ω_{LO}
$\omega_{LO} + \omega_{BB}$
Desired
LO
IM
0
ω_{BB}
$2\omega_{BB}$

I/Q Mismatch Calibration by Loop-back



- I/Q Amplitude offset
- I/Q Phase offset

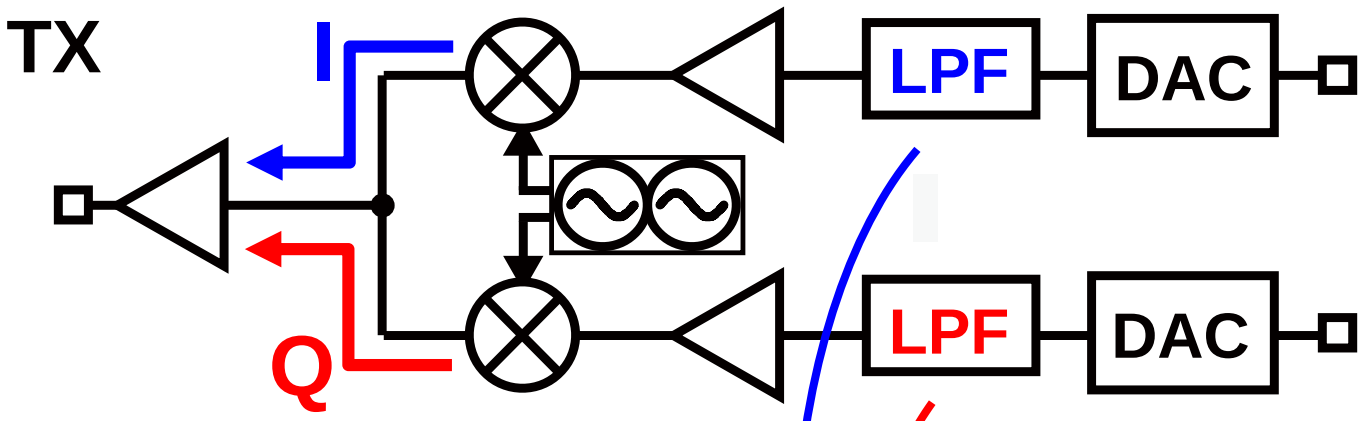
I/Q Mismatch Calibration by Loop-back

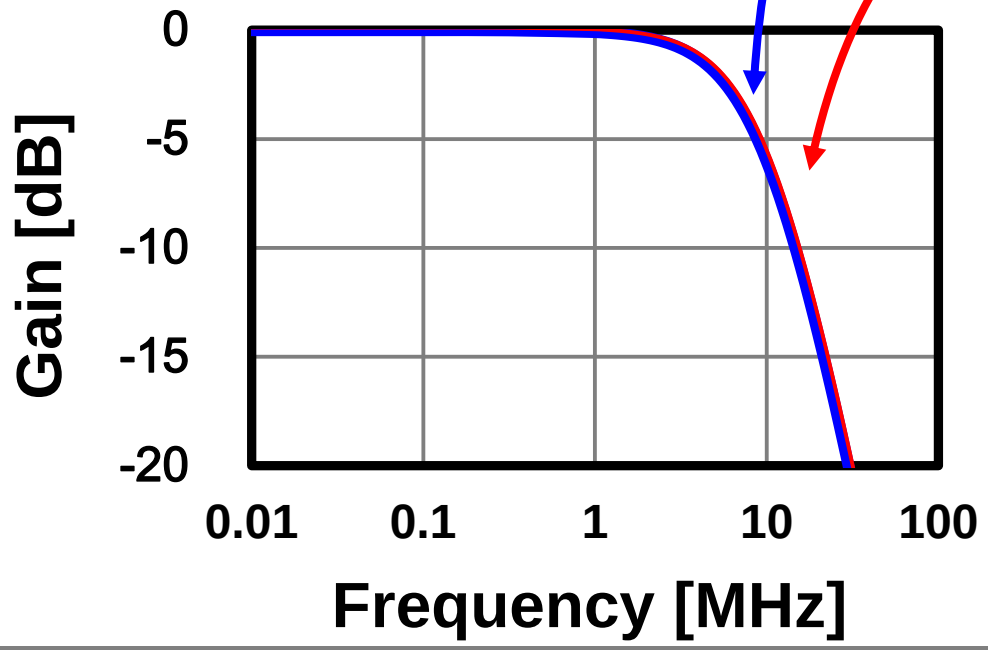


- I/Q Amplitude offset
- I/Q Phase offset

*Iason Vassiliou, *et al.*, IEEE JSSC 2003.

Frequency-Dependent I/Q Mismatch

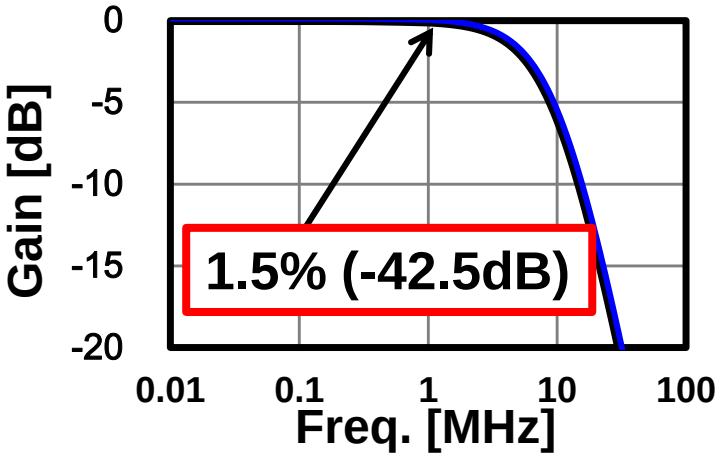


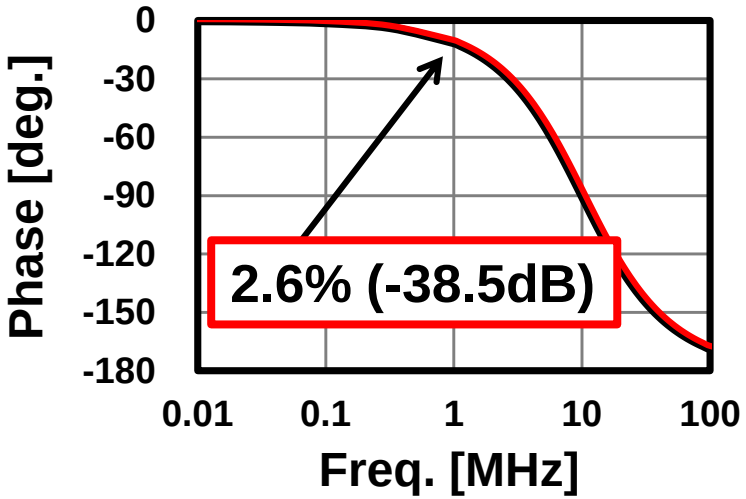


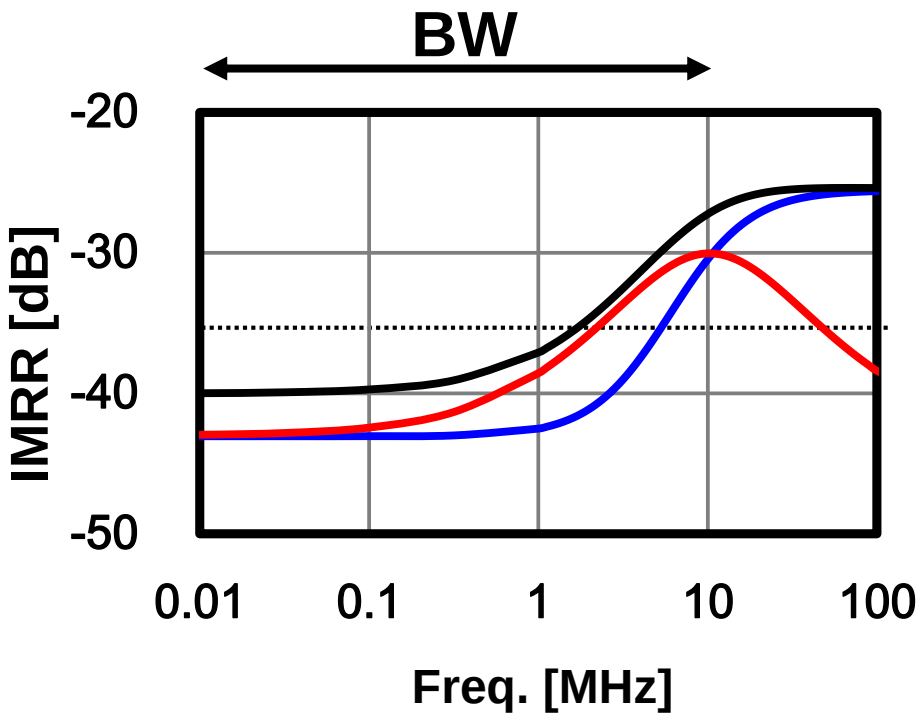
5% cut-off mismatch causes a serious frequency-dependent I/Q mismatch.

Frequency-Dependent IMRR

Gain/phase mismatch can be frequency-dependent.







5% cut-off frequency mismatch

-37dB@1MHz, -27dB@10MHz

Key Idea of Wireless Calibration

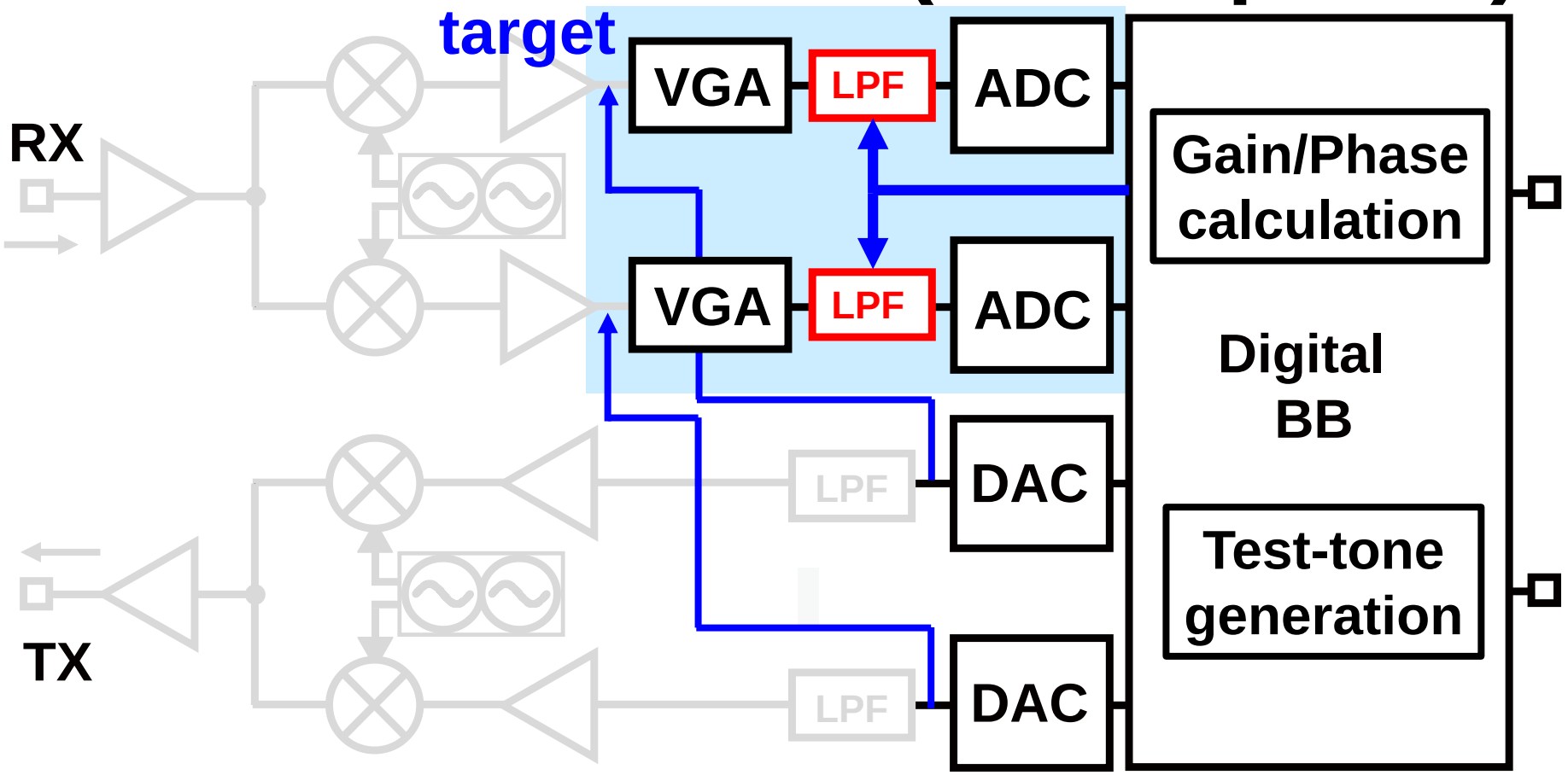
Self-calibration with less additional blocks
Reuse of TRX each other

TX = Signal Generator for RX calibration
RX = Spectrum Analyzer for TX calibration

Overall Procedure of TRX Calibration

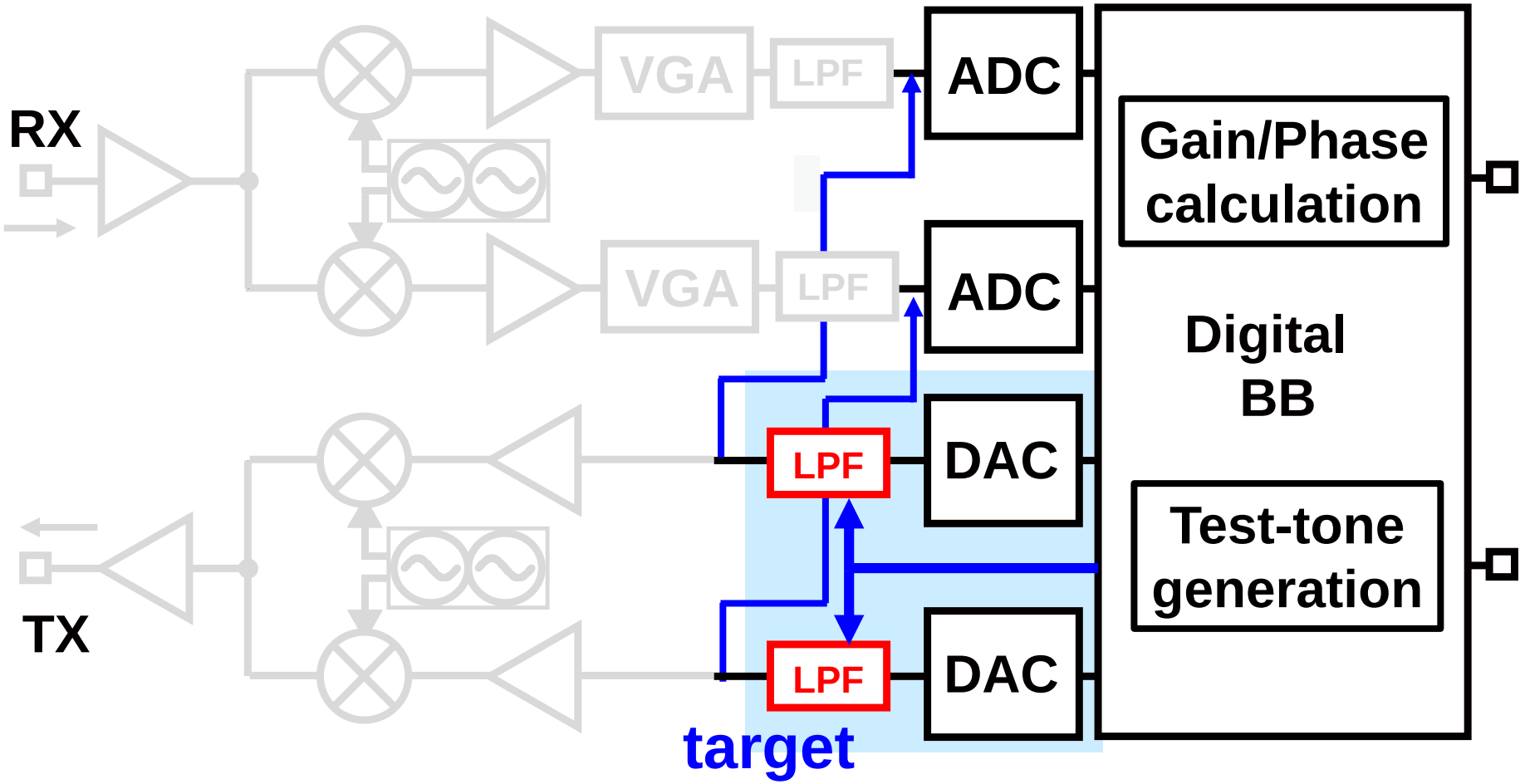
1. **RX BB LPF Calibration (using TX BB)**
   - I/Q gain mismatch
   - LPF cut-off mismatch (including VGA and ADC)
2. **TX BB LPF Calibration (using RX BB)**
   - I/Q gain mismatch
   - LPF cut-off mismatch
3. **TX I/Q Calibration (using detector and RX BB)**
   - Impairments of mixer, LO, RF I/Q amps., etc
   - compensated by digital BB
4. **RX I/Q Calibration (using TX)**
   - Impairments of mixer, LO, RF I/Q amps., etc
   - compensated by digital BB

RX Filter Calibration (BB loopback)



VGA and ADC are also included in RX BB calibration.

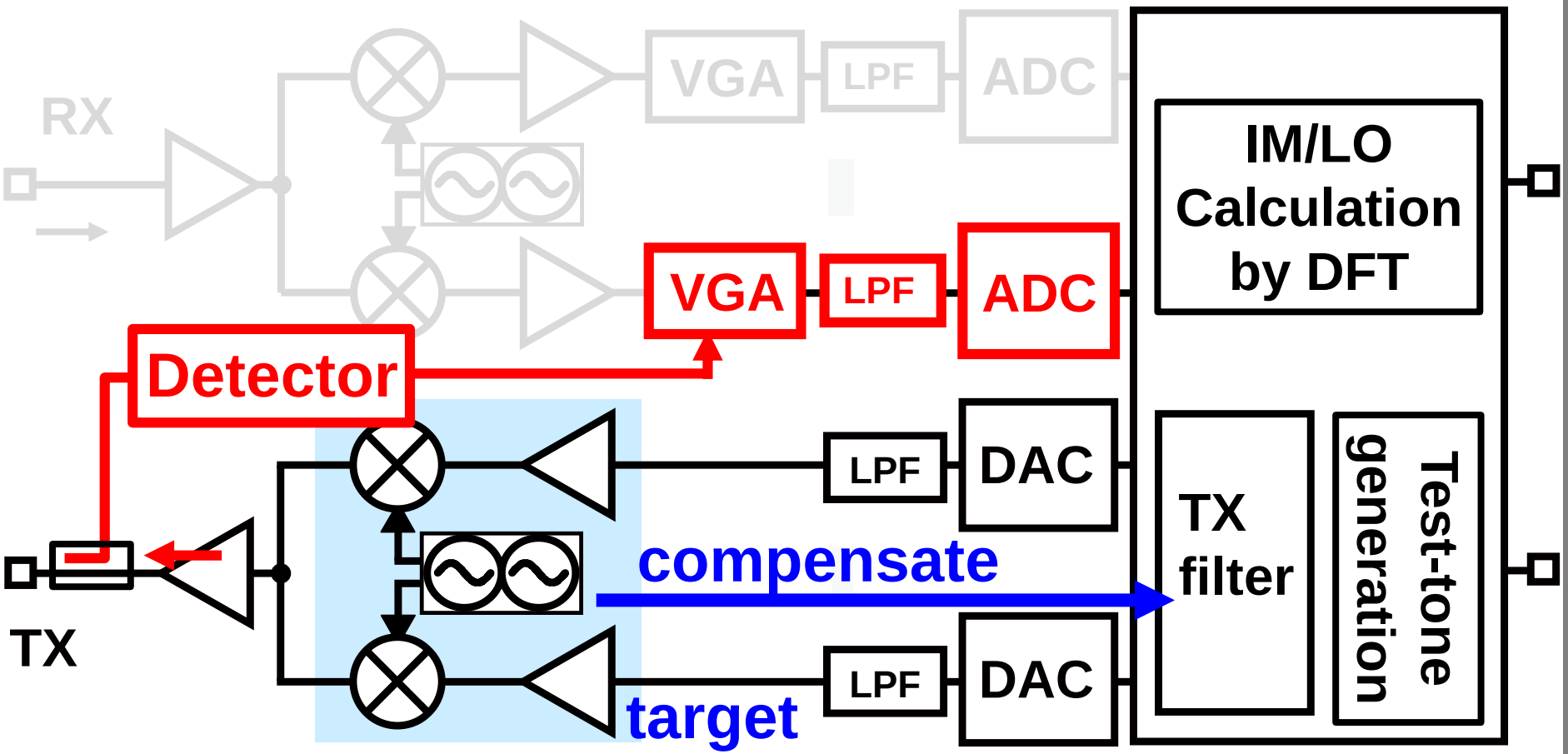
TX Filter Calibration (BB loopback)



LPF gain/cut-off mismatch between I/Q paths are calibrated.

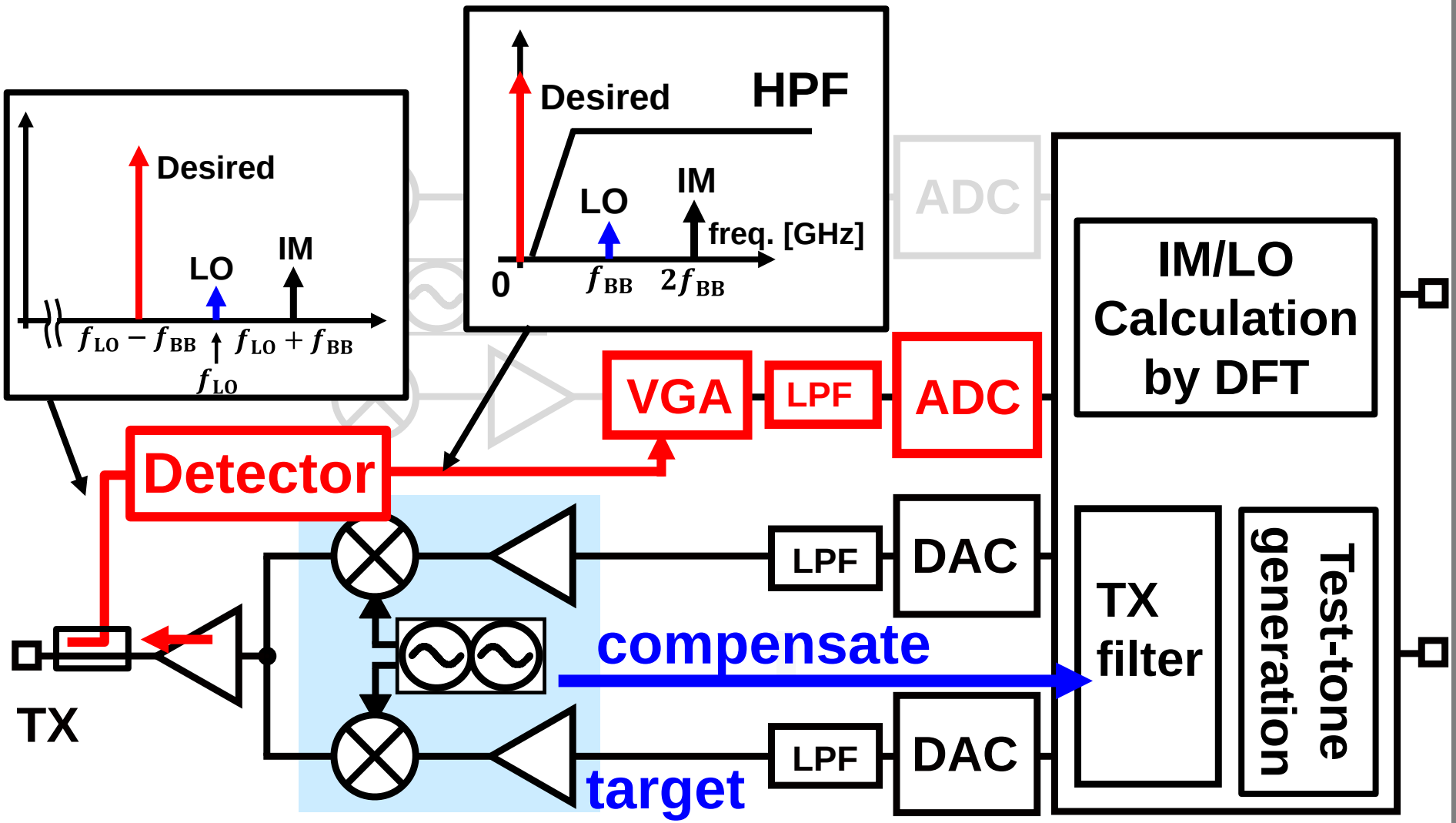
RF Loop-Back Calibration for TX

ADC is re-used for IM/LO calculation with DFT in BB.



*Iason Vassiliou, *et al.*, IEEE JSSC 2003.

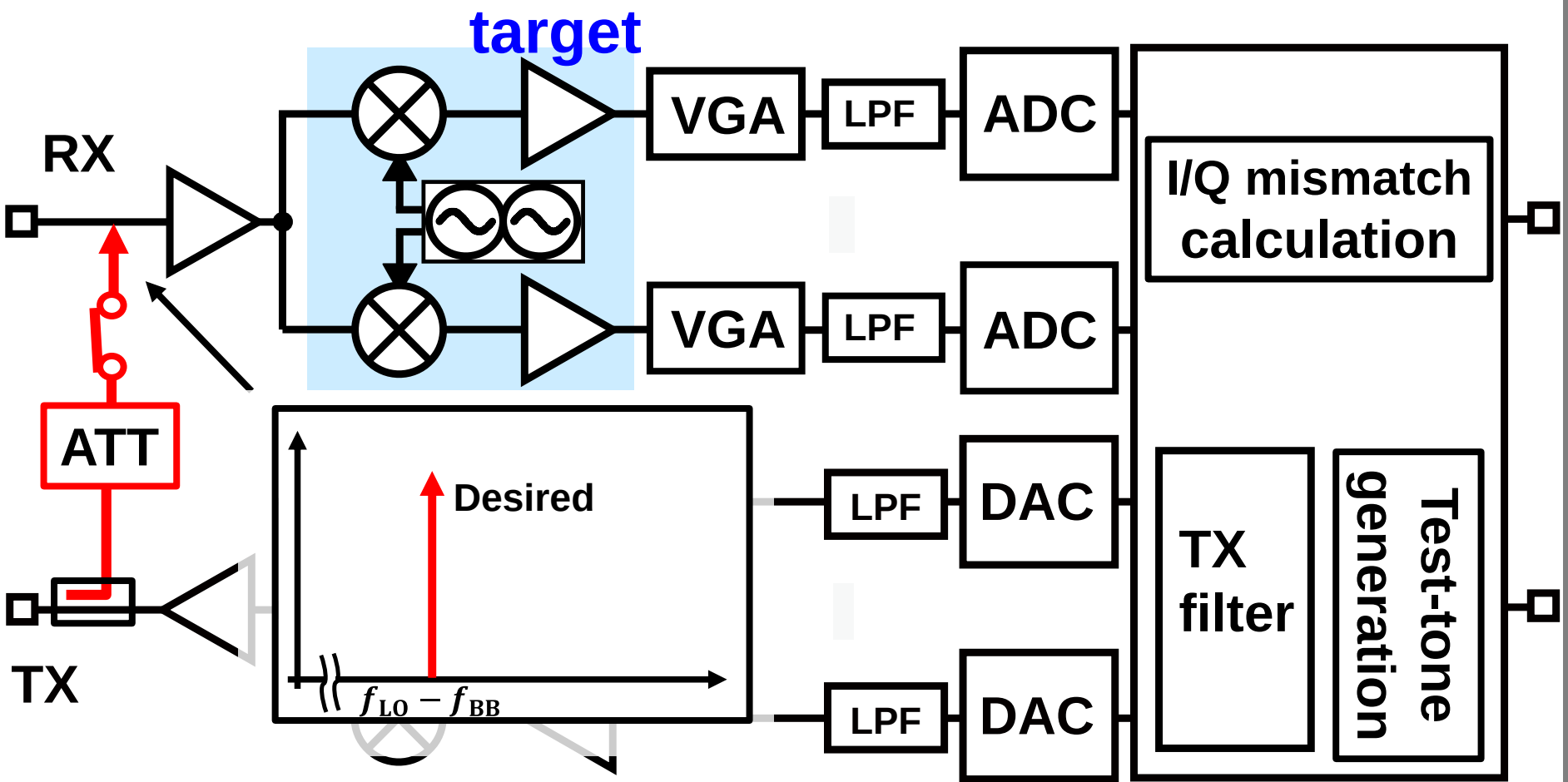
RF Loop-Back Calibration for TX



*Iason Vassiliou, *et al.*, IEEE JSSC 2003.

RF Loop-Back Calibration for RX

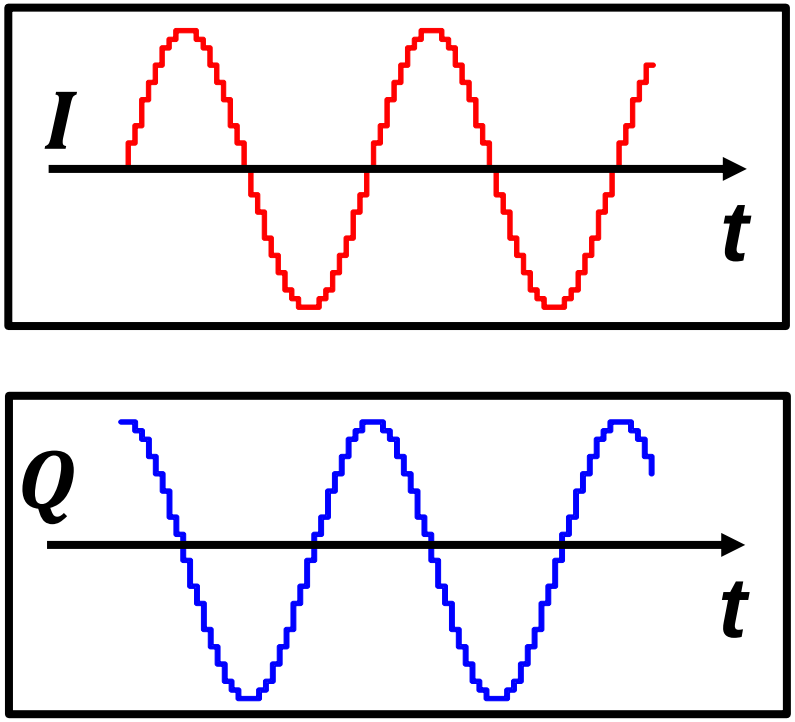
TX is used for a test-tone generator.



*Iason Vassiliou, *et al.*, IEEE JSSC 2003.

I/Q Gain/Phase Mismatch Calculation

At least, a 10-bit ADC is required for a IMRR of 40dB.



$$\mathbf{LPF}\left(I^2 + Q^2\right)$$

RSSI ➔ AGC

$$\mathbf{LPF}\left(I^2 - Q^2\right) \cong \Delta g$$

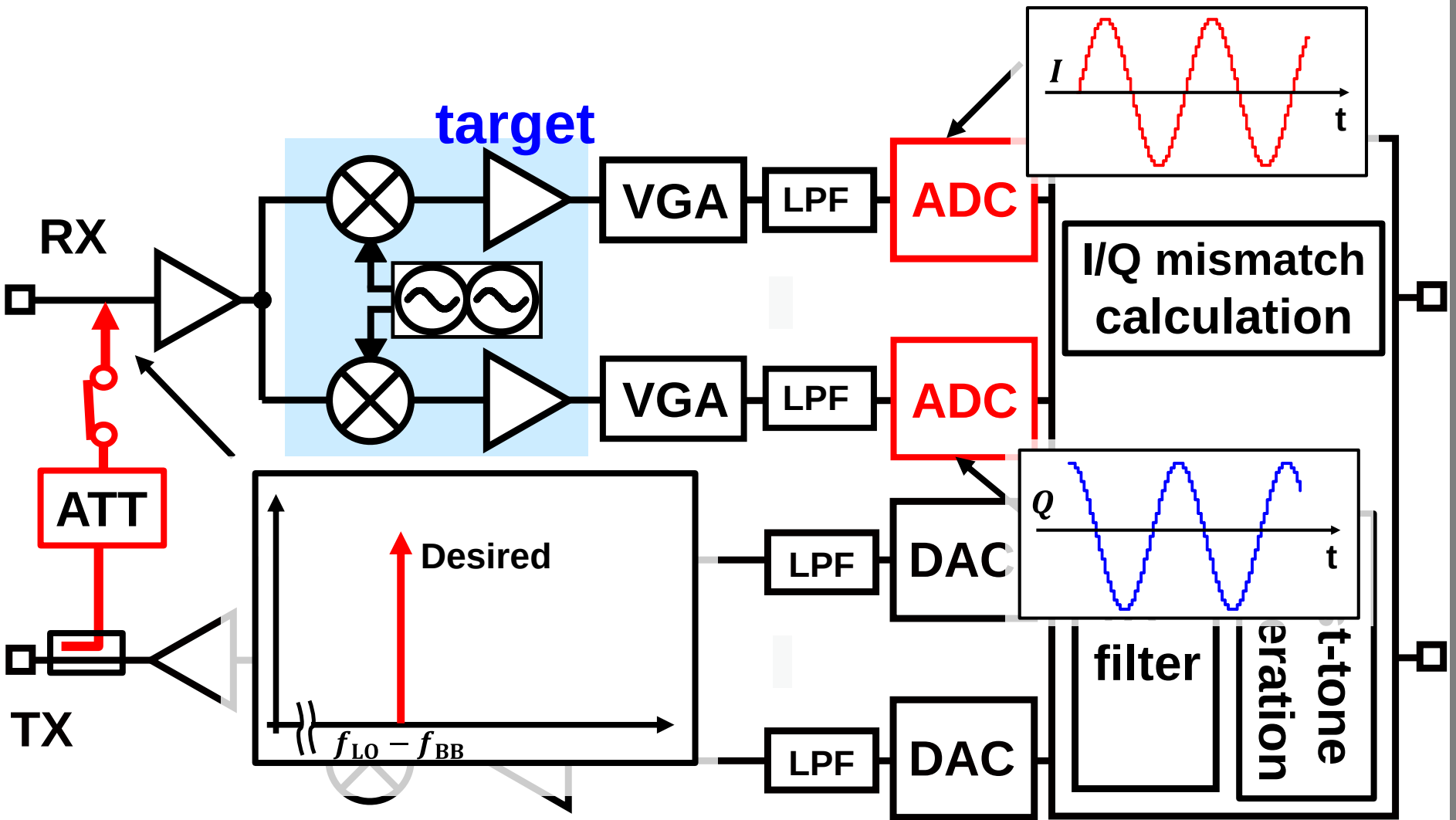
$$\mathbf{LPF}(I * Q) \cong -\Delta\theta/2$$

Modulated signal can be used.

➔ Background calibration

*S. Lerstaveesin, *et al*., IEEE JSSC 2006.

RF Loop-Back Calibration for RX



*Iason Vassiliou, *et al.*, IEEE JSSC 2003.

Calibration *vs* Compensation

Frequency independent (RF)

TX I/Q mismatch(RF) ➔ Digital compensation (BB TX filter)

RX I/Q mismatch(RF) ➔ Digital compensation (BB RX filter)

FDE/OFDM

Frequency independent (BB)

TX I/Q mismatch(BB) ➔ Digital compensation

RX I/Q mismatch(BB) ➔ Digitally-calibrated analog (AGC)

/ Digital compensation

Frequency dependent (BB)

TX I/Q mismatch(BB) ➔ Digitally-calibrated analog

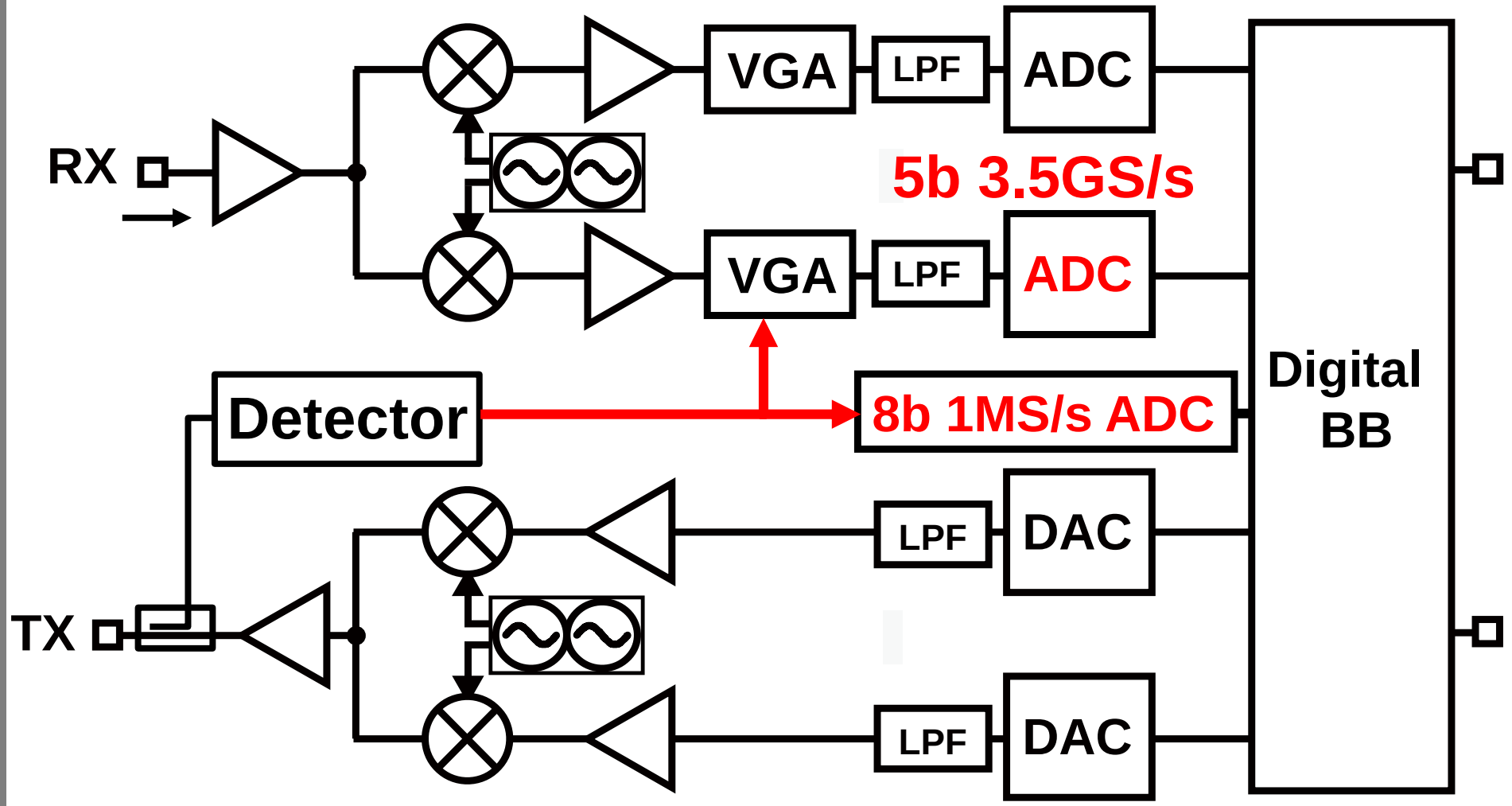
RX I/Q mismatch(BB) ➔ Digitally-calibrated analog

/ Digital compensation

as a typical case

60GHz Transceiver Calibration

One additional ADC is used for a fine resolution.



*T. Tsukizawa, *et al*., ISSCC 2013

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  - Synthesizable Analog

Calibration in Frequency Synthesizer

- AFC for capacitor-bank in LC-VCO
- ILFD/ILO Calibration
- Linearity calibration/compensation
  - Loop-BW, Quantization noise, FM/Polar-TX

VCO: frequency ← voltage (varactor, C-bank)

DCO: frequency ← code (C-bank, I-control)

TDC: code ← delay (PVT, noise, layout, etc)

(ADC: code ← voltage)

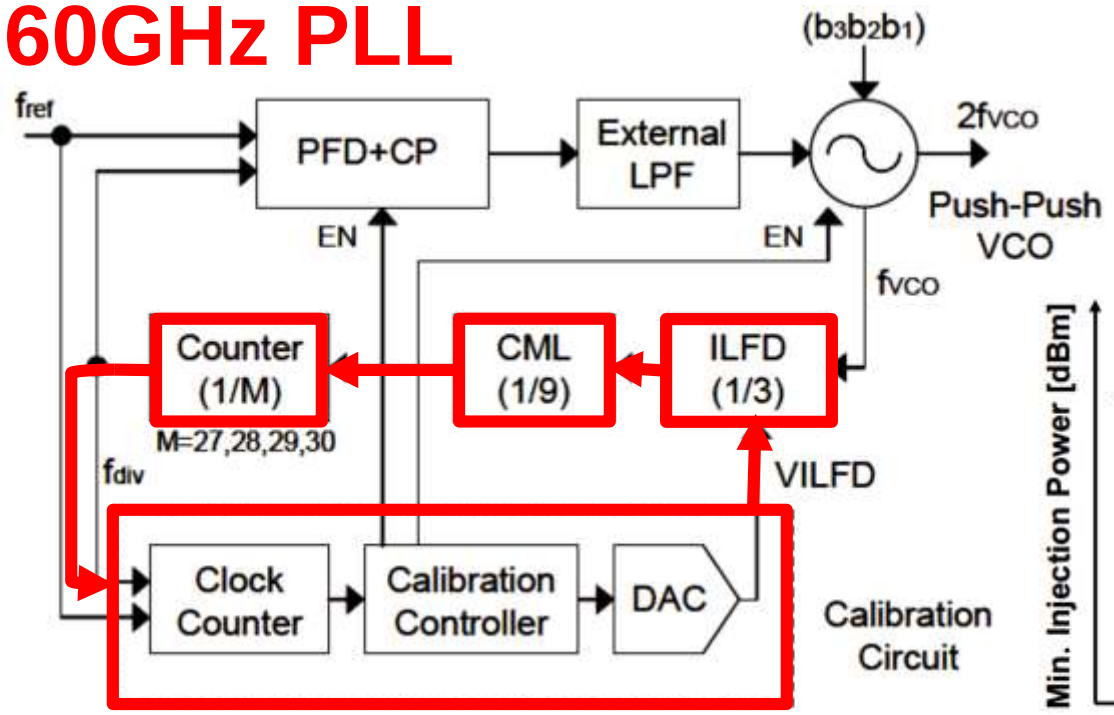
(DAC: voltage ← code)

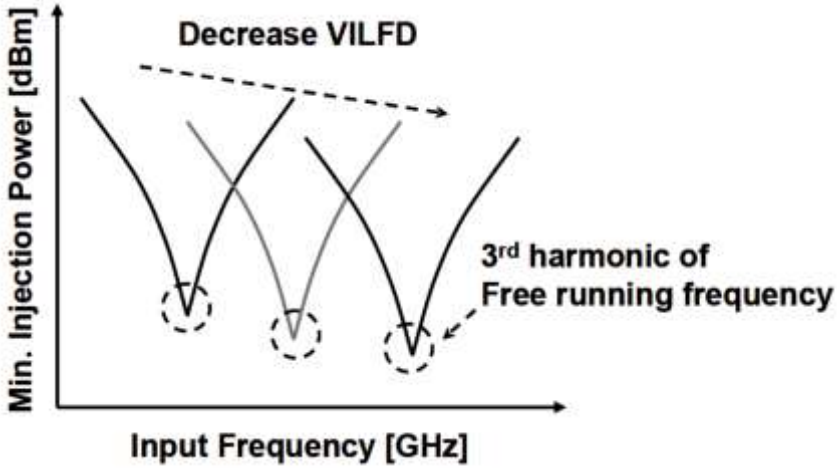
(Amp: voltage ← voltage)

AFC: Automatic Frequency Calibration
ILFD: Injection-Locked Frequency Divider
ILO: Injection-Locked Oscillator (Multiplier)

ILFD Calibration

Locked*/Free-run** frequency is used.





*S. Pellerano, *et al*., ISSCC 2008 **T. Shima, *et al*., APMC 2011
***W. Deng, *et al*., A-SSCC 2012

Summary of Transceiver Calibration

- **Wireless transceiver is a big system.**
- **Historically, architecture-level digitization has been applied with system-level calibration and compensation for PVT and environmental variations.**
- **Re-use of counter-part block for calibration**

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Issues of Analog Circuit Design

Why is the simulated performance degraded?

Imperfection caused by physical implementation

PVT

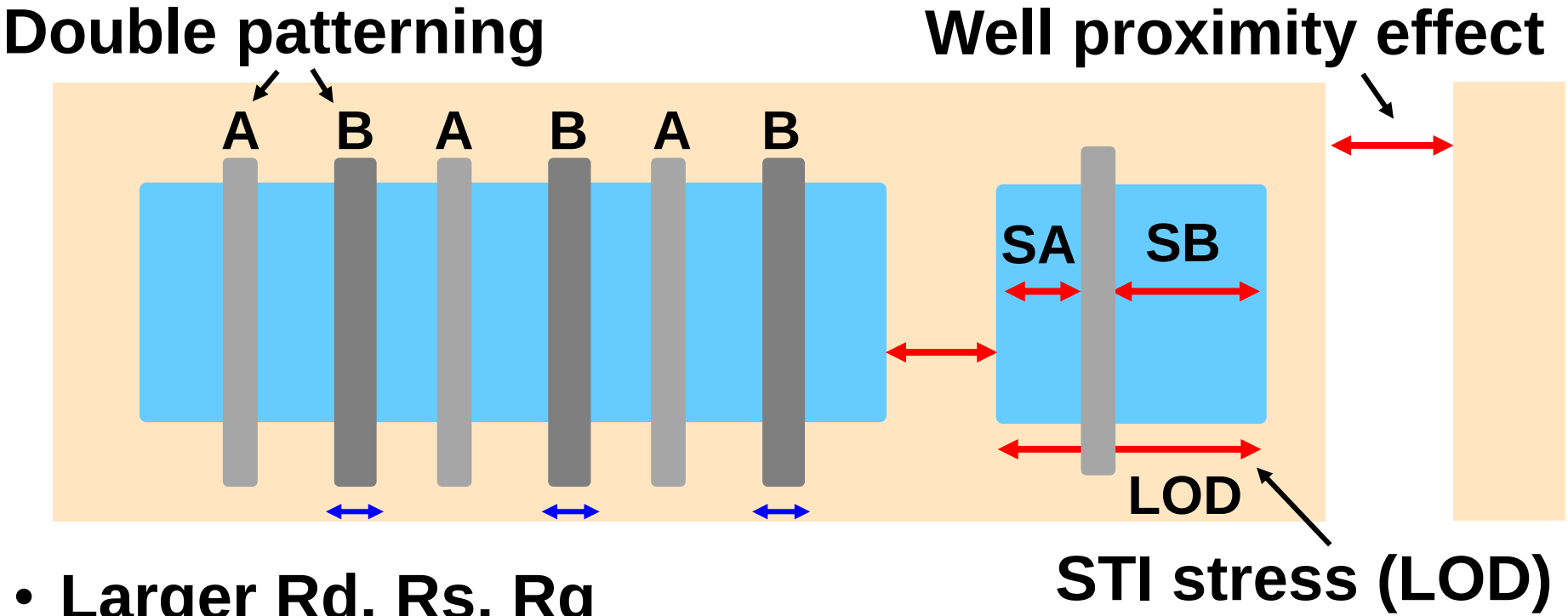
layout non-ideality

- **mismatch**
- **isolation/coupling**

} **Compensated by digital assistance**

Layout Design Issues beyond 20nm

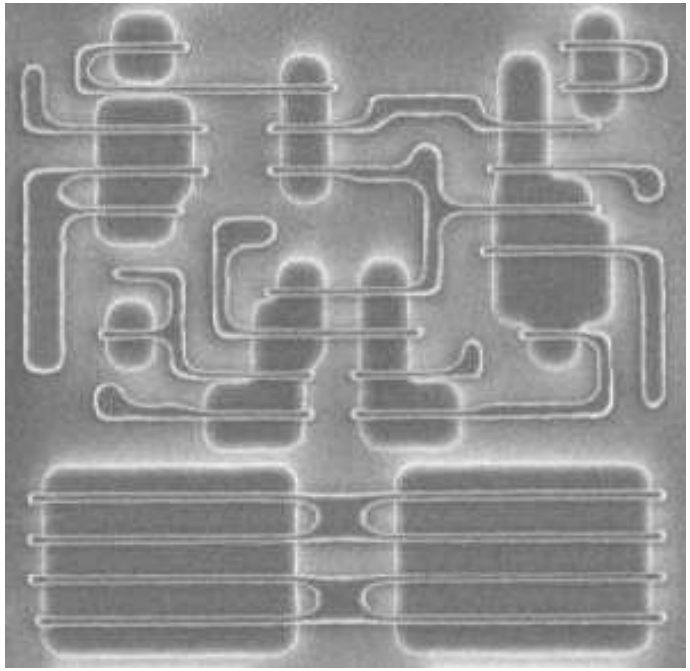
Transistor matching cannot be expected any more.



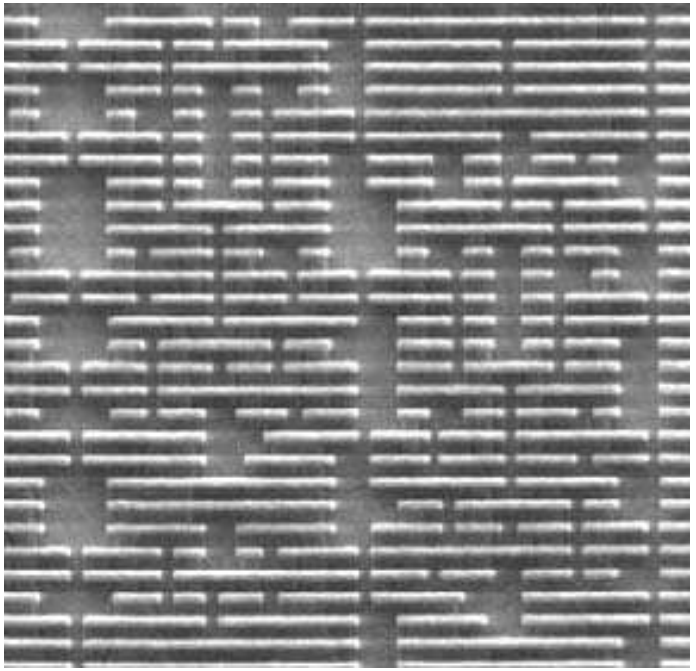
- Larger Rd, Rs, Rg
- Fixed fin height (for FinFET)
- Self-heating
- No body effect

Scaled CMOS Layout

65nm layout style



32nm layout style



- Uni-directional features
- Uniform gate dimension
- Gridded layout

*M. Bohr, ISSCC 2009

Massive Digital Assistance

PVT

layout non-ideality

- mismatch
- isolation/coupling

} Compensated by digital assistance

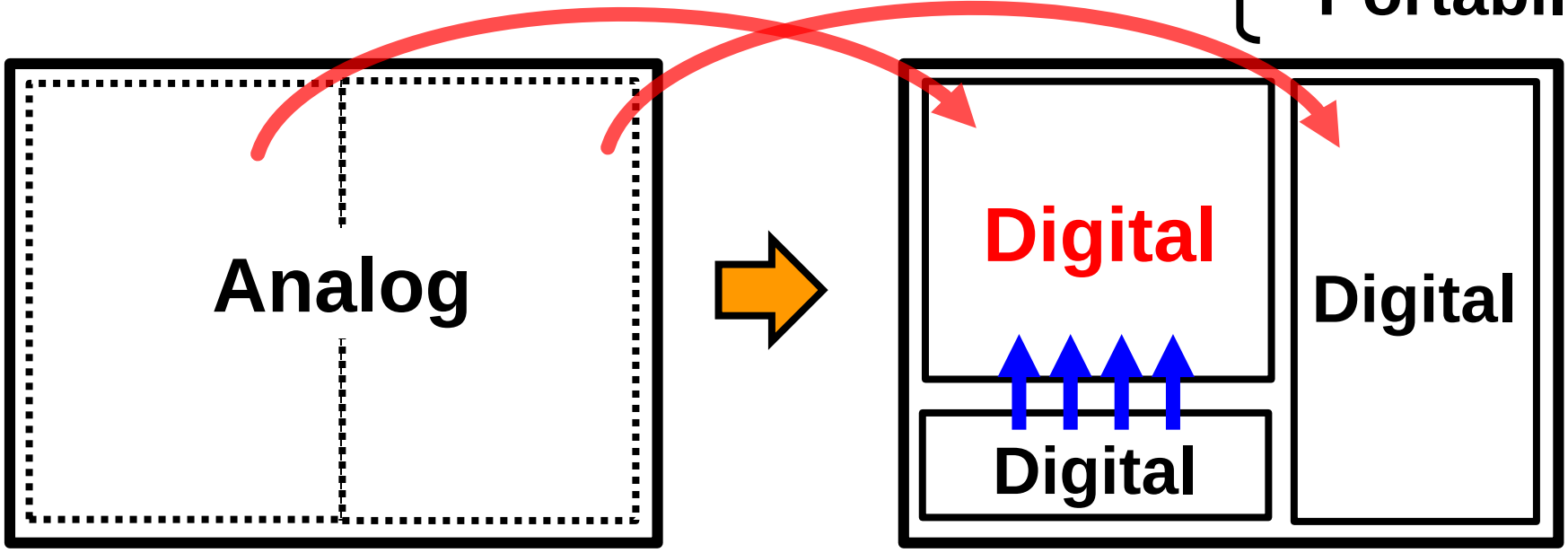
Delay and linearity in delay can be calibrated easily in time-domain analog circuits,

e.g. AD-PLL.

Further Analog Circuit

Digitization

- Scalability
- Portability



Massive Digital Assistance

- Robustness
- Less redundancy

Outline

- Analog to Digital
  - Digitization of Wireless TRX
- Digital Assistance
  - Wireless Transceiver
  - Frequency Synthesizer
- Future Analog Design
  - Synthesizable Analog

Synthesizable Analog Circuits

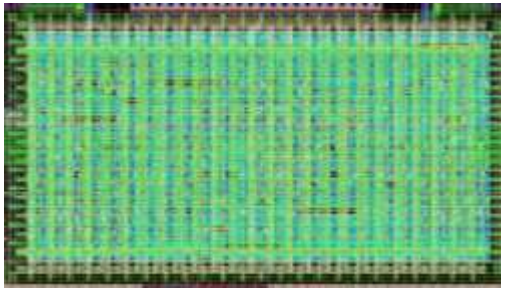
HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

Commercial P&R tools…

GDS

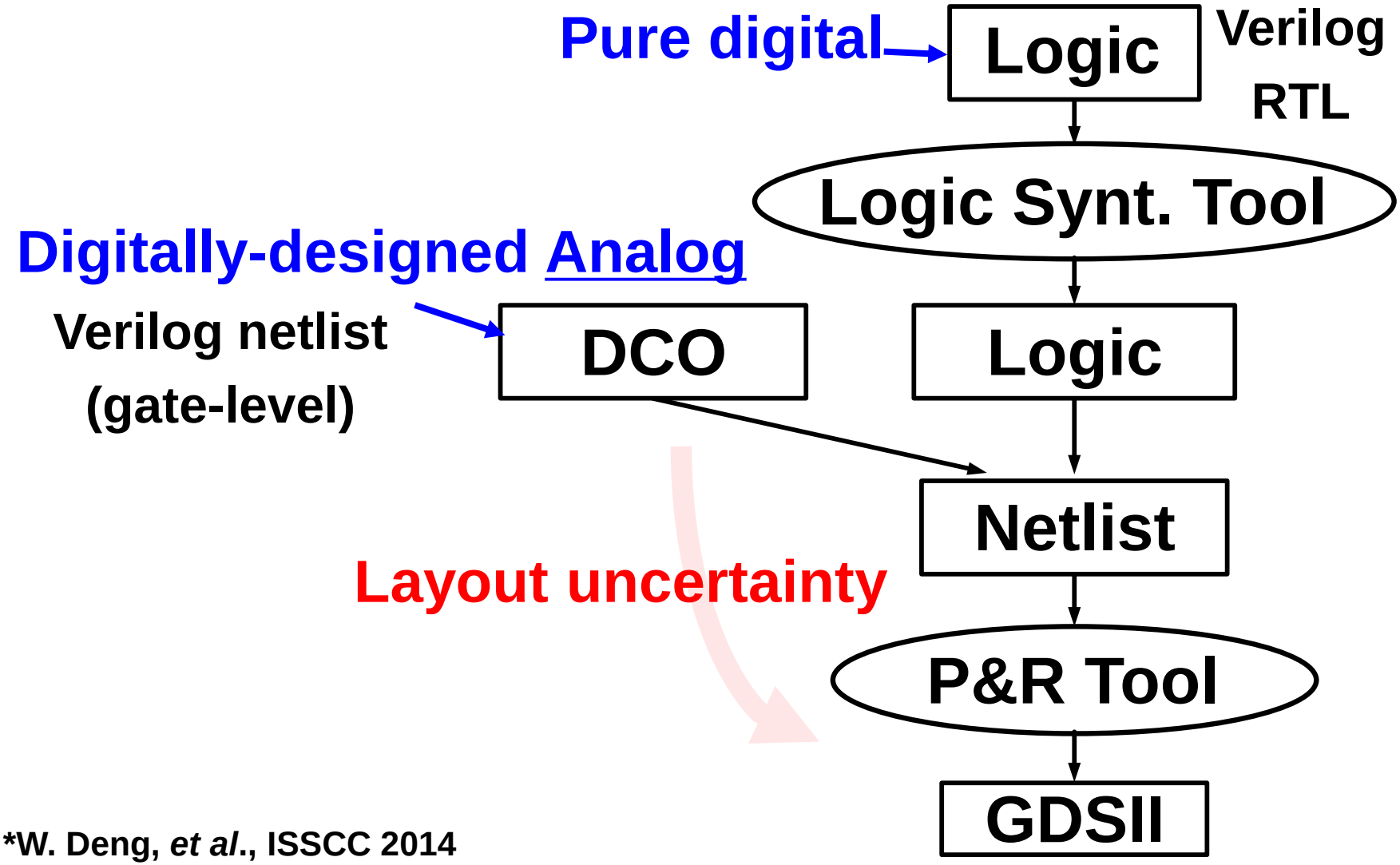


with a standard-cell library

without any custom-designed cells

without manual placement

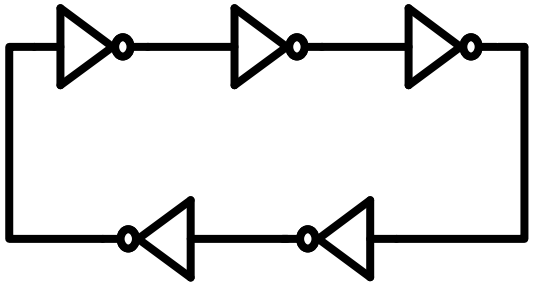
Analog Synthesis by Digital Tools



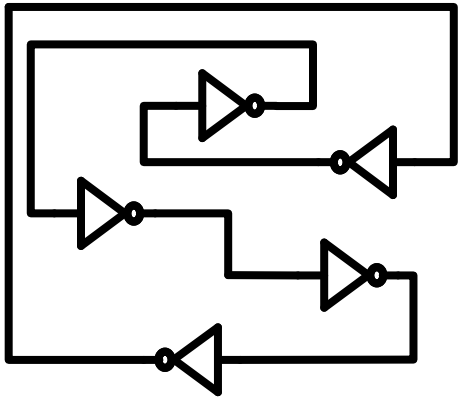
*W. Deng, *et al*., ISSCC 2014

Issue: Layout Uncertainty

Massive digital assistance can overcome the layout uncertainty issue.



Ideal placement



Actual placement

➔Unbalanced loading

No layout symmetry

e.g., DCO &TDC linearity

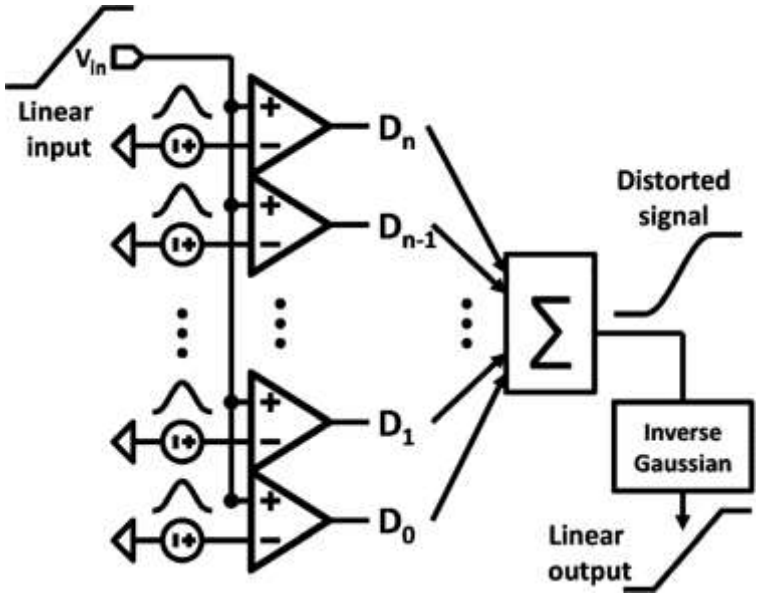
Synthesizable Analog Circuits

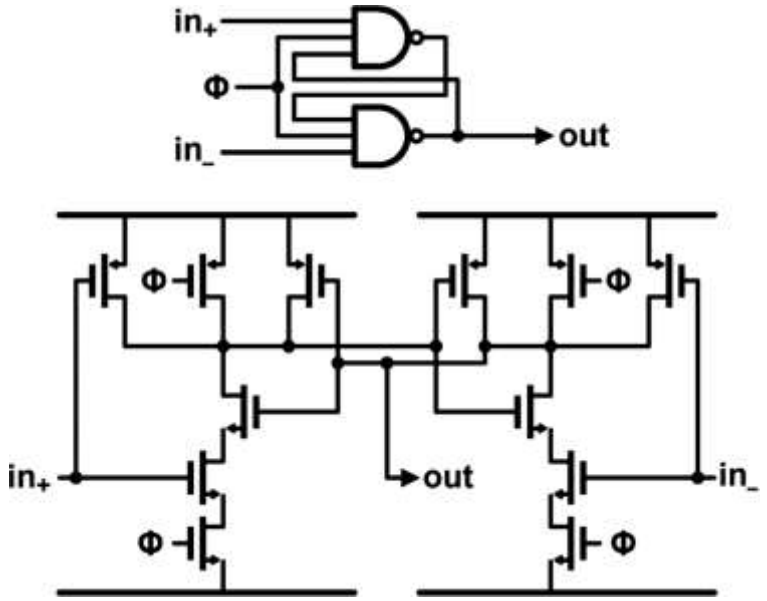
only by standard cells

- **Synthesizable PLL***
- **Synthesizable DCO**
- **Synthesizable DAC**
- **Synthesizable TDC**
- **Synthesizable ADC****

***W. Deng, *et al*., ISSCC 2014 **S. Weaver, *et al*., IEEE TCAS-I 204**

Synthesizable ADC





ADC architecture

SNDR of 35.9dB, 210MS/s

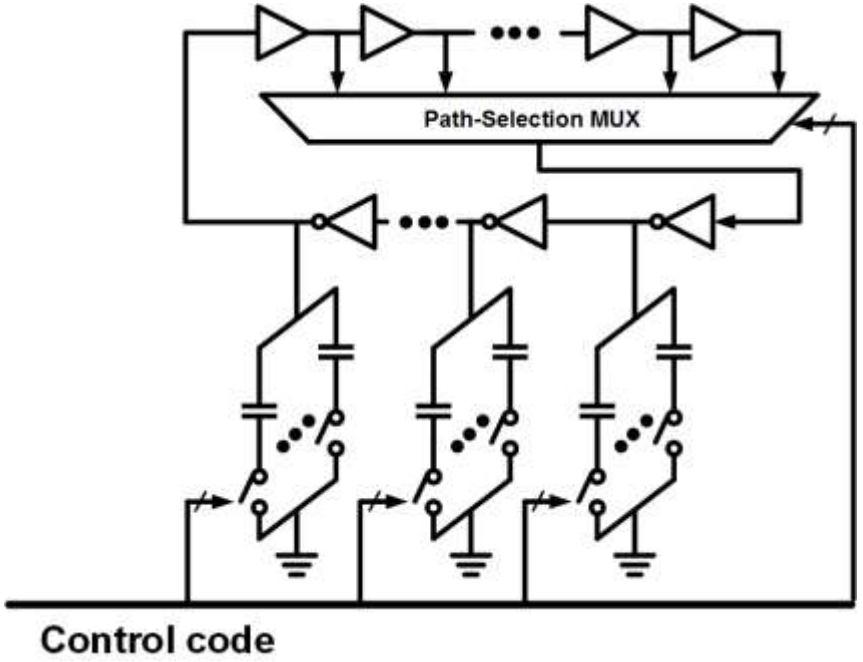
Comparator by NAND3

Gaussian offset distribution

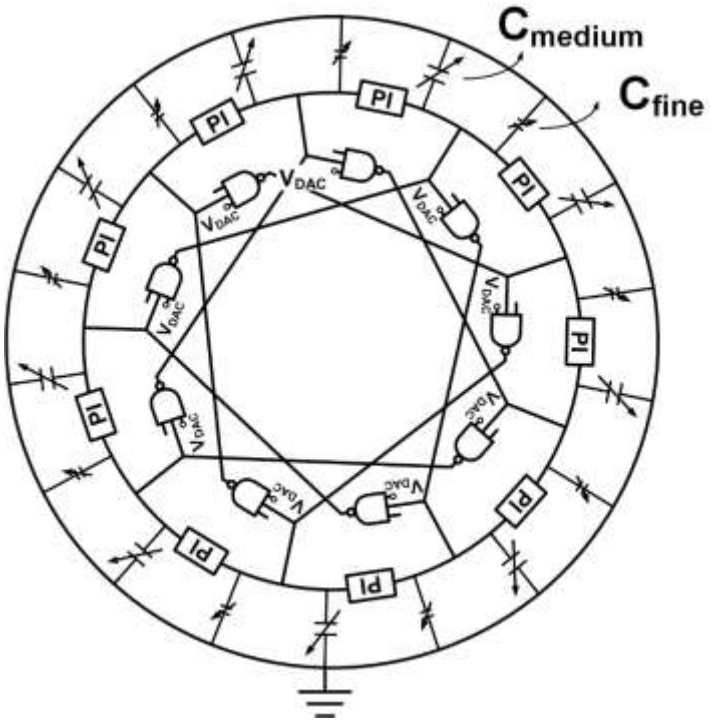
Linearity compensation by inverse Gaussian

***S. Weaver, *et al*., IEEE TCAS-I 2014**

Synthesizable DCO



MUX and varactor*



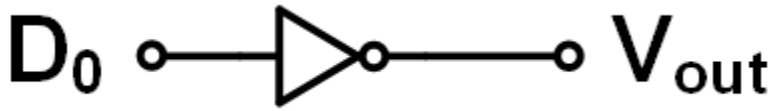
Phase-Interpolator**, I-DAC***, and fine varactor***

*D. Sheng, *et al*., IEEE TCAS-II 2007

**A. Matsumoto, *et al*., JSSC 2008 ***W. Deng, *et al*., ISSCC 2014

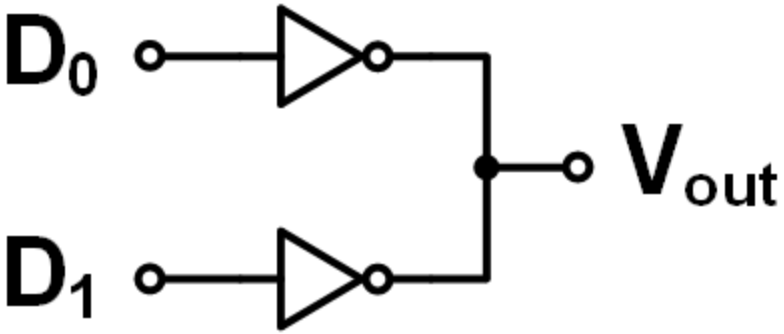
Synthesizable DAC

Only standard cell



$D_0 = 0$ $V_{out} = 1V$

$D_0 = 1$ $V_{out} = 0V$



$D_0D_1 = 11$ $V_{out} = 0V$

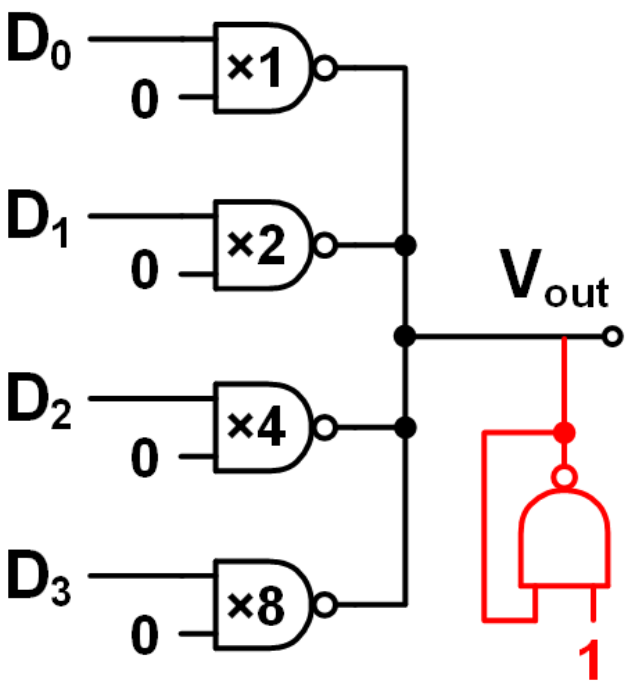
$D_0D_1 = 10$ $V_{out} = 0.5V$

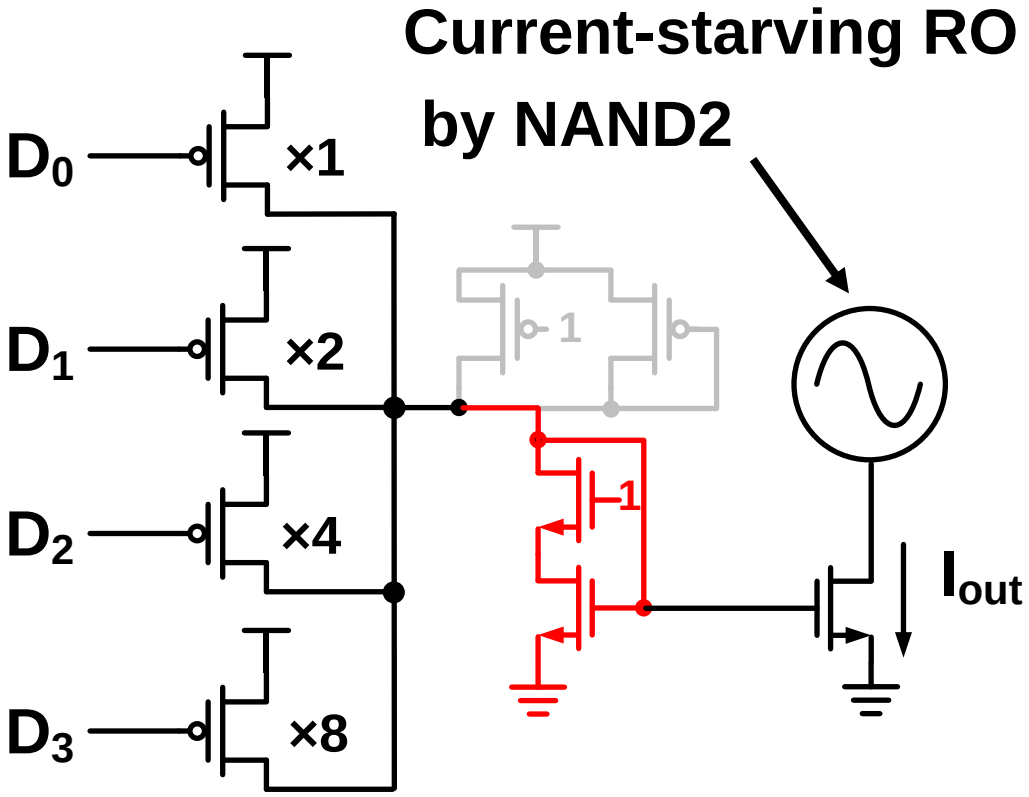
$D_0D_1 = 01$ $V_{out} = 0.5V$

$D_0D_1 = 00$ $V_{out} = 1V$

Synthesizable I-linear DAC

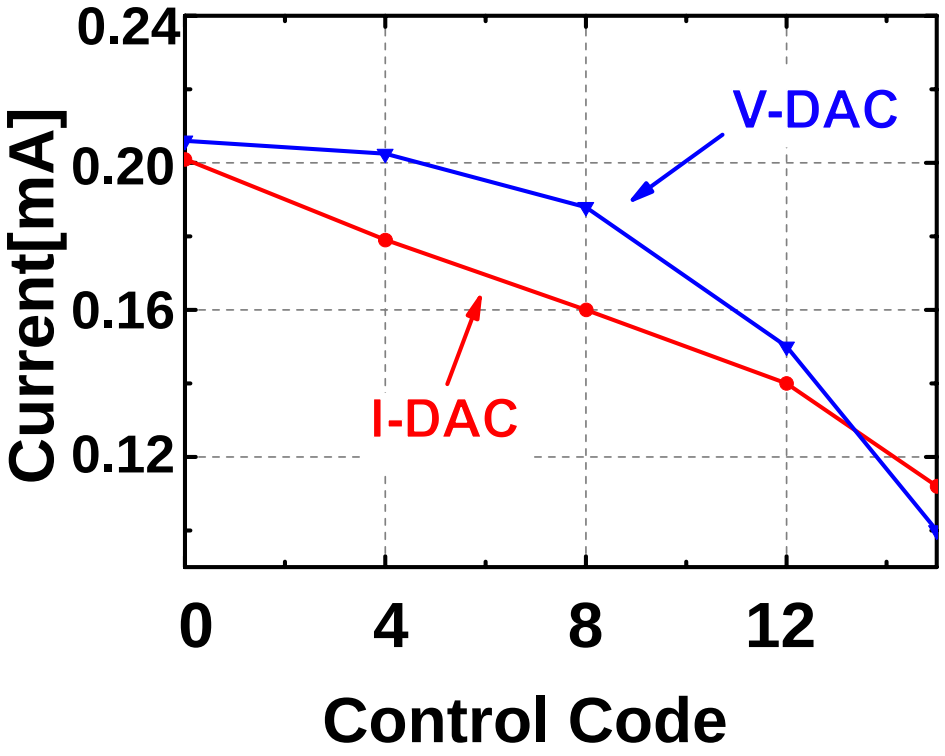
Only standard cell



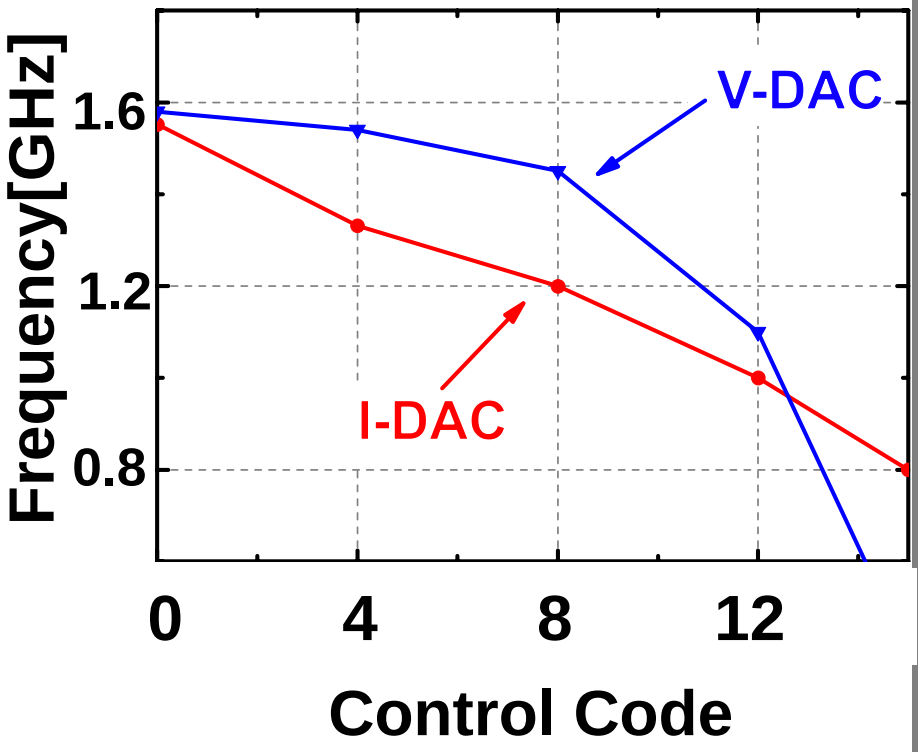


*W. Deng, *et al*., ISSCC 2014

V-linear DAC vs I-linear DAC

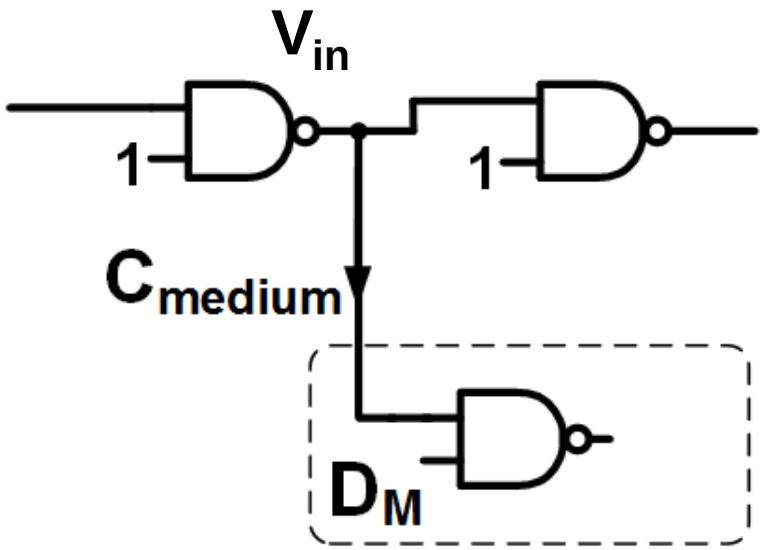


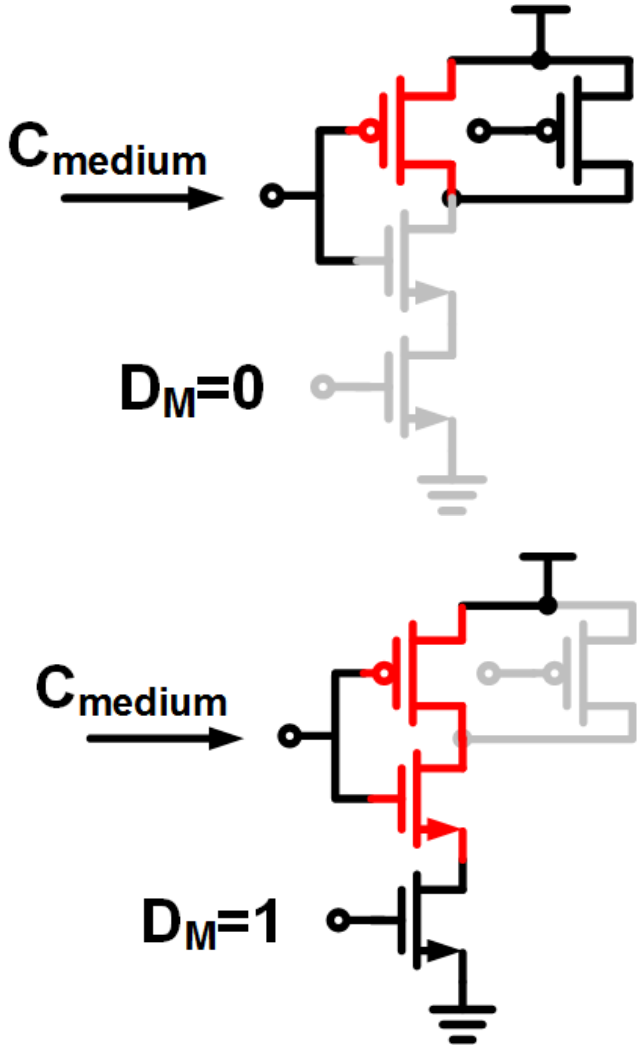
Current-starving RO
by NAND2



Stdcell Varactor

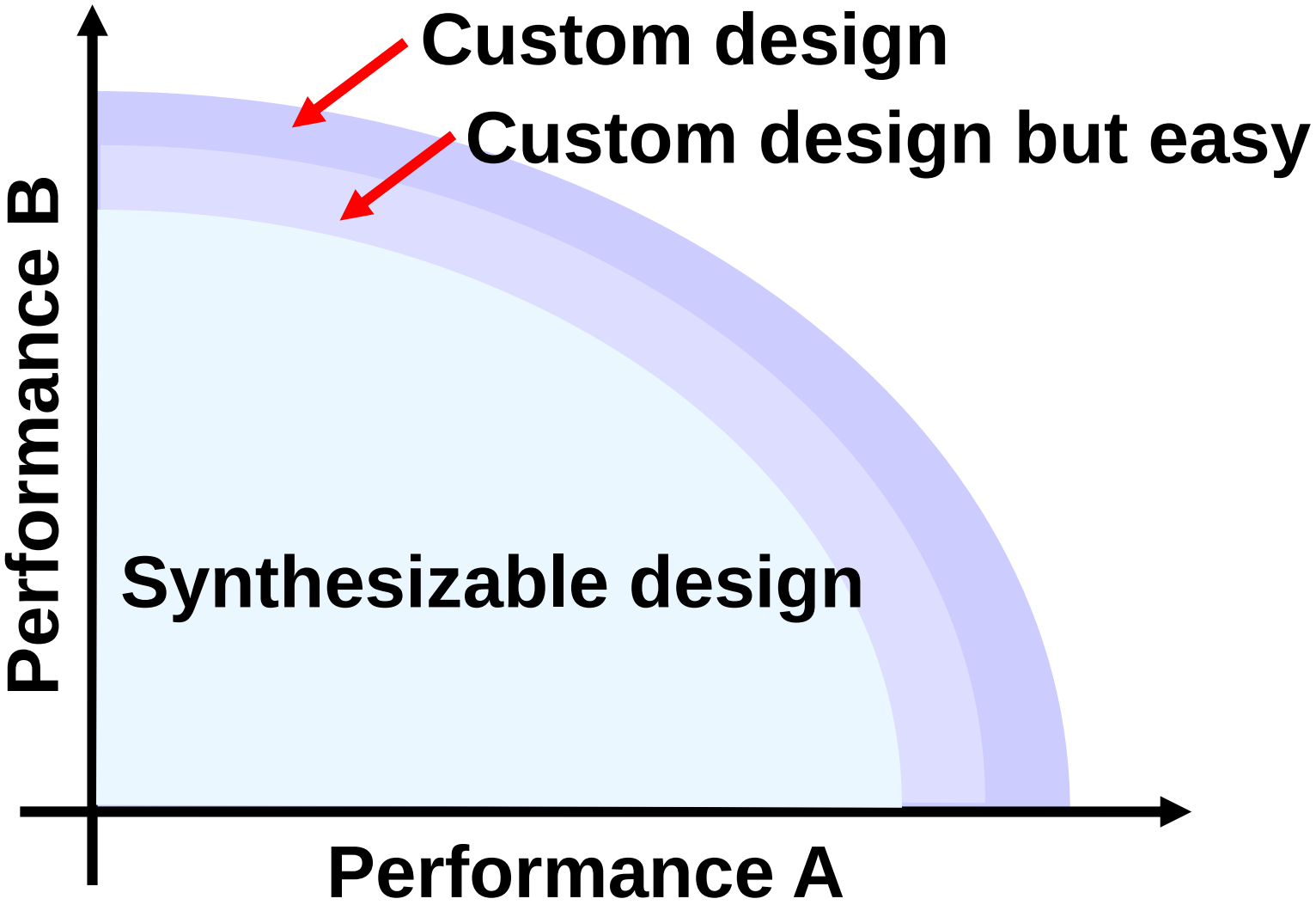
1.55ps@200MHz



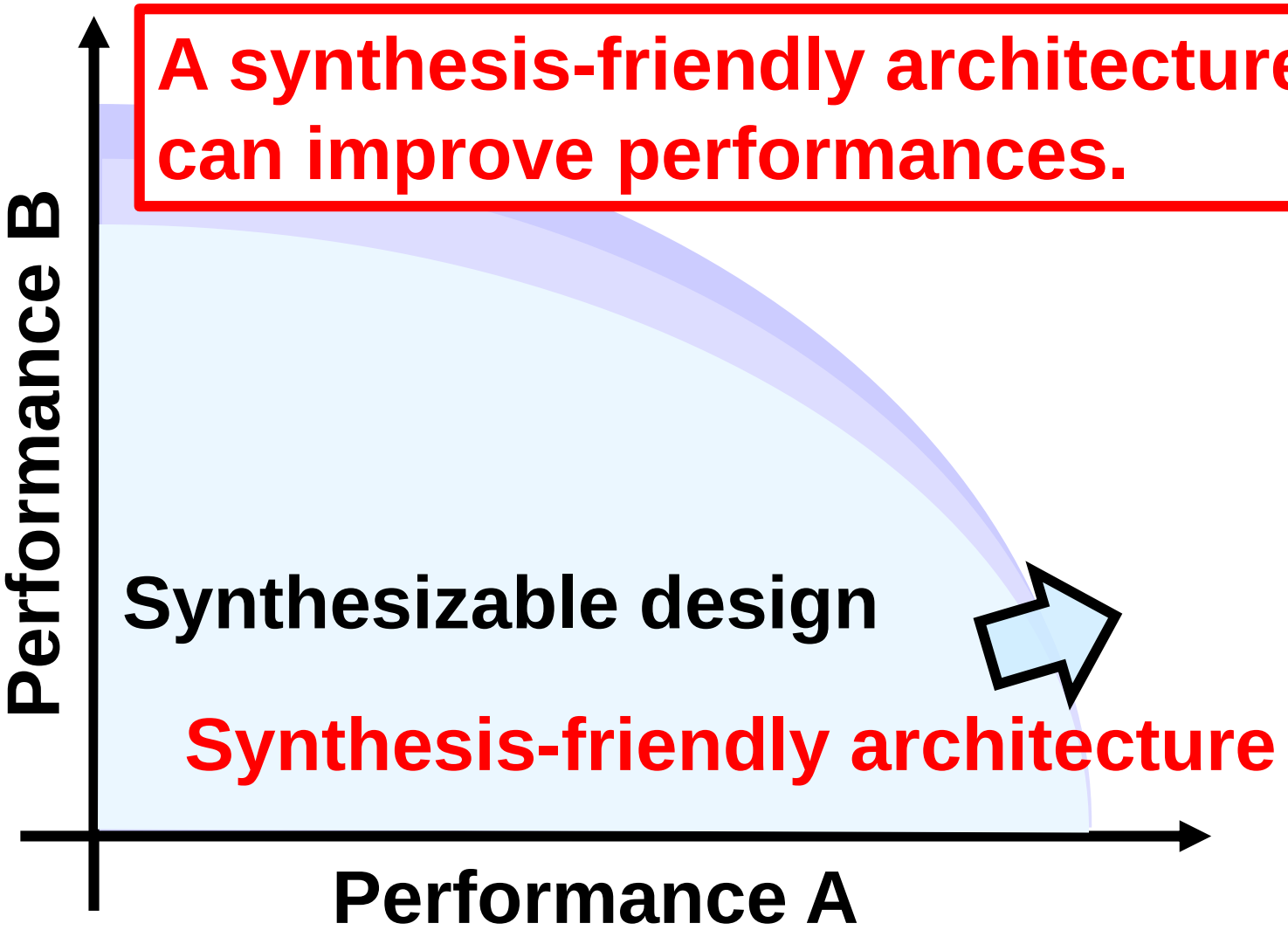


*P. L. Chen, *et al.*, TCAS II 2005

Performance Trade-off



Performance Trade-off



Injection-Locked PLL (IL-PLL)

Conventional CP-PLL and TDC-PLL (AD-PLL)

- **Phase lock: feedback**
- **Frequency lock: feedback**

Injection-Locked PLL (IL-PLL)

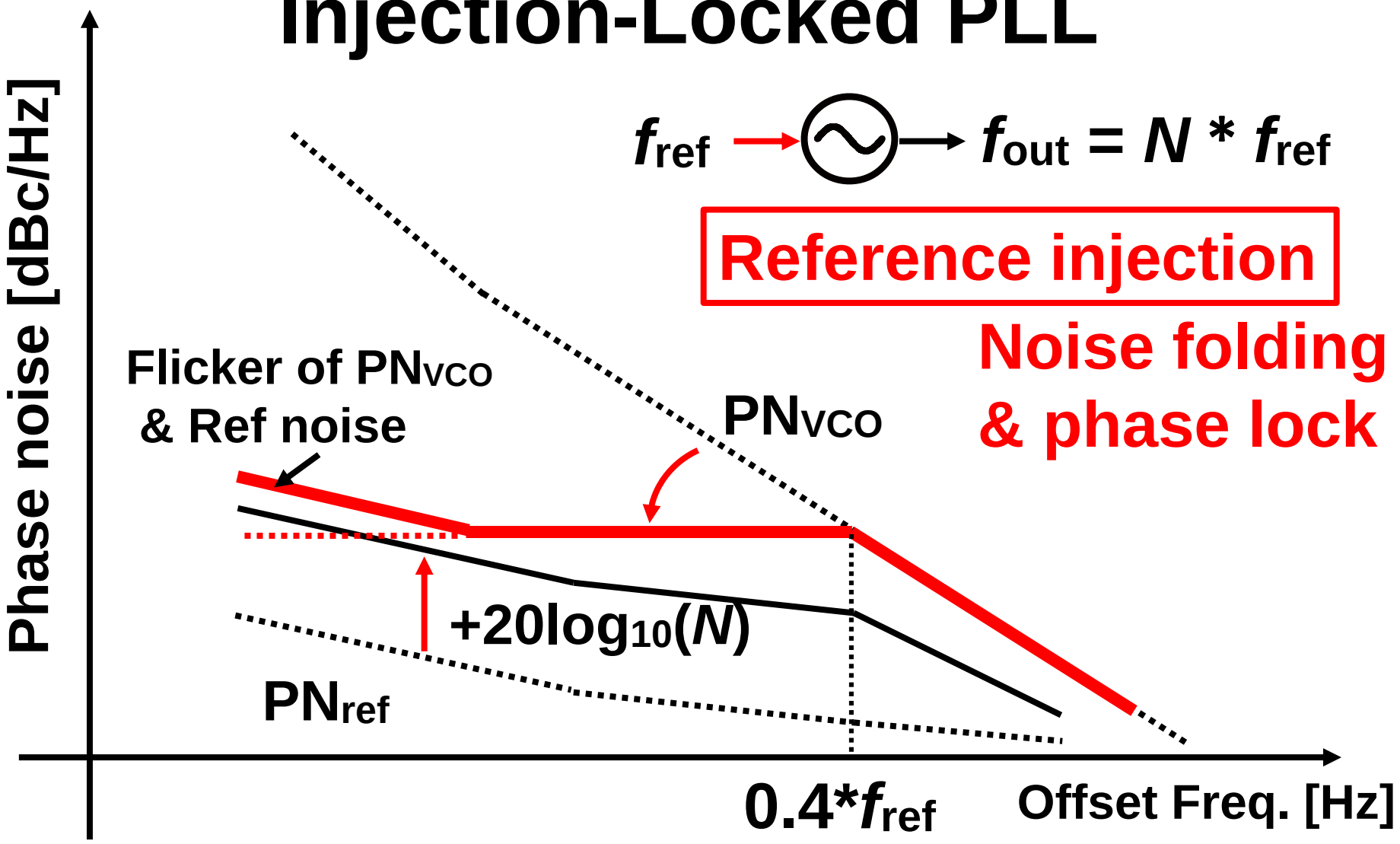
- **Phase lock: feed-forward ⟵ Injection-lock**
- **Frequency lock: feedback ⟵ Counter**

The fine timing feedback is not required.

➔ Synthesis-friendly

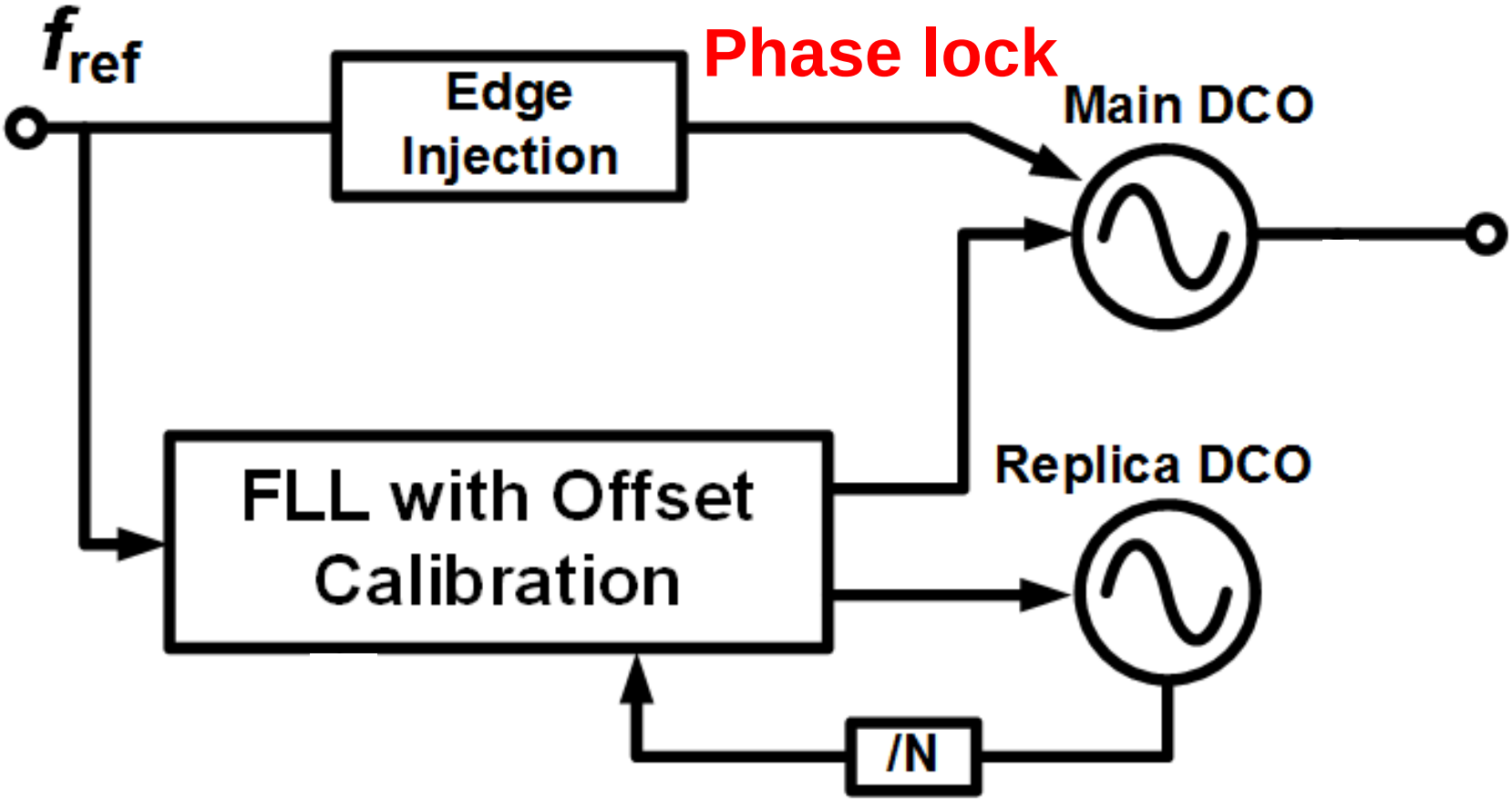
***W. Deng, *et al*., ISSCC 2014**

Injection-Locked PLL



*S. Ye, *et al*., IEEE JSSC 2002 **N. D. Dalt, IEEE TCAS-II 2014

Synthesizable IL-PLL

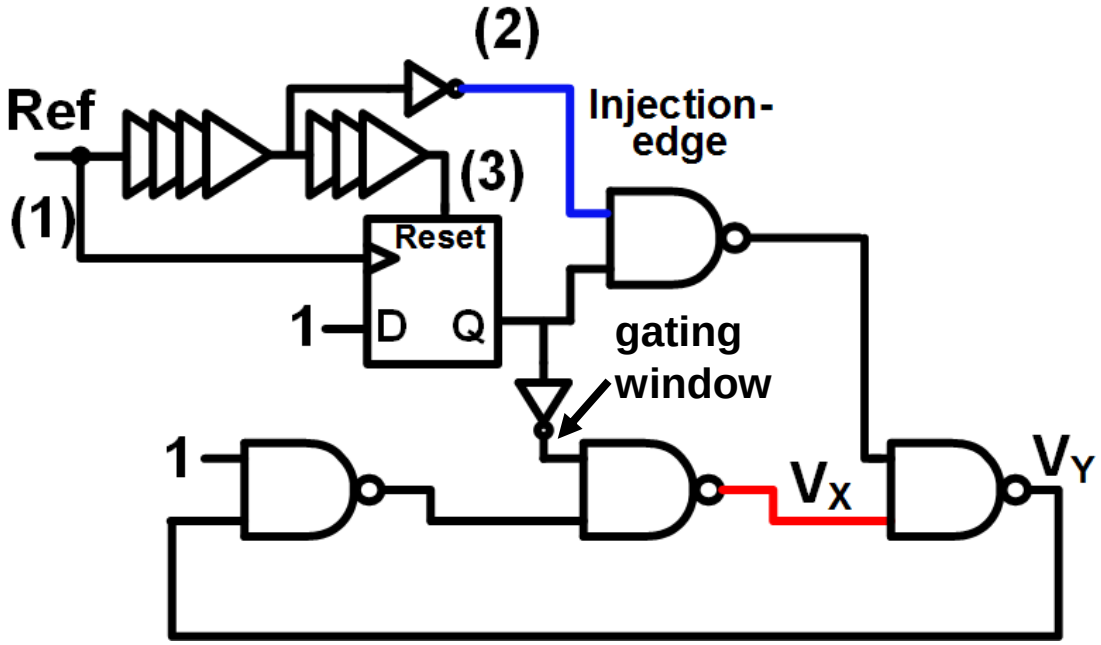


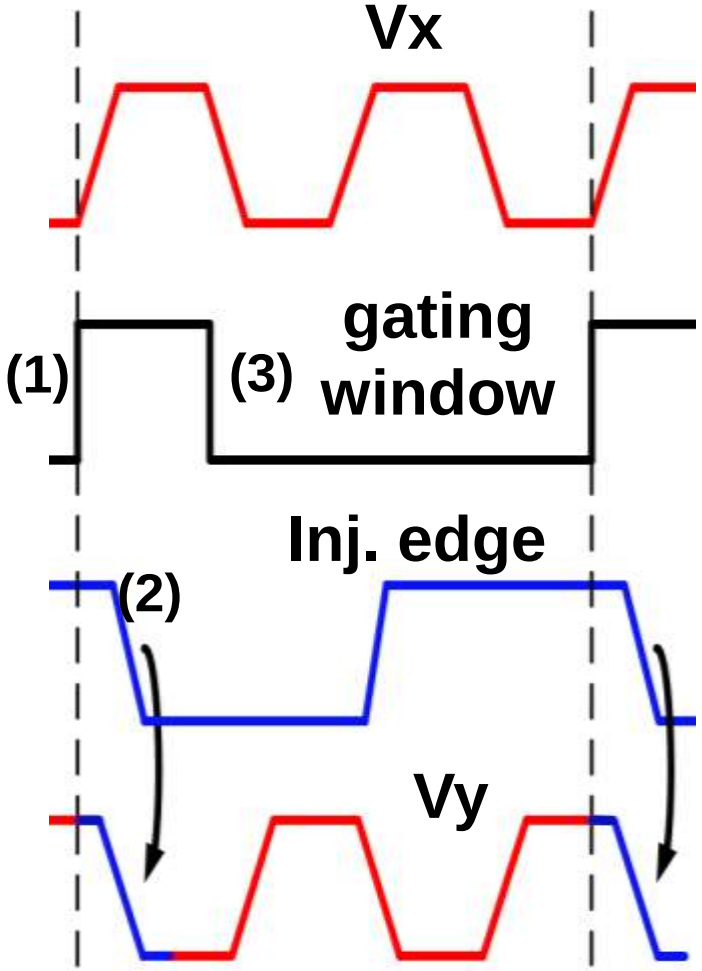
Frequency tracking with very narrow BW

*W. Deng, *et al*., ISSCC 2013 **A. Musa, *et al*., JSSC 2014 ***W. Deng, *et al*., ISSCC 2014

Gated Edge Injection

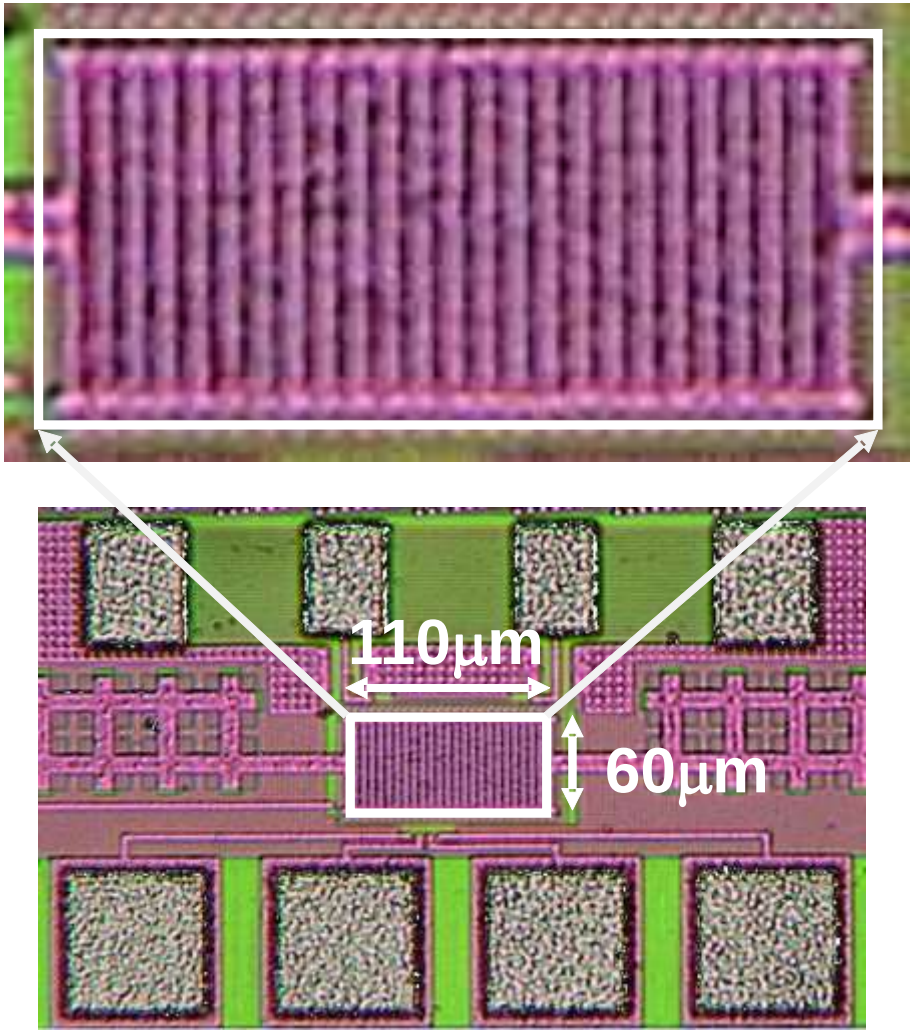
Severe timing design is NOT required.





*W. Deng, *et al*., ISSCC 2014 **D. Park, *et al*., ISSCC 2012

Layout



CMOS 65nm

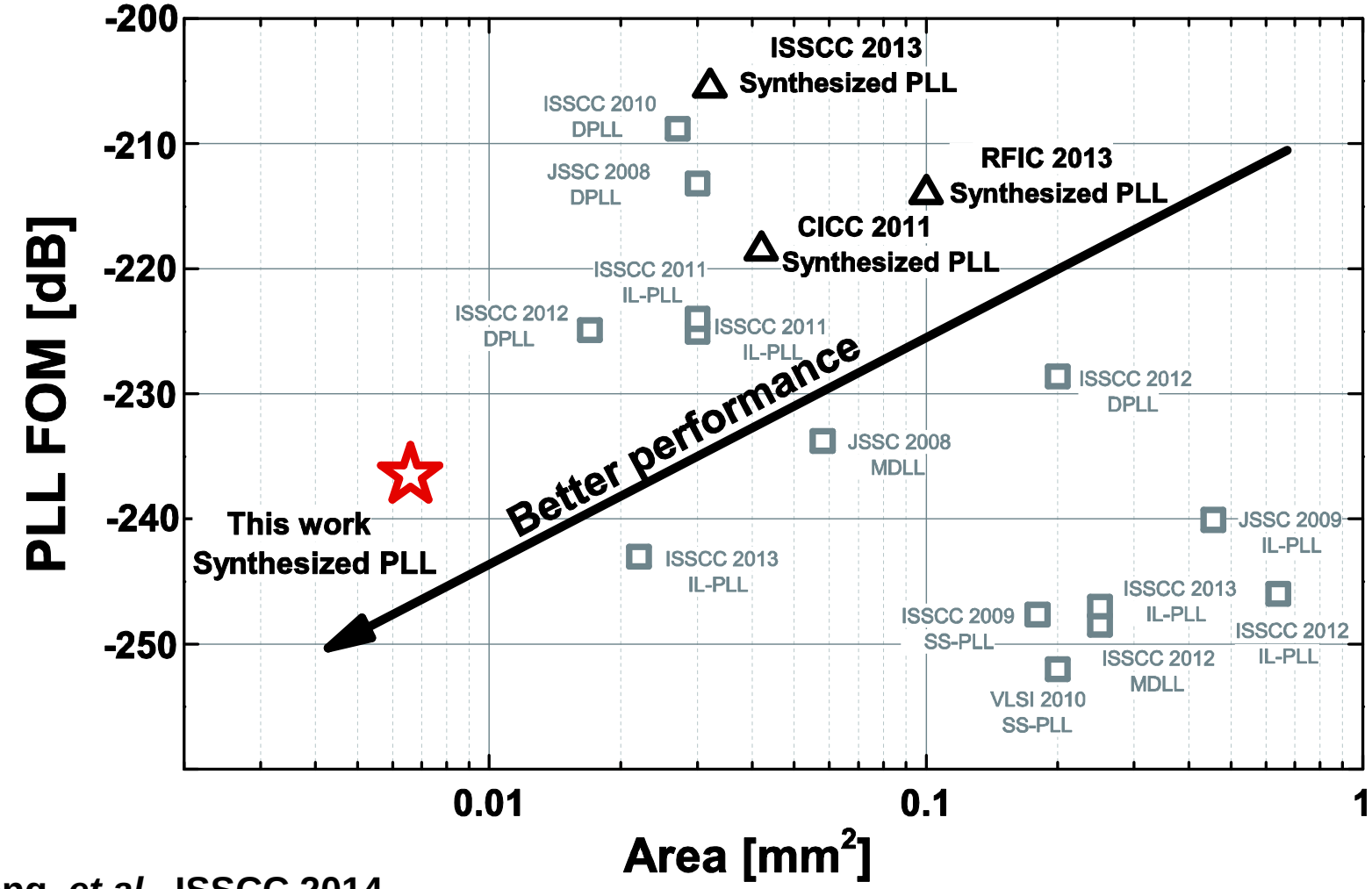
Area: 0.0066mm^2

Jitter: 1.7ps

P_{DC}: 780μW

FOM: -236.5 dB

Comparison of the state-of-the-art PLLs



*W. Deng, *et al*., ISSCC 2014

Comparison of Synthesizable PLL

	This work 65nm	[22] 28nm	[23] 65nm	[24] 65nm
Power [mW]	0.78 @900MHz	13.7 @2.5GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	0.0066	0.042	0.032	0.1
Integ. Jitter [ps]	1.7	N.A.	30	N.A.
RMS Jitter [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	-236.5	-218.6*	-205.5	-214*
W/ custom cells?	No	No	Yes	Yes
Topology	IL-base	TDC-base	TDC-base	TDC-base

*FOM is calculated based on RMS jitter.

Conclusion

- **Digitization *vs* Digitally-Assisted Analog**
- **Digitally-Assisted Analog**

  to Digitally-Designed Analog

  ***e.g.* Synthesizable Analog Circuit**

  portability, scalability, robustness,..

References

[1] F. Gardner, "Interpolation in Digital Modems-Part I: Fundamentals," IEEE Trans. on Communications, Vol. 41, No. 3, pp. 501-507, Mar. 1993.

[2] H. Suzuki, Y. Yamao, and H. Kikuchi, "A Single-Chip MSK Coherent Demodulator for Mobile Radio Transmission," IEEE Trans. on Vecular Technology, Vol. VT-34, No. 4, pp. 157-168, Nov. 1985.

[3] A. Jerng, “Digital Calibration for RF Transceivers,” ISSCC 2012, Tutorial 9.

[4] I. Vassiliou, *et al*., "A Digitally Calibrated 5.15-5.825GHz Transceiver for 802.11a Wireless LANs in 0.18µm CMOS," IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, pp. 2221-2231, Dec. 2003.

[5] S. Lerstaveesin, *et al*., "A Complex Image Rejection Circuit with Sign Detection Only," IEEE Journal of Solid-State Circuits, Vol. 41, No. 12, pp. 2693-2702, Dec. 2006.

[6] T. Tsukizawa, *et al*., "A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-in Self-Calibration for Mobile Applications," ISSCC Dig. Tech. Papers, pp. 230-231, Feb. 2013.

[7] S. Pellerano, R. Mukhopadhyay, A. Ravi, J. Laskar, and Y. Palaskas, "A 39.1-to-41.6GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer in 90nm CMOS," ISSCC Dig. Tech. Papers, pp. 484-485, Feb. 2008.

[8] T. Shima, J. Sato, K. Mizuno, K. Takinami, "A 60 GHz CMOS PLL Synthesizer Using a Wideband Injection-Locked Frequency Divider with Fast Calibration Technique," APMC, pp. 1530-1533, Dec. 2011.

References

[9] W. Deng, A. Musa, K. Okada, and A. Matsuzawa, "A 0.38mm^2, 10MHz-6.6GHz Quadrature Frequency Synthesizer Using Fractional-N Injection-Locked Technique," A-SSCC Dig. Tech. Papers, pp. 353-356, Nov. 2012.

[10] M. Bohr, "The New Era of Scaling in an SoC World," ISSCC Dig. Tech. Papers, pp. 23-28, Feb. 2009.

[11] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.0066-mm^2 780-μW Fully Synthesizable PLL with a Current Output DAC and an Interpolative-Phase Coupled Oscillator using Edge Injection Technique," ISSCC Dig. Tech. Papers, pp. 266-267, Feb. 2014.

[12] S. Weaver, B. Hershberg, and Un-Ku Moon, "Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells," IEEE Transactions on Circuits and Systems-I, Vol. 61, No. 1, pp. 84-91, Jan. 2014.

[13] P. M. Levine, and G. W. Roberts, “A High-Resolution Flash Time-to-Digital Converter and Calibration Scheme,” IEEE International Test Conference, pp. 1148-1157, Oct. 2004.

[14] D. Sheng, *et al*., "An Ultra-Low-Power and Portable Digitally Controlled Oscillator for SoC Applications," IEEE Trans. Circuits and Systems-II, Vol. 54, No. 11, pp. 954-958, Nov. 2007.

References

[15] A. Matsumoto, S. Sakiyama, Y. Tokunaga, T. Morie, and S. Dosho, "A Design Method and Developments of a Low-Power and High-Resolution Multiphase Generation System," IEEE Journal of Solid-State Circuits, Vol. 43, No. 4, pp. 831-843, Apr. 2008.

[16] P. L. Chen, *et al*., "A Portable Digitally Controlled Oscillator Using Novel Varactors," IEEE Trans. Circuits and Systems-II, Vol. 52, No. 5, pp. 233-237, May 2007.

[17] S. Ye, L. Jansson, and I. Galton, "A Multiple-Crystal Interface PLL With VCO Realignment to Reduce Phase Noise," IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, pp. 1795-1803, Dec. 2002.

[18] N. D. Dalt, "An Analysis of Phase Noise in Realigned VCOs," IEEE Transactions on Circuits and Systems-II, Vol. 6, No. 3, pp. 143-147, March 2014.

[19] W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A 0.022mm2 970μW Dual-Loop Injection-Locked PLL with -243dB FOM Using Synthesizable All-Digital PVT Calibration Circuits," ISSCC Dig. Tech. Papers, pp. 248-249, Feb. 2013.

[20] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A Compact, Low Power and Low Jitter Dual-Loop Injection Locked PLL Using All-Digital PVT Calibration," IEEE Journal of Solid-State Circuits, Vol. 49, No. 1, pp. 50-60, Jan. 2014.

References

[21] D. Park, and S. Cho, "A 14.2mW 2.55-to-3GHz Cascaded PLL with Reference Injection, 800MHz Delta-Sigma modulator and 255fsrms Integrated Jitter in 0.13um CMOS," ISSCC Dig. Tech. Papers, pp. 344-345, Feb. 2012.

[22] Y. Park, and D.D. Wentzloff, "An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS," IEEE Custom Integrated Circuits Conf., Oct. 2011.

[23] W. Kim, et al., "A 0.032mm2 3.1mW Synthesized Pixel Clock Generator with 30psrms Integrated Jitter and 10-to-630MHz DCO Tuning Range," ISSCC Dig. Tech. Papers, pp.250-251, Feb. 2013.

[24] M. Faisal, and D.D. Wentzloff, "An Automatically Placed-and-Routed ADPLL for the MedRadio Band using PWM to Enhance DCO Resolution," IEEE Radio Frequency Integrated Circuits Symposium, pp.115-118, Jun. 2013.

Other example:

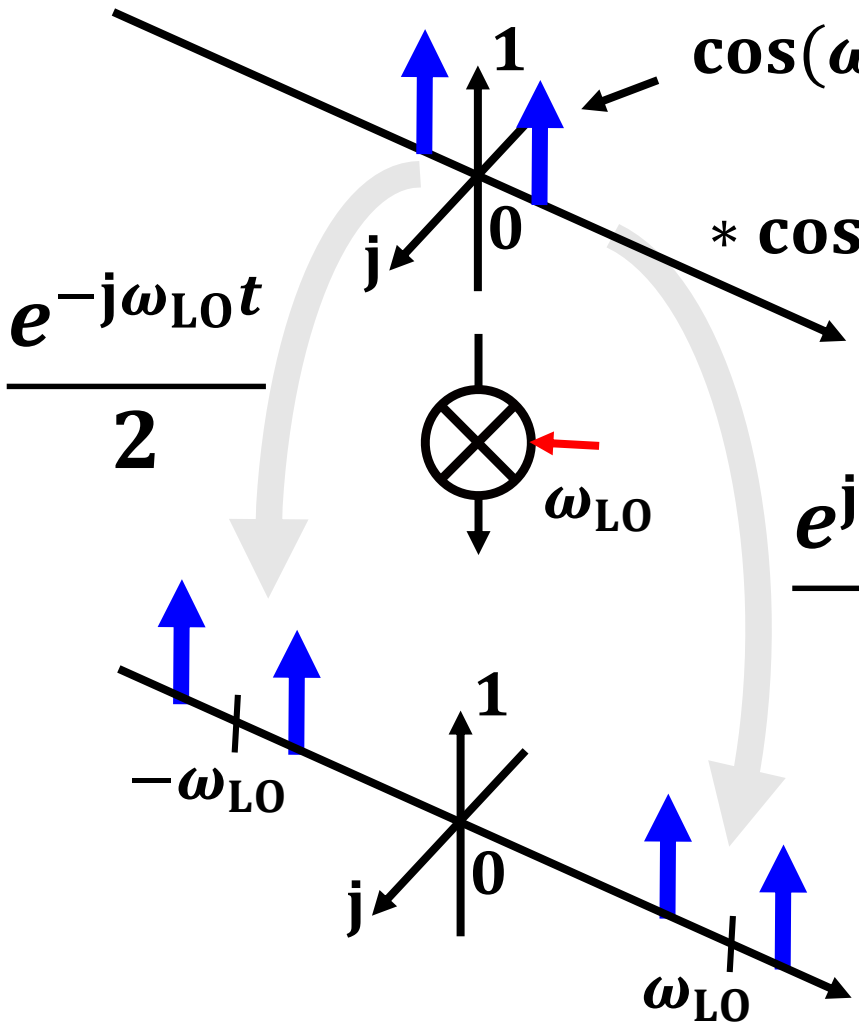
[25] D. Kaczman, et al., "A Single-Chip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE SAW-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2," IEEE JSSC, Vol. 44, No. 3, pp. 718-739, March 2009.

Acknowledgement

This work was partially supported by MIC, SCOPE, MEXT, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

Appendix

Up-conversion by $\cos(\omega_{LO}t)$



$$\cos(\omega_{BB}t) = \frac{e^{j\omega_{BB}t} + e^{-j\omega_{BB}t}}{2}$$

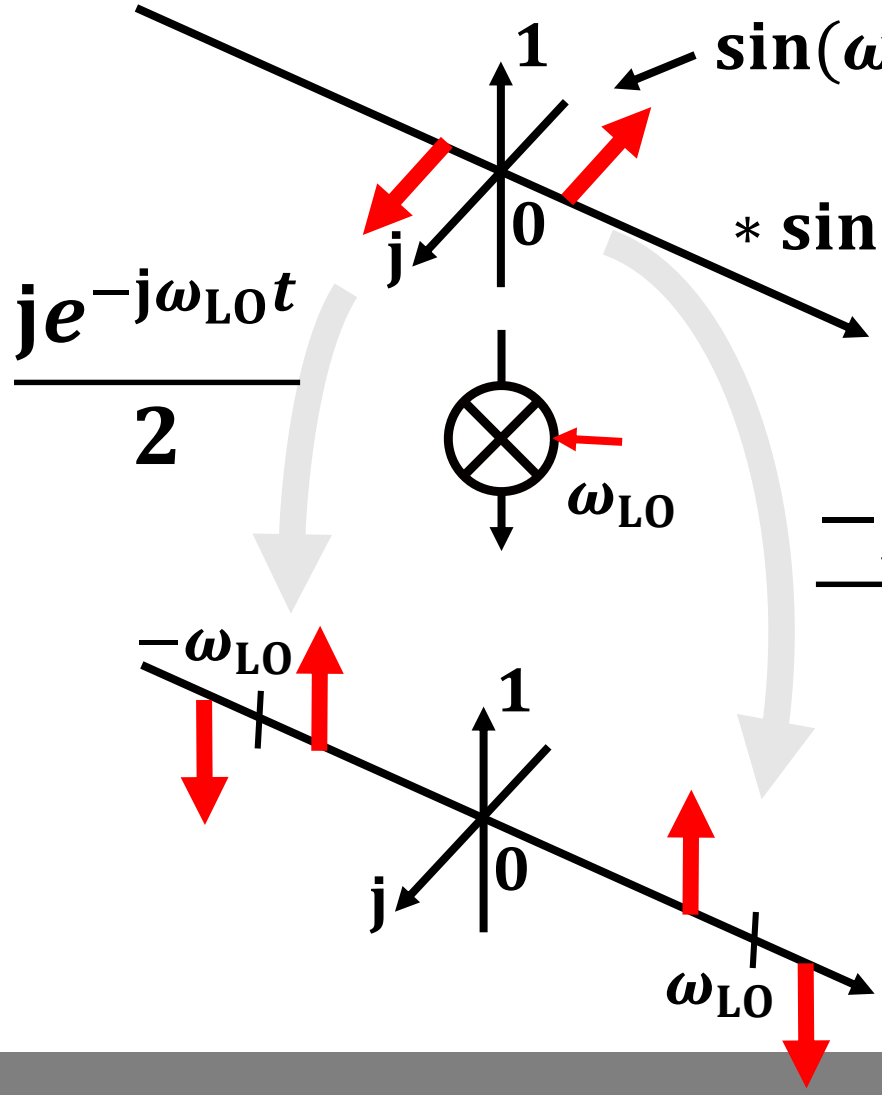
$$* \cos(\omega_{LO}t) = \frac{e^{j\omega_{LO}t} + e^{-j\omega_{LO}t}}{2}$$

$$\frac{e^{-j\omega_{LO}t}}{2}$$

$$\frac{e^{j\omega_{LO}t}}{2}$$

$$\cos(\omega_{BB}t) * \cos(\omega_{LO}t)$$

Up-conversion by $\sin(\omega_{LO}t)$



$$\sin(\omega_{BB}t) = \frac{-je^{j\omega_{BB}t} + je^{-j\omega_{BB}t}}{2}$$

$$* \sin(\omega_{LO}t) = \frac{-je^{j\omega_{LO}t} + je^{-j\omega_{LO}t}}{2}$$

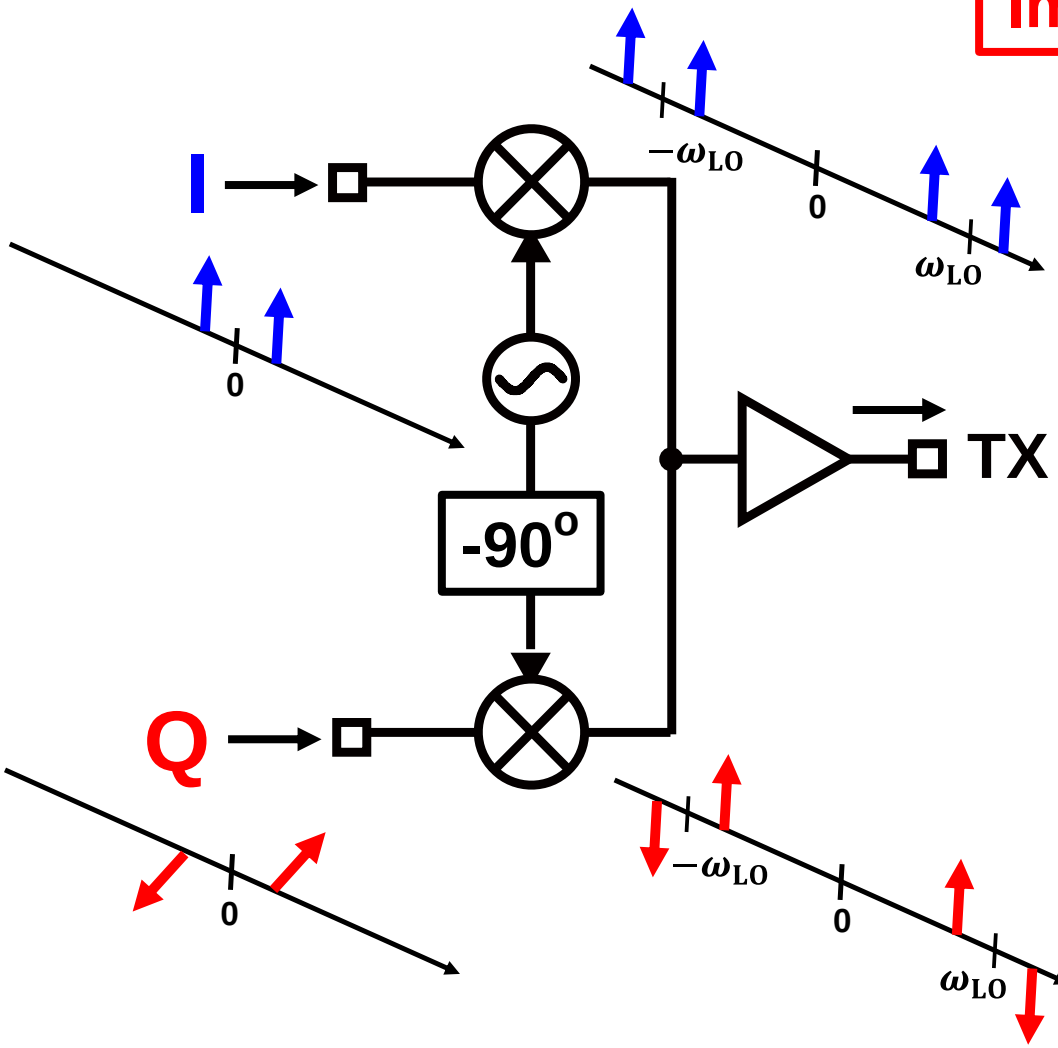
$$\frac{je^{-j\omega_{LO}t}}{2}$$

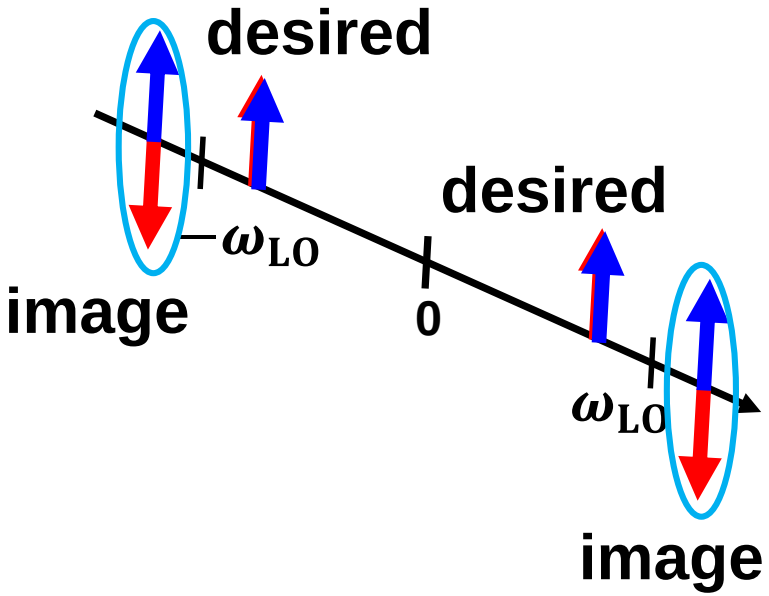
$$\frac{-je^{j\omega_{LO}t}}{2}$$

$$\sin(\omega_{BB}t) * \sin(\omega_{LO}t)$$

Ideal I/Q Up-Conversion

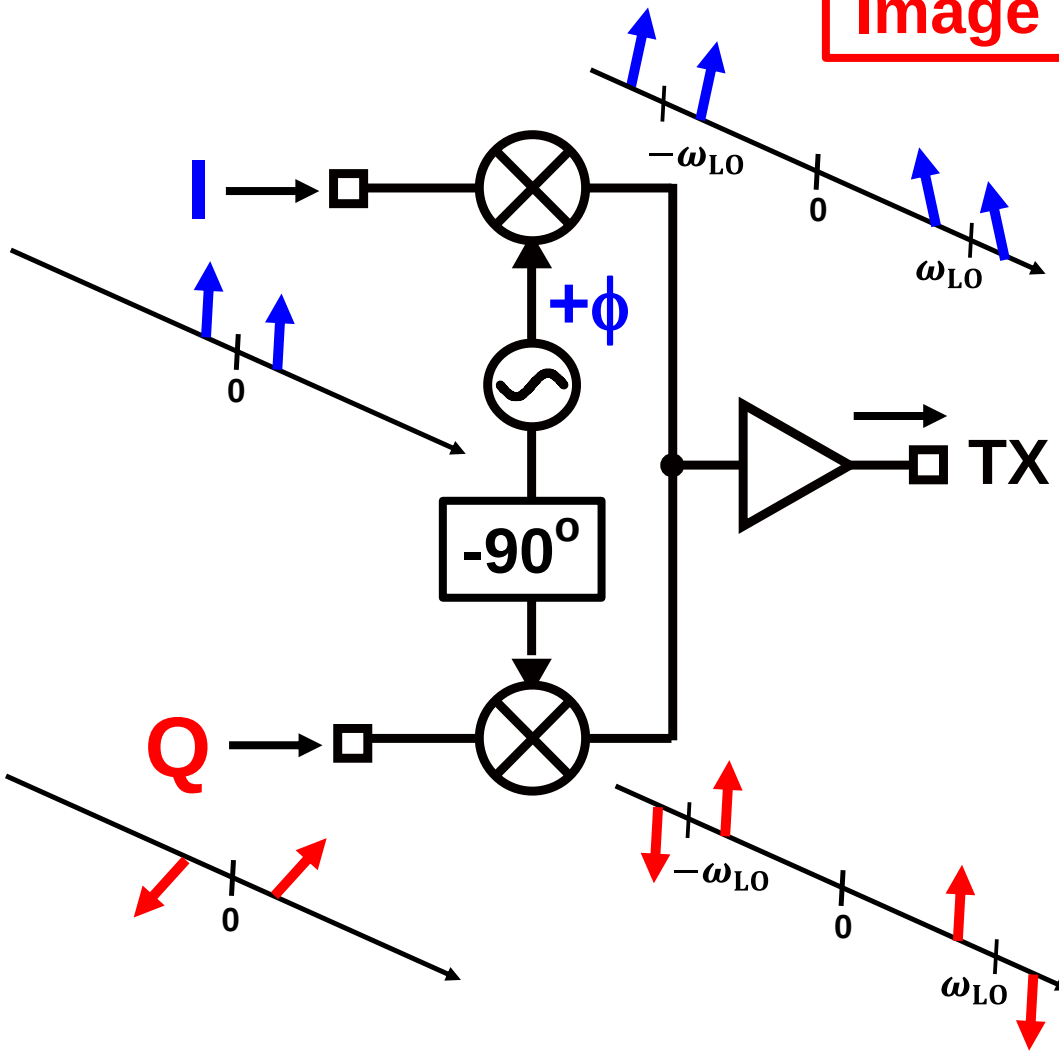
Image signals are canceled.

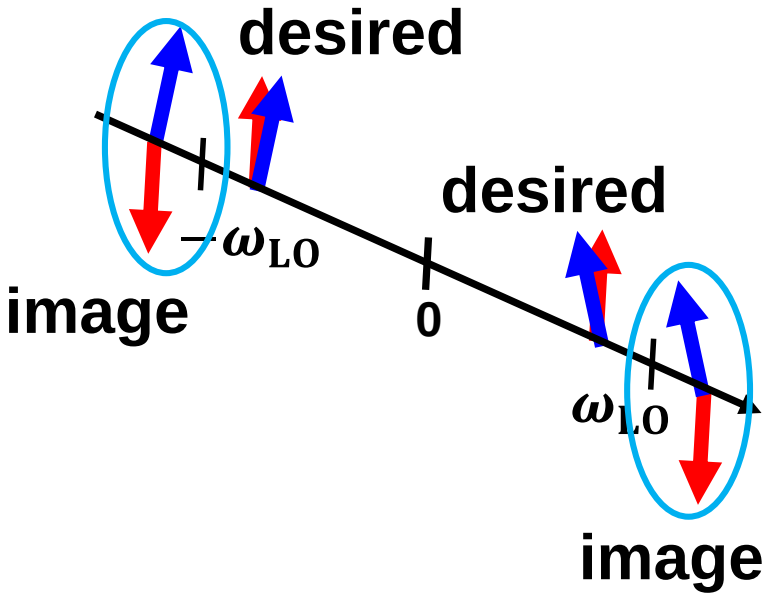




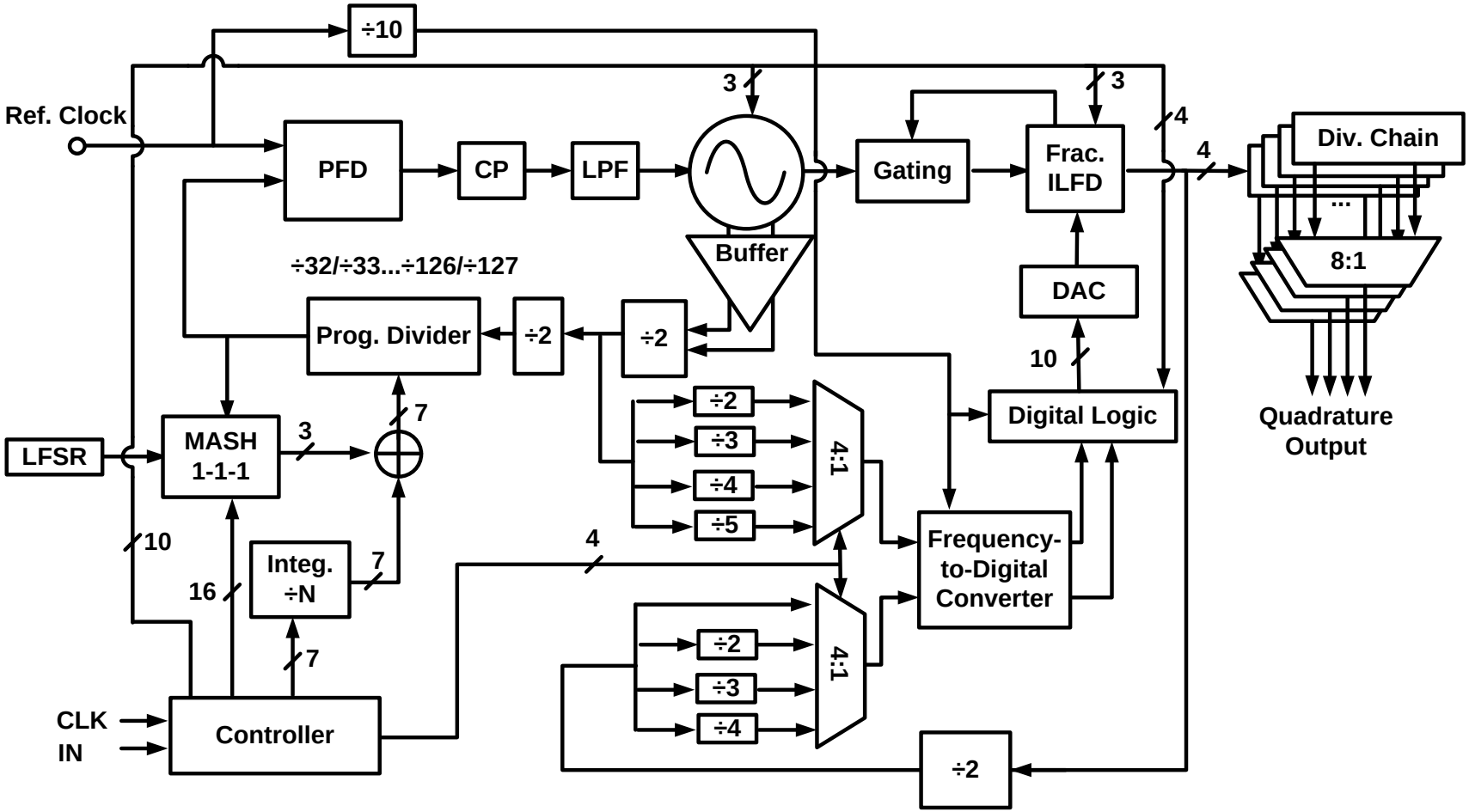
I/Q Up-Conversion with Mismatch

Image signals are NOT canceled.



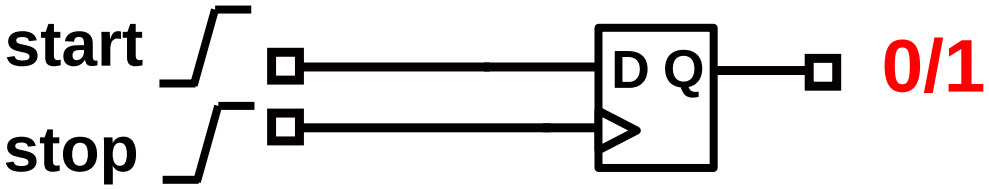


Calibration of Injection Lock Oscillator

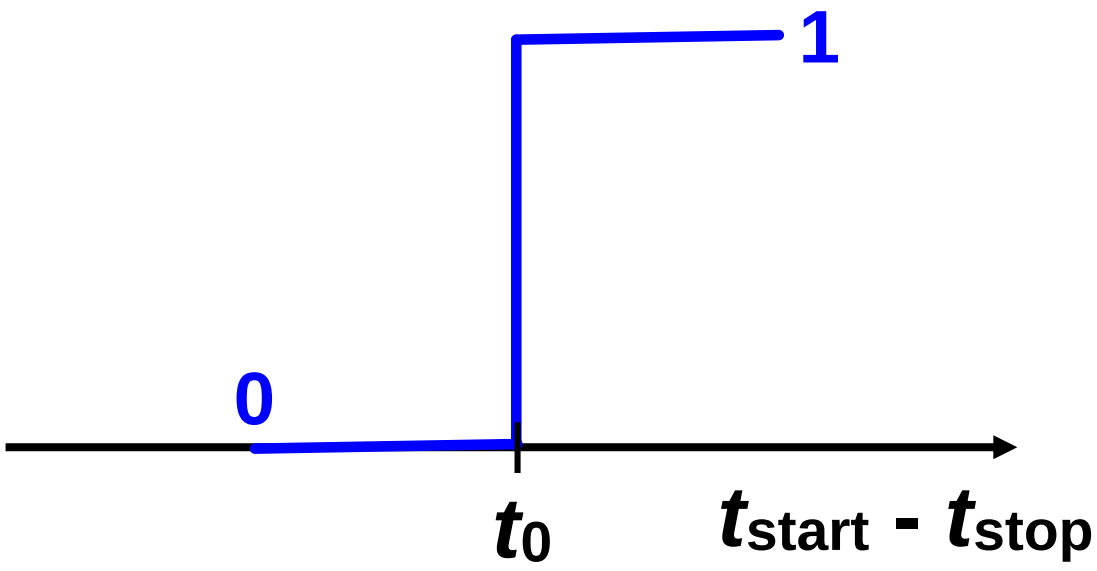


*W. Deng, *et al*., A-SSCC 2012

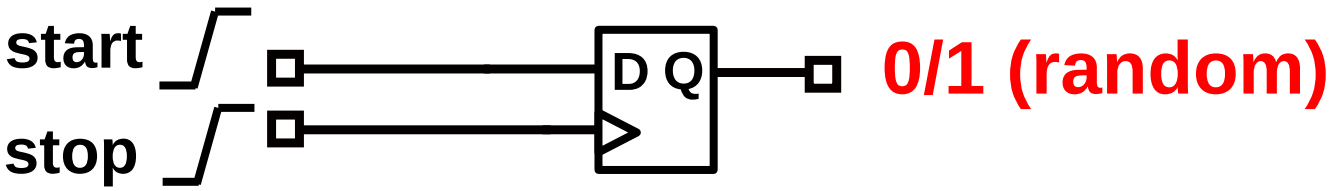
Stochastic TDC



Ideal condition (no noise, no PVT)

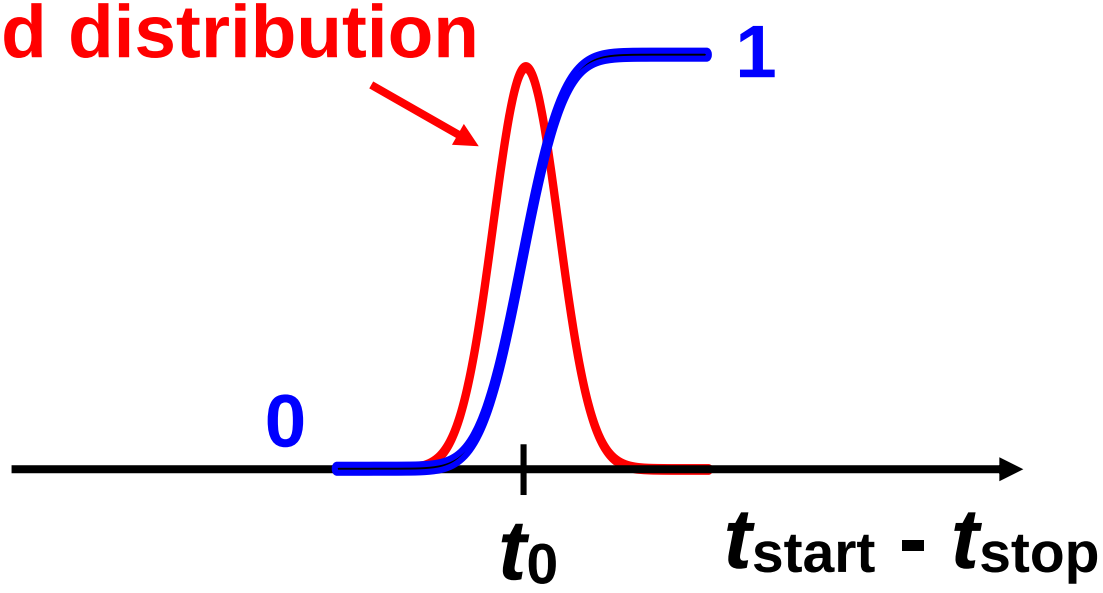


Stochastic TDC



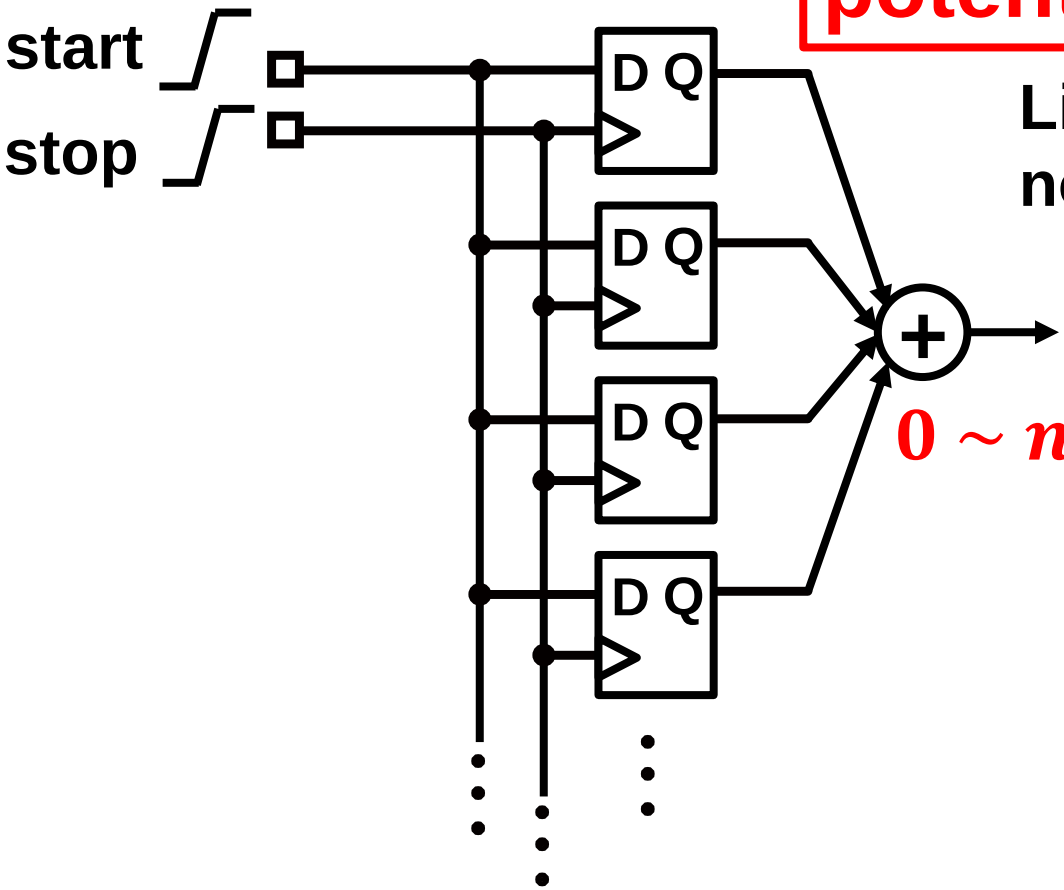
Noise & Process variation

threshold distribution

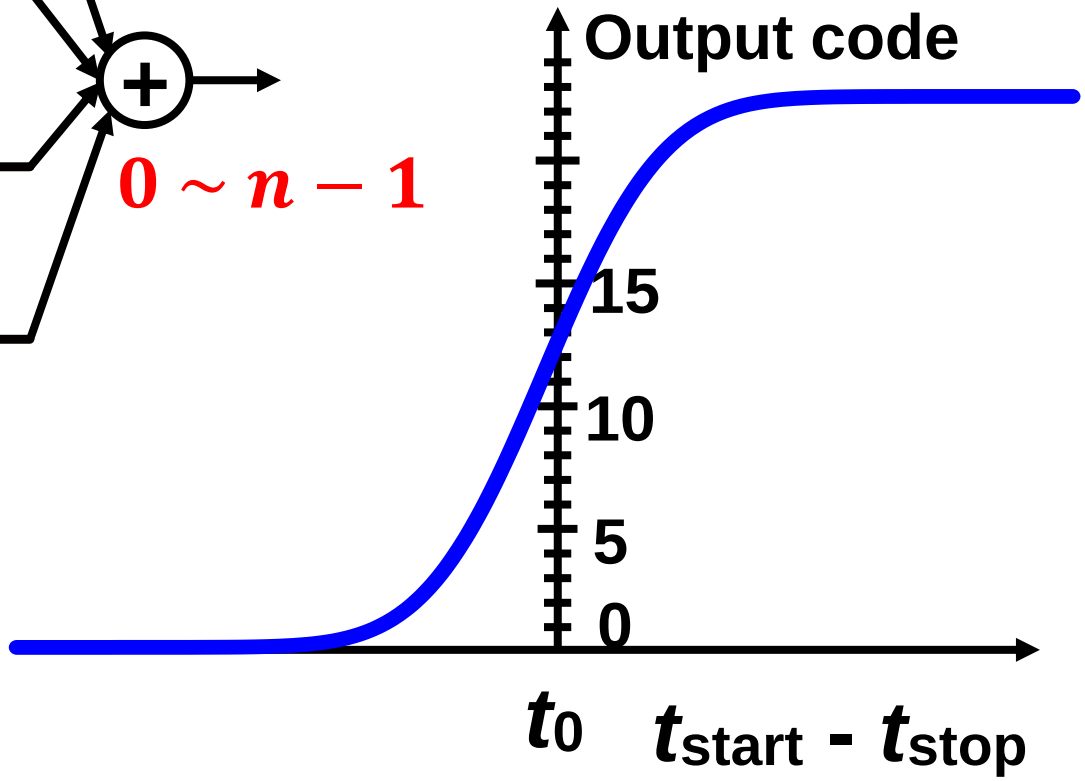


Stochastic TDC

potentially synthesizable

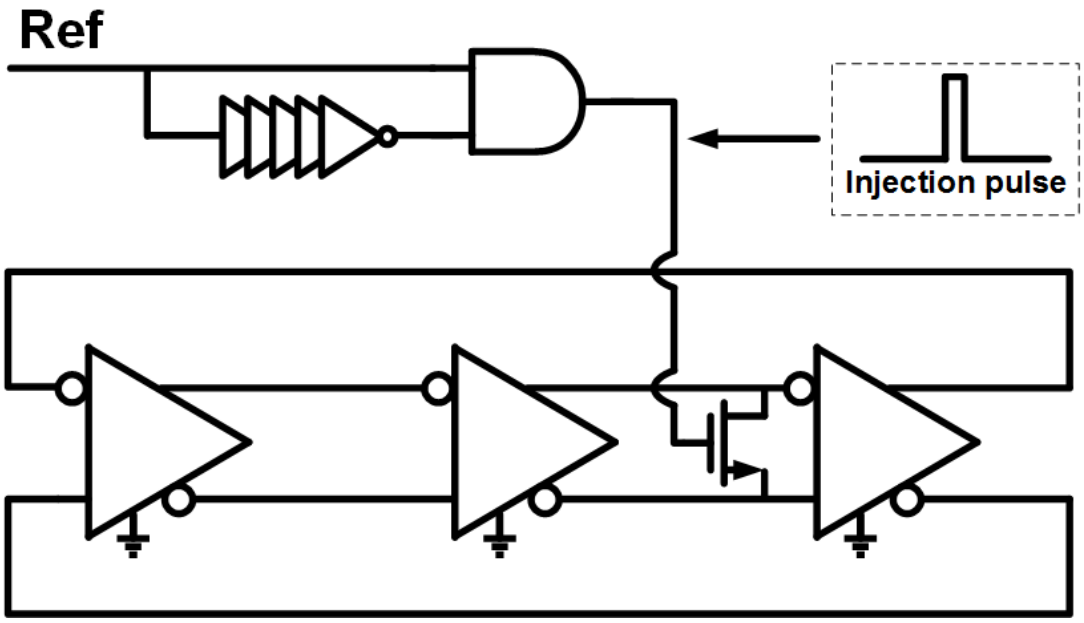


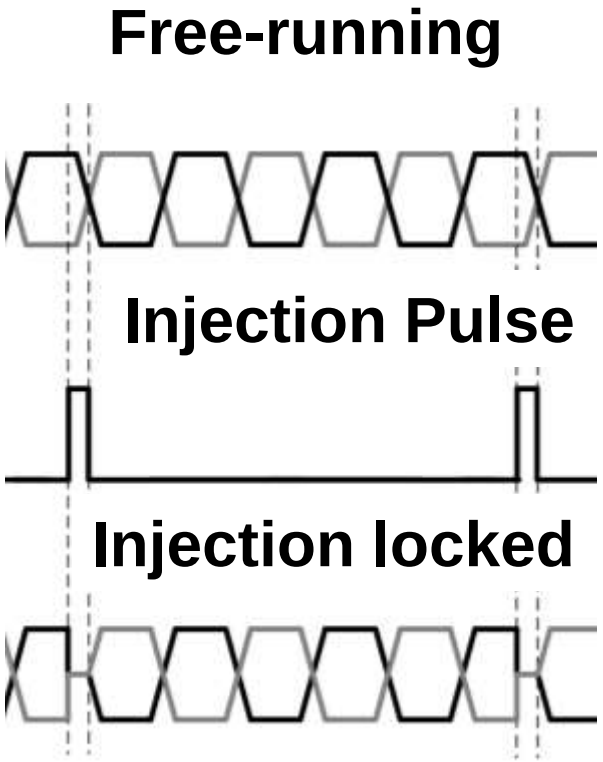
Linearity compensation is not very difficult.



*P. M. Levine, *et al*., IEEE ITC 2004

Pulse Injection

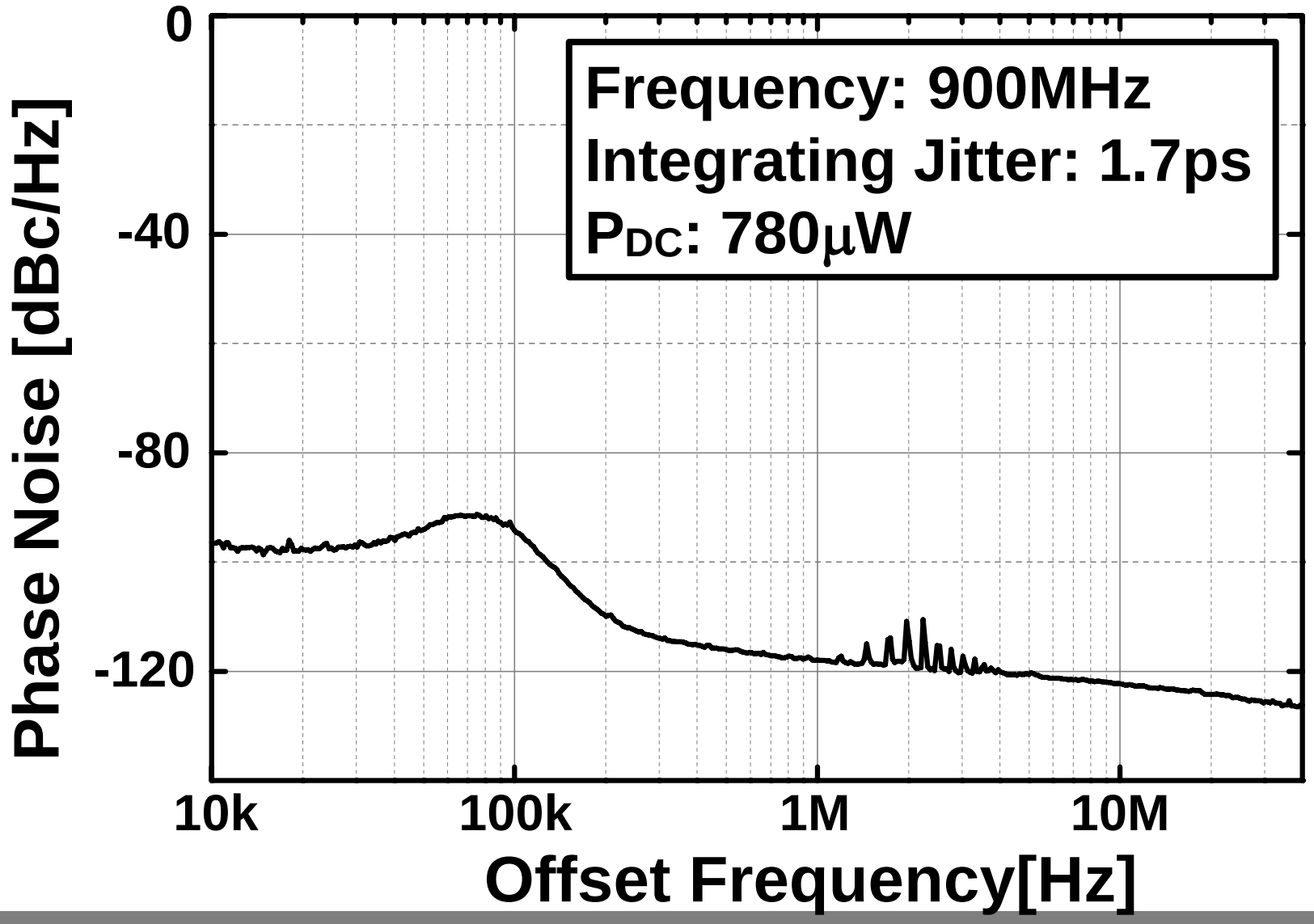




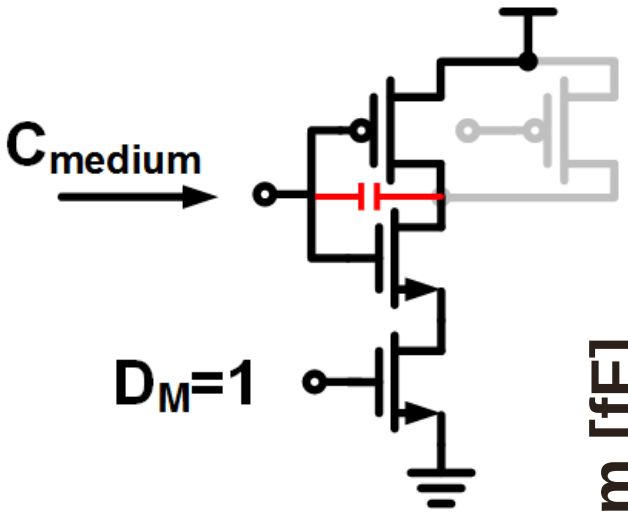
- **Severe timing design** is required on the injection pulse width.

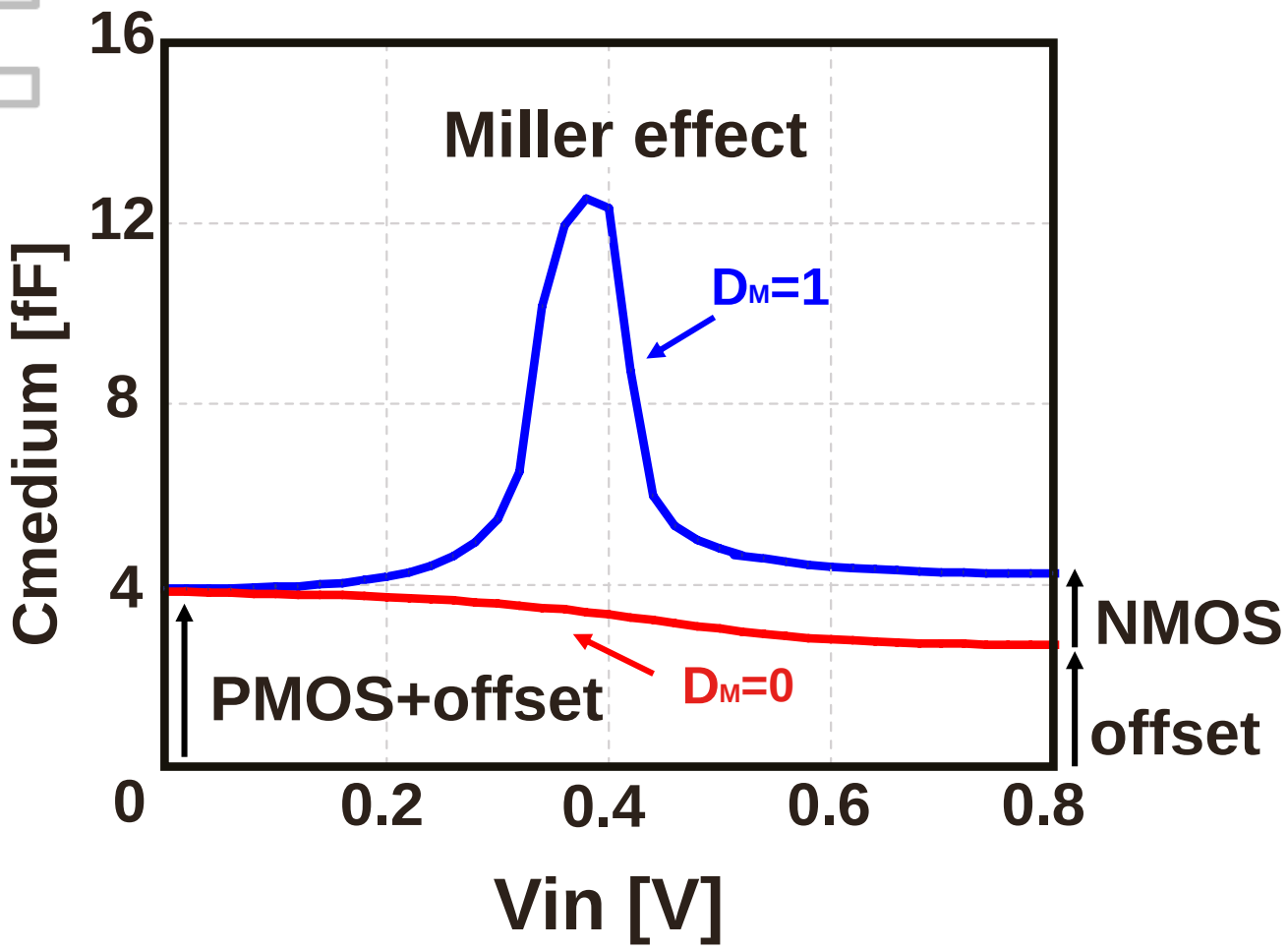
*B. Helal, *et al.*, JSSC 2009

Measured Phase Noise



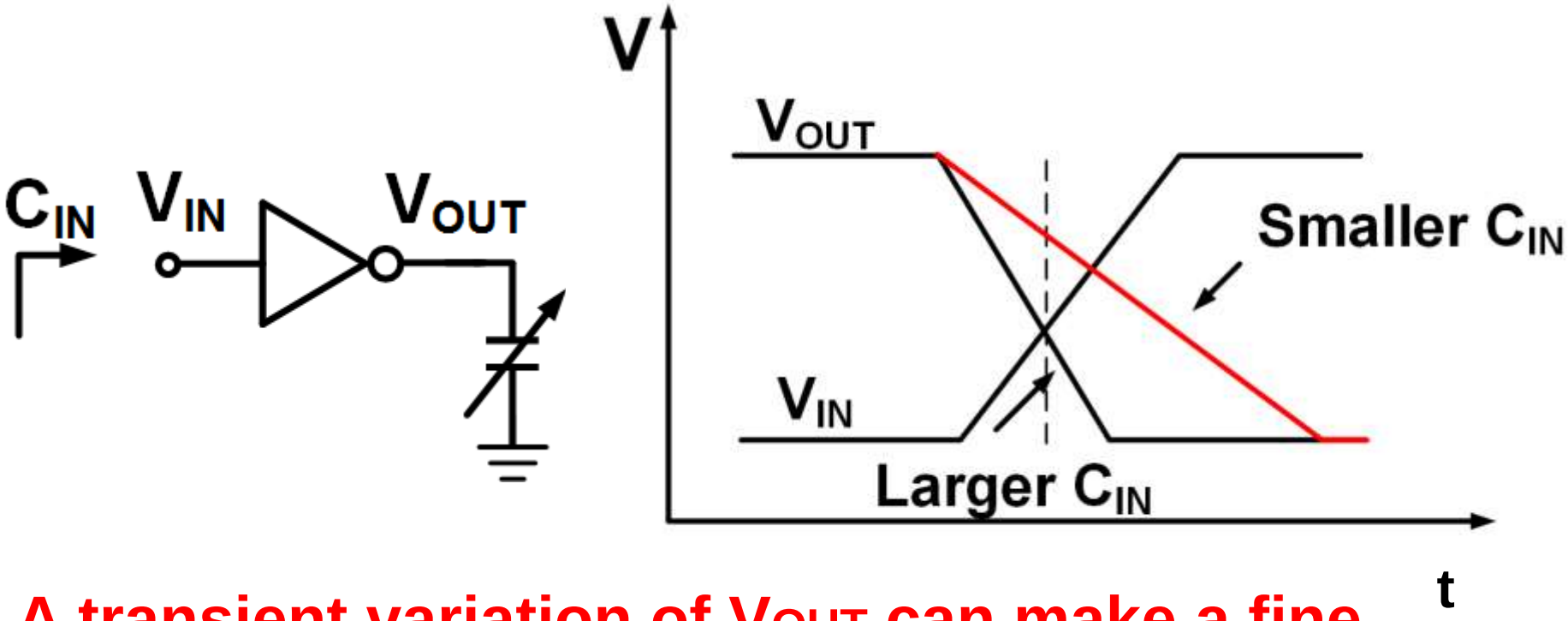
Simulated C_{medium} against V_{in}





Fine Varactor

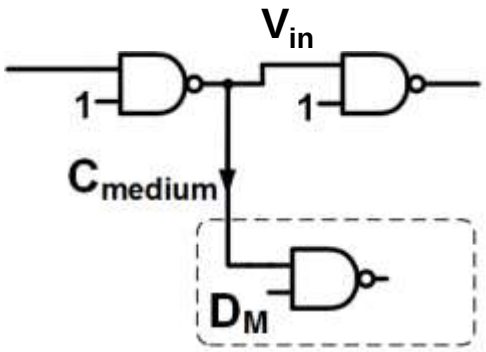
Miller effect is gain-dependent.



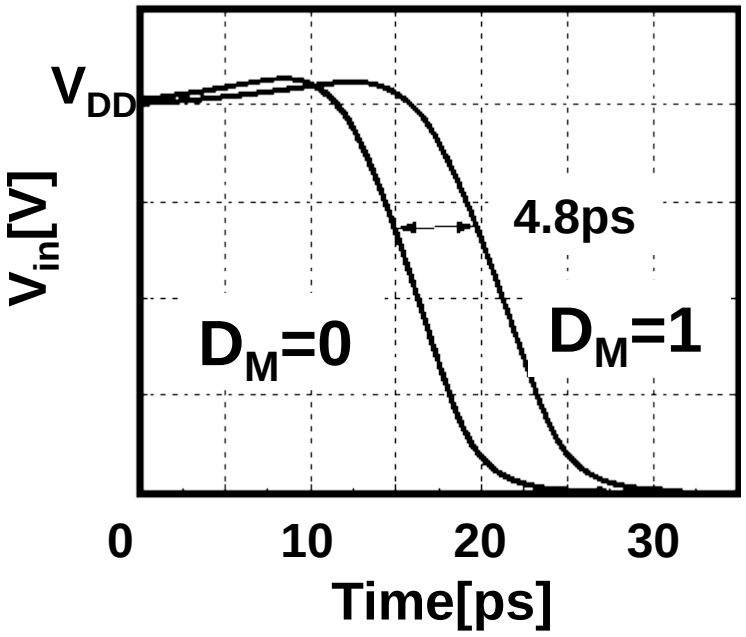
A transient variation of V_{OUT} can make a fine capacitance difference in C_{IN}.

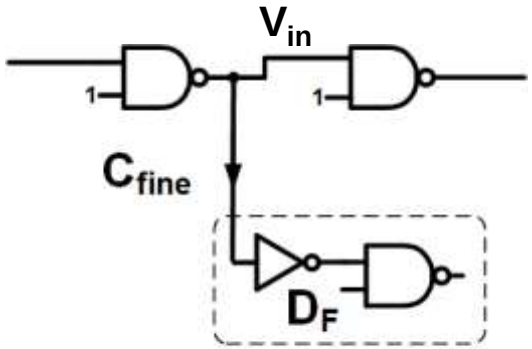
*W. Deng, *et al*., ISSCC 2014

Fine Varactor (cont.)

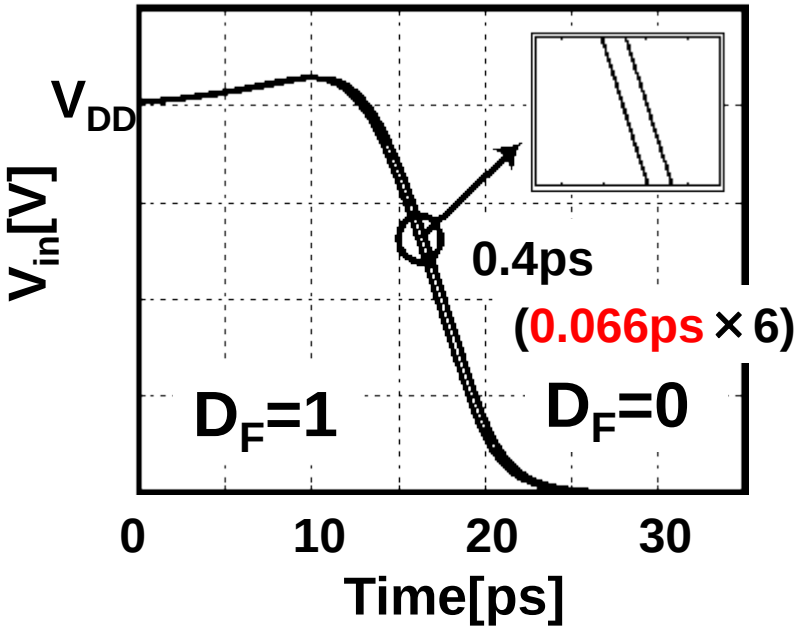


Medium resolution





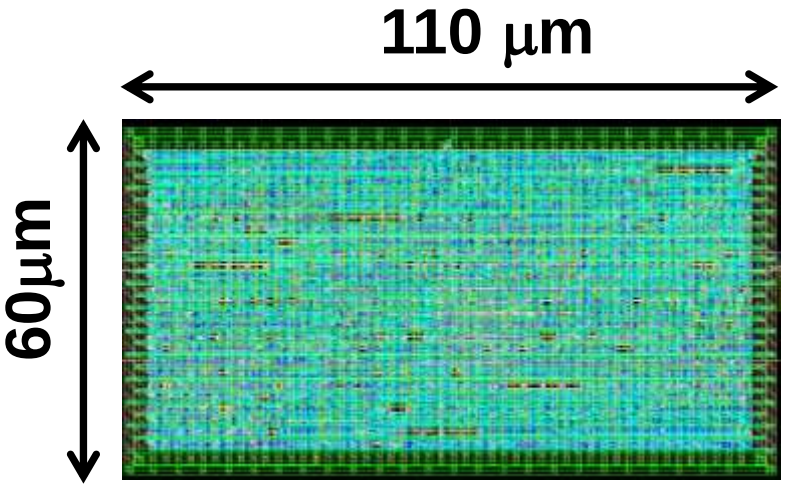
Fine resolution



*W. Deng, *et al.*, ISSCC 2014

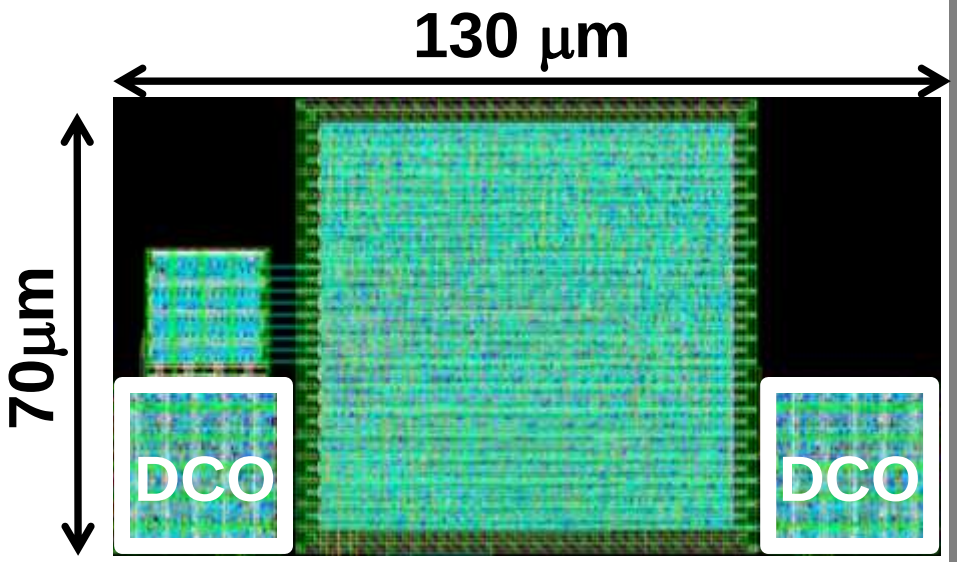
Robust for Layout Uncertainty

Integrating Jitter: 1.7ps
P_{DC}: 780μW
FOM: -236.5 dB



Fully synthesized (proposed)

Integrating Jitter: 2.32ps
P_{DC}: 640μW
FOM: -234.6 dB



Hierarchical P&R with synthesized DCOs (for comparison)