High-Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits

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Abstract

A novel helium-3 ion bombardment technique is proposed for creating locally semi-insulating substrate areas. A helium-3 dose of only $1.5x10^{13}cm^{-2}$ increases a Si substrate resistivity from 6Ω-cm to 1.5kΩ-cm, which improves the quality factor of a 2-nH inductor with a 140μm-diameter by 38% (Q=16.3). An aluminum mask is used for covering active areas, and at most 15-μm distance from the mask edge is required to avoid the p-n junction leakage. The proposed technique is applied to an 8-GHz oscillator, and an 8.5-dB improvement in the measured phase noise has been achieved.

Keywords: Inductor, Helium-3 Bombardment, and CMOS

Introduction

The on-chip spiral inductor is one of the most important key components in RF CMOS circuits. The proton bombardment [1-3] and the use of post-passivation interconnect (PPI) [4] have been proposed for realizing high-Q inductors. The PPI inductor cannot be used for high-frequency applications due to a large parasitic in long interconnections between an inductor and circuit, resulting in a low self-resonance frequency of 16GHz [4]. The bombardment technique can be applied even for millimeter-wave circuits, and can also be used for making an isolation area between noisy digital circuits and noise-sensitive analog circuits [2]. However, the conventional proton bombardment [1-3] requires an enormous dose amount of $10^{15}cm^{-2}$ to keep a resistivity of more than 10^{4}Ω-cm for an originally 15Ω-cm substrate [2], which results in less reliability and high process cost. In this work, a helium-3 bombardment is proposed, which can realize a shallow implantation as compared with the proton one. The helium-3 has 9.1-times higher irradiation efficiency and can reduce the dose amount, moreover, helium-3 has less lateral scattering than proton, which realizes higher reliability and lower process cost.

Helium－3 Bombardment

Fig. 1 explains a simplified process of the helium-3 bombardment. A cyclotron is used for the helium-3 irradiation, and a 0.5mm-thick aluminum mask plate is used to protect transistors. Due to charge trappings created by the irradiation and Coulomb scattering of the charged traps [1,2], the substrate resistivity becomes higher depending on the dose amount as shown in **Fig. 2**. **Fig. 3** shows the measured resistivity profile, and the bombardment conditions have been summarized in **Table 1**. For the condition #1, a helium-3 dose of $1x10^{13}cm^{-2}$ is irradiated twice into the target depth of 15μm and 30μm, which corresponds to the two peaks in **Fig. 3**. The calculated beam spread range both for helium-3 and proton by using an ion-implantation simulator (TRIM) calculating 10 thousand times are compared in **Fig. 4**. For a 100-μm stopping range, the beam spread range of helium-3 is only 6.8μm, while that of proton more than 10μm, both with the assumption that 95% ion falls within the spread range, which causes greater difference when ion irradiated from the bottom of silicon substrate. **Fig. 5** shows the electromagnetic (EM) simulation results of the distribution of the power to weight ratio for a 140-μm diameter spiral inductor with/without the bombardment.

Experimental Results

Figs. 6 and 7 show the measured inductances and quality factors with/without the bombardment (condition #2), and a 38-% Q-factor improvement is achieved for the 2-nH inductor, while the inductance has little change. **Fig. 8** shows the TEG structure for evaluating the p-n junction leakage. Transistors are arranged at various positions (A1-A5, B1-B5). The width of irradiated area is 294μm. The transistors at A1 and B1 are exposed while the others are covered by the aluminum mask. **Fig. 9** shows the leakage current as a function of distance from the mask edge before/after the bombardment. The distance of at most 15μm is a required margin including the mask alignment, while 50μm is required in the proton bombardment [3] due to the enormous dose amount and lateral scattering.

A voltage control oscillator (VCO) is implemented by the same CMOS technology for evaluating the phase noise improvement. **Fig. 10** shows a circuit schematic, and **Fig. 11** shows a micrograph with the irradiated area. **Fig. 12** shows the measured phase noise with/without the bombardment (condition #2). The phase noise without the bombardment is -94.0dBc/Hz at 1MHz-offset while -102.5dBc/Hz is achieved by the bombardment with the same 5.6mW power consumption. The power consumption of 18.0mW is required to achieve the same phase noise performance without the bombardment.

Conclusion

The proposed helium-3 bombardment can improve the quality factor of on-chip inductors by the local semi-insulated 1.5kΩ-cm substrate and achieve the 8.5-dB phase-noise improvement in the 8-GHz oscillator. The required dose amount can be successfully reduced from $1.0x10^{15}cm^{-2}$ to $1.5x10^{13}cm^{-2}$, and the placement margin from the mask edge can be reduced from 50μm to 15μm compared to the proton bombardment.

Acknowledgements

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References

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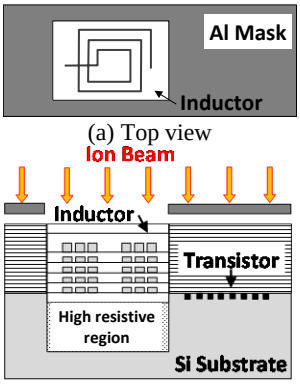


Fig. 1: Helium-3 bombardment process. For covering active areas, a 0.5mm-thick aluminum plate is used as a mask from the irradiation.

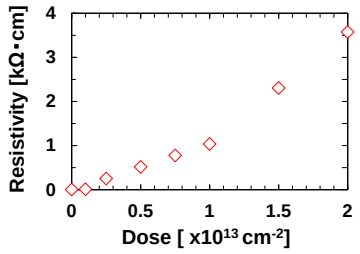


Fig. 2: Substrate resistivity with dose amount.

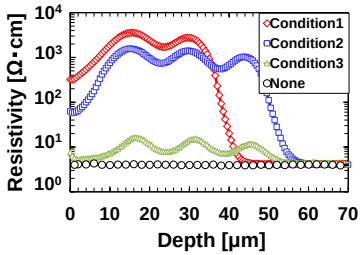


Fig. 3: Substrate resistivity variation as a function of depth from the surface of Si wafer with various conditions (Table 1).

Cond.	Total time [s]	Target irradiation depth [μm]	Total dose [cm^{-2}]
#1	444	15, 30	2.0 x10^{13}
#2	332	15, 30, 45	1.5 x10^{13}
#3	66	15, 30, 45	3.0 x10^{12}

Table 1: Conditions of the irradiation in Fig. 3. Each peak in resistivity corresponds to the target irradiation depth.

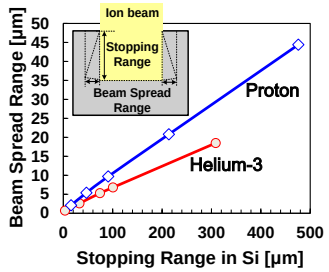


Fig. 4: Calculated beam spread range with respect to ion stopping range in silicon by using TRIM calculating 10 thousand times with 95% ion falling within the range.

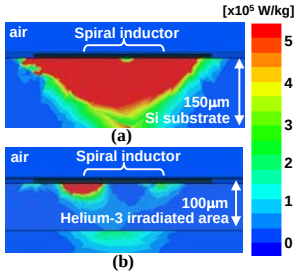


Fig. 5: Electromagnetic simulation results of specific absorption rate (SAR) wo (a) / w (b) 100μm-depth helium-3 bombardment, which contributes to drastically reducing the absorption into the lossy Si substrate.

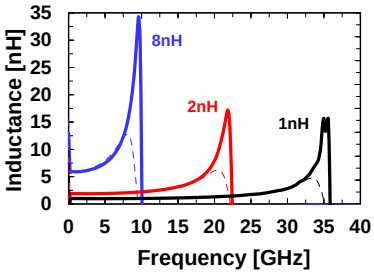


Fig. 6: Inductance (1nH, 2nH, and 8nH) with (solid lines) and without (dotted lines) the helium-3 bombardment. Condition #2 in Table 1 is applied.

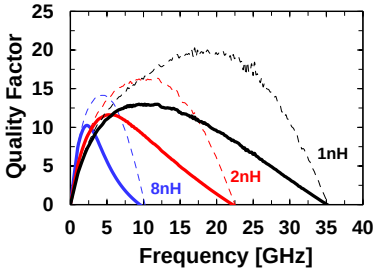


Fig. 7: Quality factor of inductors (1nH, 2nH, and 8nH) with (solid lines) and without (dotted lines) the helium-3 bombardment. Condition #2 in Table 1 is applied. The Q improvement ratios are 36% (Q=10.3 to 14.1), 38% (Q=11.6 to 16.3), and 54% (Q=13.0 to 20) for 8nH, 2nH, and 1nH inductors, respectively. The peak frequencies are shifted to higher while the self-resonance frequencies are not changed.

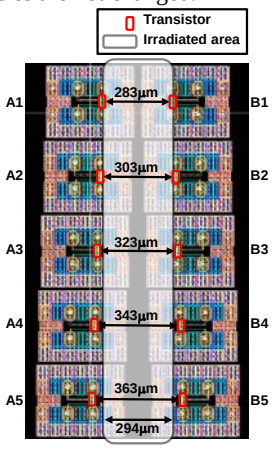
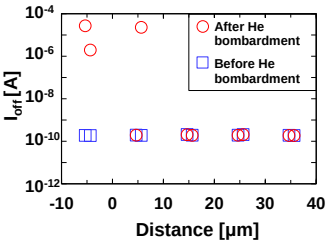
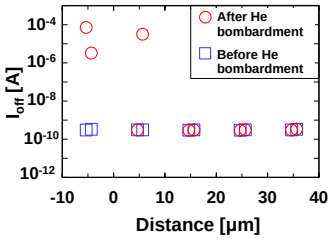


Fig. 8: TEG structure for evaluating transistor damage from the bombardment.



(a) Transistor width of 40μm



(b) Transistor width of 60μm

Fig. 9: Leakage current at V_{gs}=0V as a function of distance from the mask edge. The same transistors are measured before/after the bombardment. The distance of at most 15μm is a required margin including the mask alignment.

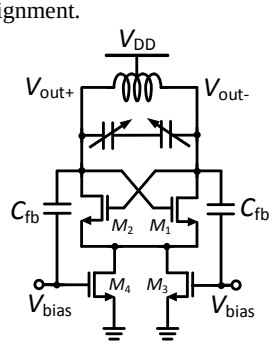


Fig. 10: Circuit schematic of tail-feedback voltage control oscillator (VCO), designed for 8-GHz oscillation. A 1-nH inductor is used.

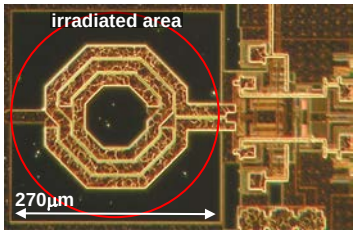


Fig. 11: VCO chip photo with the irradiated area (condition #2). The active area covered by the aluminum mask.

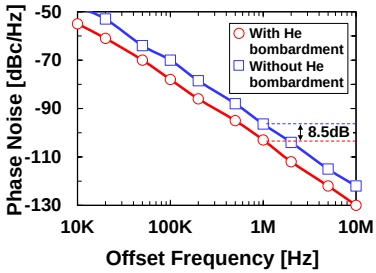


Fig. 12: Measured phase noise with/without the bombardment. An 8.5-dB improvement is achieved with the same 5.6-mW power consumption.