High-Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits

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Outline

- Background
- Motivation
- Conventional Methods to improve inductor quality factor
- Helium-3 Bombardment
- Experimental Results
  - Quality Factor Improvement
  - Reliability
  - VCO Phase Noise Improvement
- Conclusion

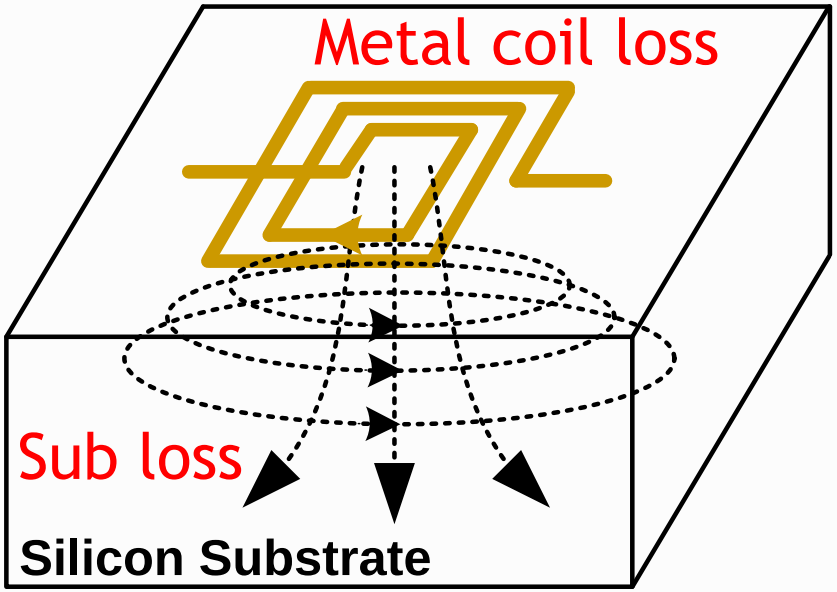
Background

- CMOS on-chip inductors are indispensable for RF circuits.
  - High integration
  - No need for 50-Ω interface
  - VCO, LNA, PA, etc

- RF circuits suffer from the poor performance.
  - Thin metal line
  - Low substrate resistivity less than 10Ω·cm
  - Q is around ten for on-chip inductor.

Inductor Loss Mechanisms

- Losses by currents in metal coil
  - Ohmic loss, Skin effect, Proximity effect
  - Improved by using thick metal
- Substrate loss
  - Eddy currents in substrate



$$Q(\omega) \cong \frac{\omega L}{R}$$

Q: quality factor
ω: frequency in radius
L: inductance
R: parasitic resistance

Ref.: Bunch, IEEE Microwave magazine June 2002.

Motivation

- Improve quality factor of on-chip inductors by decreasing silicon substrate loss

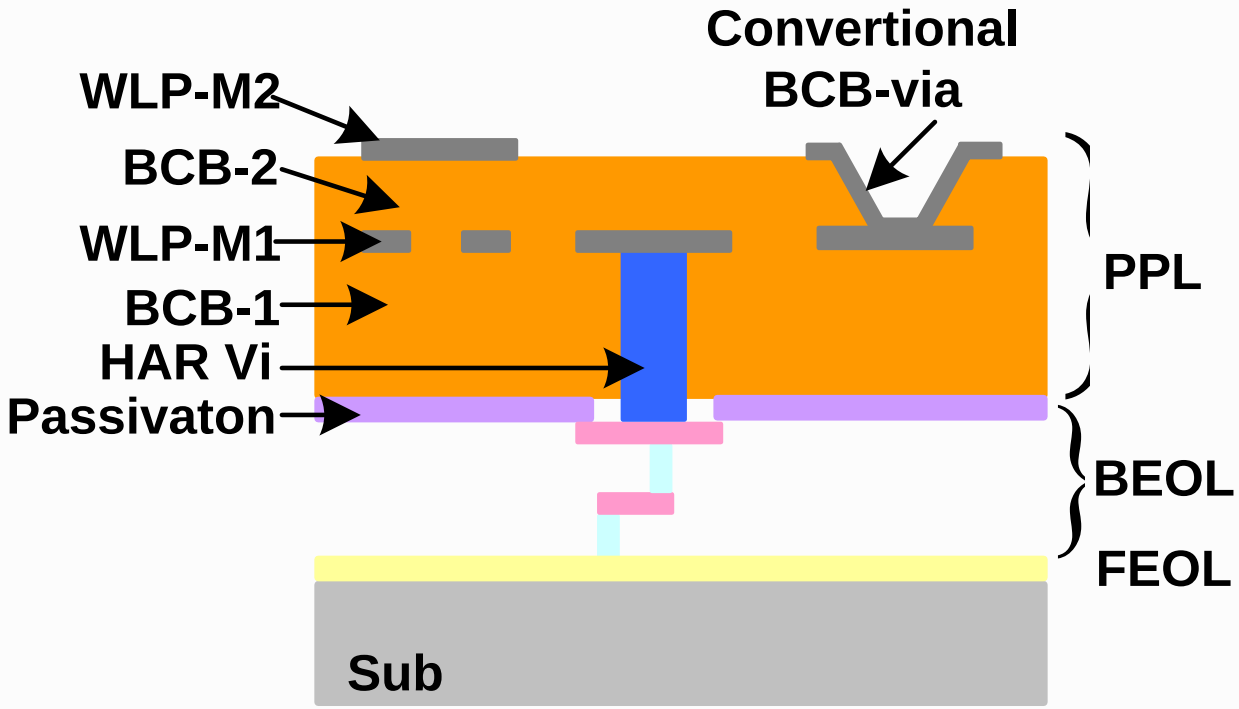
- Ensure circuits working well
  - No damage on active devices

Conventional Methods to Improve Q

- Post-passivation interconnect (PPI)
- Proton Implantation

Conventional Methods to Improve Q

- Post-passivation interconnect (PPI)
  - limited to wafer level packaging (WLP)
  - Large parasitic from the high aspect ratio via (HAR vi)

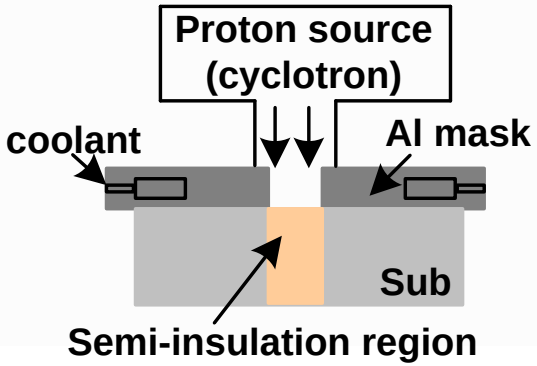


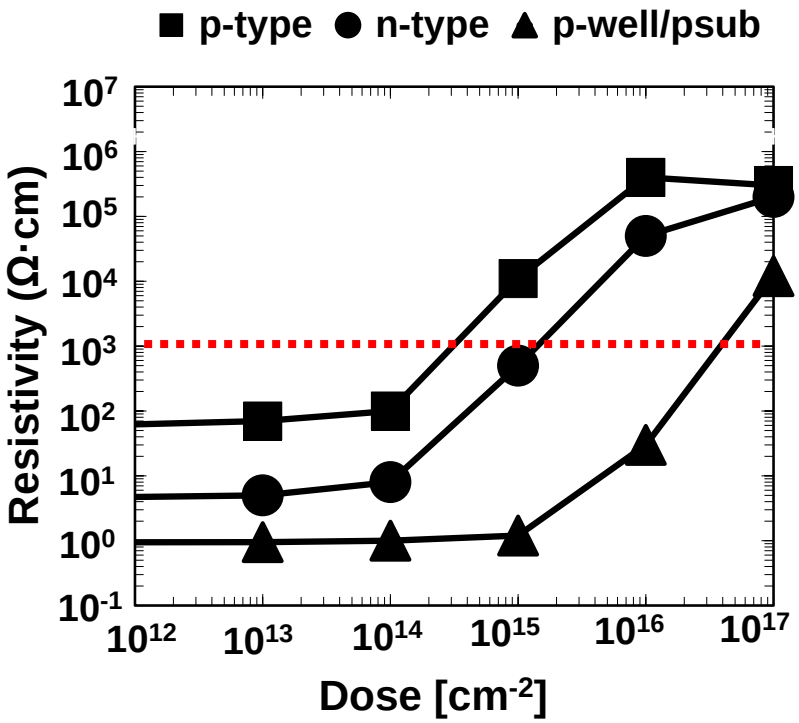
Schematic Cross section of PPI

Reference: [1], C. C. Liu et al., IEDM 323, 2012. [2], G. J. Carchon, et al., MTT 2004

Conventional Methods to Improve Q (Cont'd)

- Proton bombardment
  - Good performance
  - Large dose amount
    - For R_{sub}>1kΩ, about $10^{15}cm^{-2}$
  - High cost
    - 10^{15}-cm^{-2} dose amount needs more than 3h.
  - Poor reliability
    - 50-μm margin





Reference: [1], L. S. Lee, et al., TED 2001. [2] D. D. Tang, *et al*, IEDM 2003.

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Why Helium-3?

Method	Reliability	Cost	Performance
Thick metal[1]	Good	Fair	Good (thickness limitation)
PPI[2]	Good	High	Good (Package limitation)
Silicon on Insulator[3]	Good	Very High	Fair(failed in high freq.)
Proton[4]	Poor	High	Good
Helium-3 (This work)	Good	Fair	Good

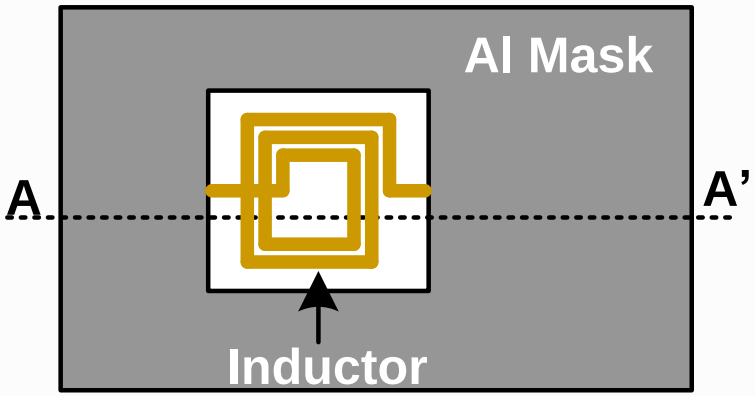
Compared to Proton, Helium-3

- higher vacancies generation ability
- higher irradiation efficiency
- High throughput
- less lateral scattering
- less dose amount
- less process cost

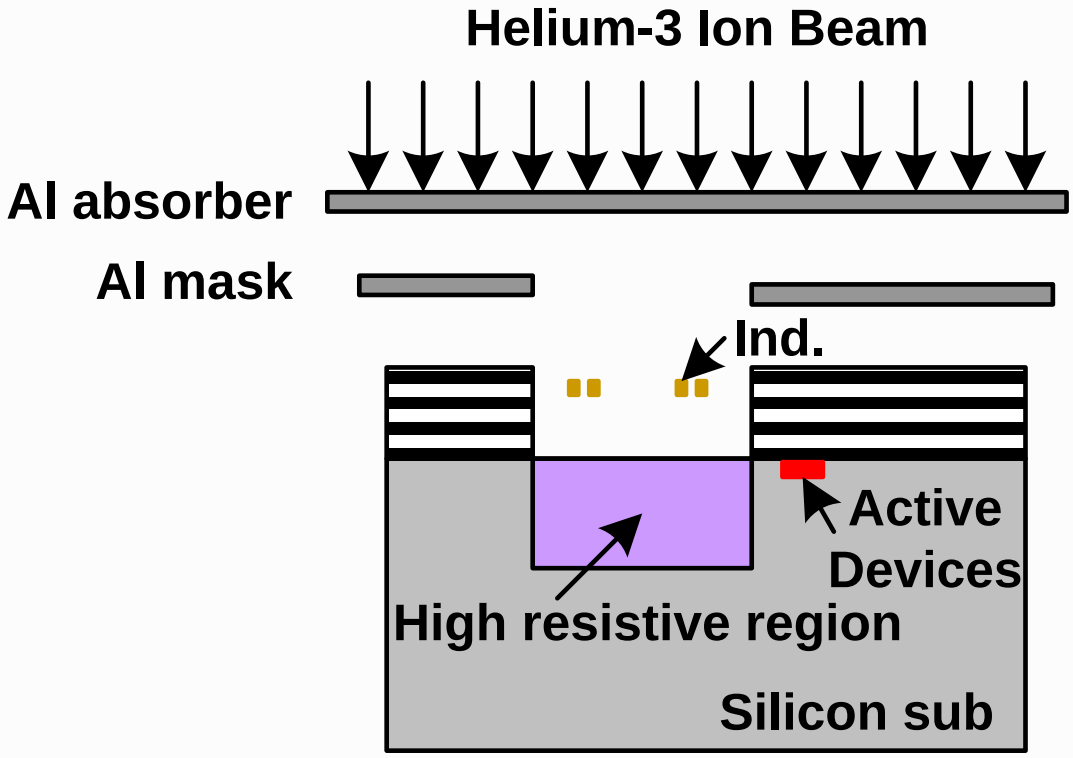
Reference: [1], J. R. long, et al., JSSC 1997. [2], C. C. Liu, et al., IEDM 2012. [3], J. H. Kim, et al., RFIC 2003. [4], L. S. Lee, et al., TED 2001.

Helium-3 Bombardment

- Improving substrate resistivity
- 500-μm Al mask is used to protect active devices.



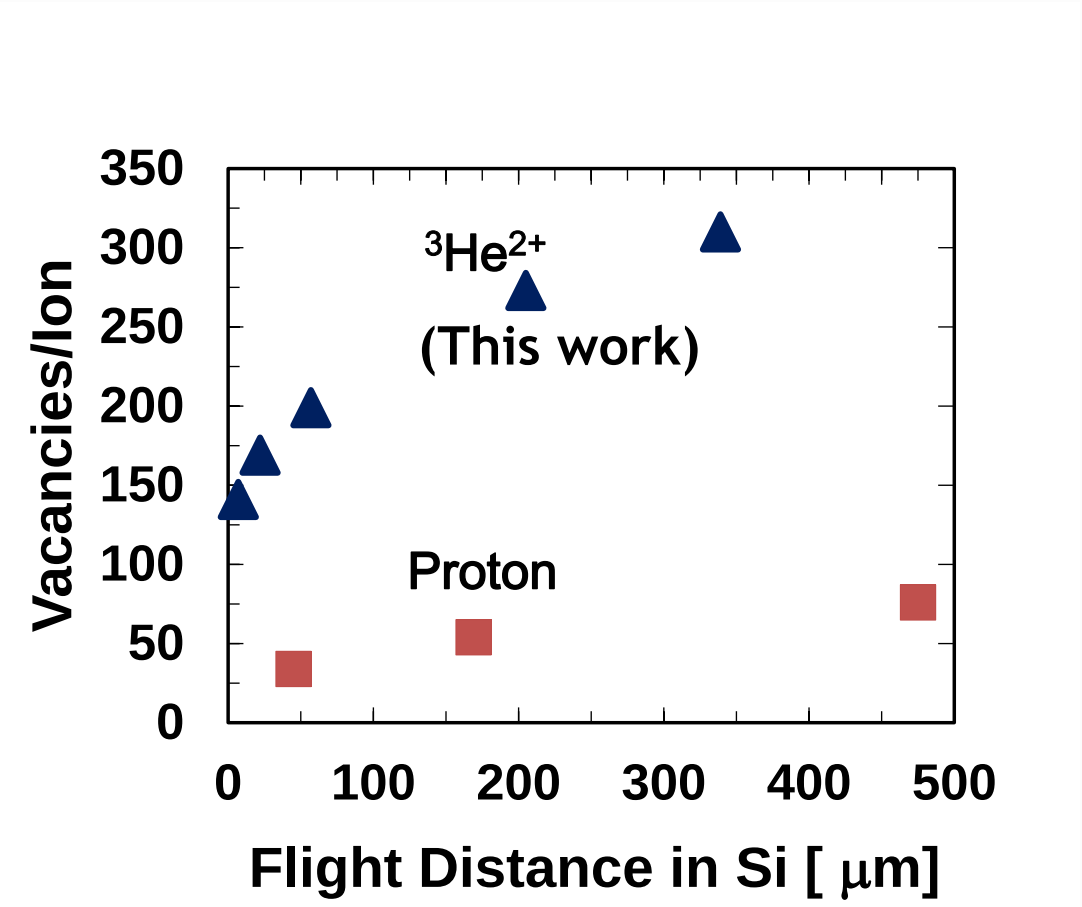
Top view



Cross view

Helium-3 Bombardment (Cont'd)

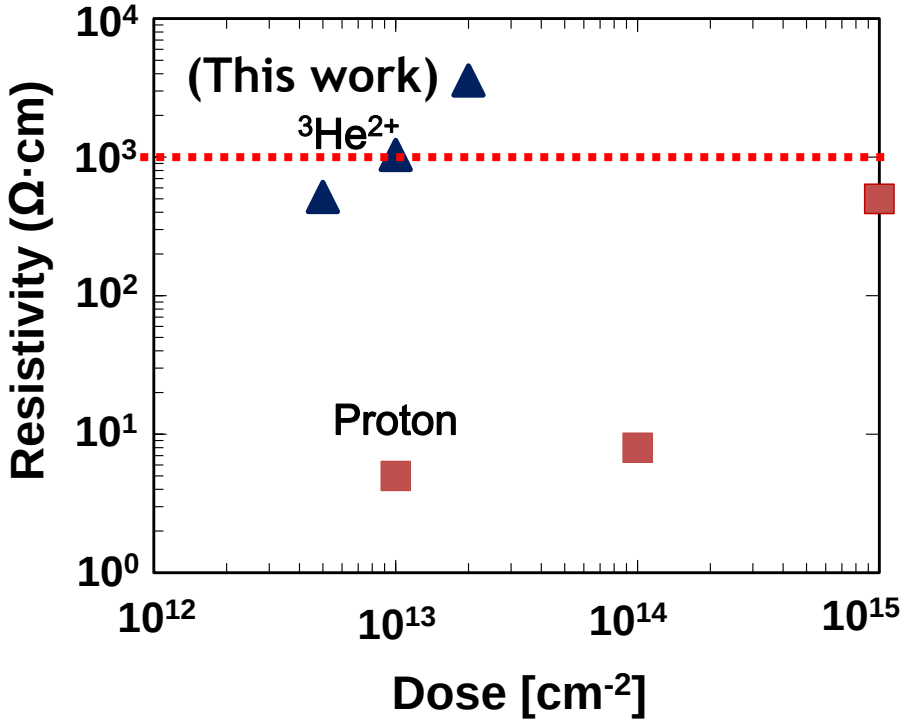
- Larger vacancy generation per ion at the same flight distance in silicon
- Vacancies/ion of Helium-3 is more than 5~6 times larger than that of proton



Calculated by Transport of ions in matter (TRIM) of a software named Stopping and Range of Ion in Matter (SRIM)

Helium-3 Bombardment (Cont'd)

- Small dose amount
  - For R_{sub}>1kΩ, about $10^{13}cm^{-2}$
- lower cost
  - 10^{13}-cm^{-2} dose amount needs only 3.7min



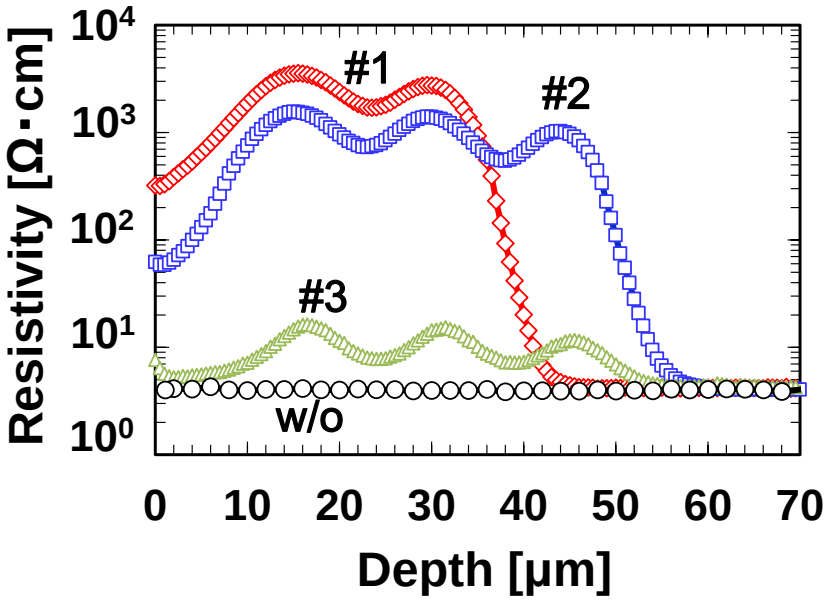
CZ-N wafer
Boron dopant
$1x10^{15}$ atms/cm^3

Reference: L. S. Lee, et al., TED, 2001

Substrate Resistivity Profile

- Spreading resistance profiler (SRP) method
- Large dose amount, higher substrate resistivity
- Peaks are correspond to implantation times and depth.
- About $10^{13}cm^{-2}$ dosing twice realizes a 30-μm high resistivity region above 1kΩ. (red line)

Cond.	Total time [s]	Target irradiation depth [mm]	Total dose [cm^{-2}]
#1	444	15, 30	2.0 x10^{13}
#2	332	15, 30, 45	1.5 x10^{13}
#3	66	15, 30, 45	3.0 x10^{12}



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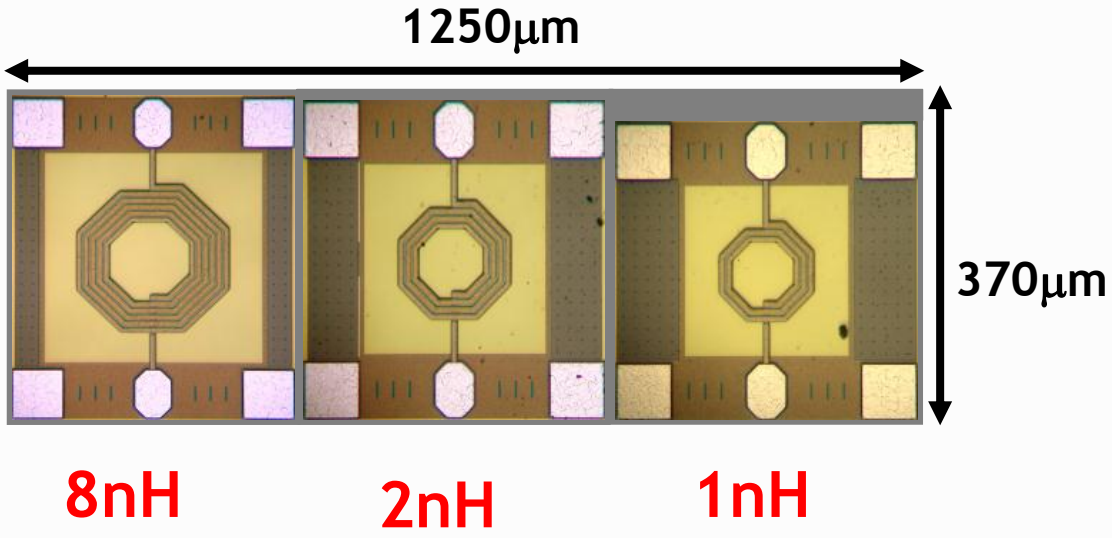
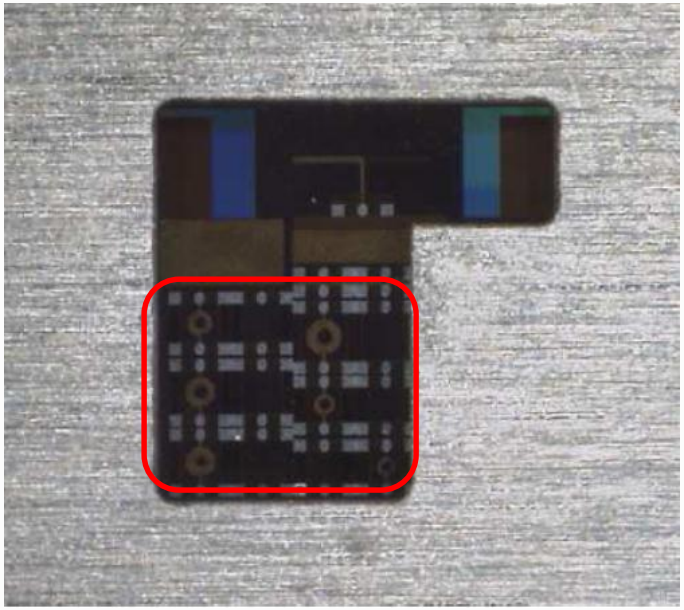
Inductor Implementation

- 180-nm CMOS process
- 6 metal layers
- Measured s-parameter
- Open de-embedding



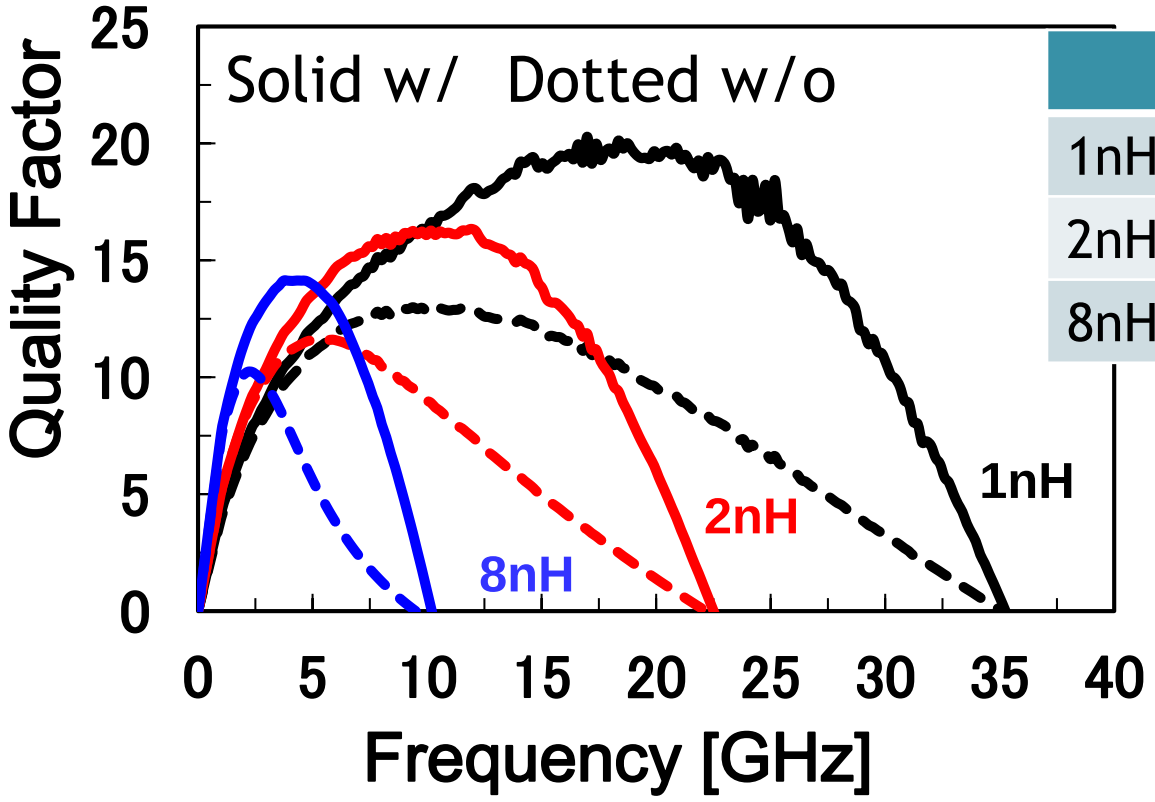
Chip photo



Chip and mask

Inductor Implementation Results

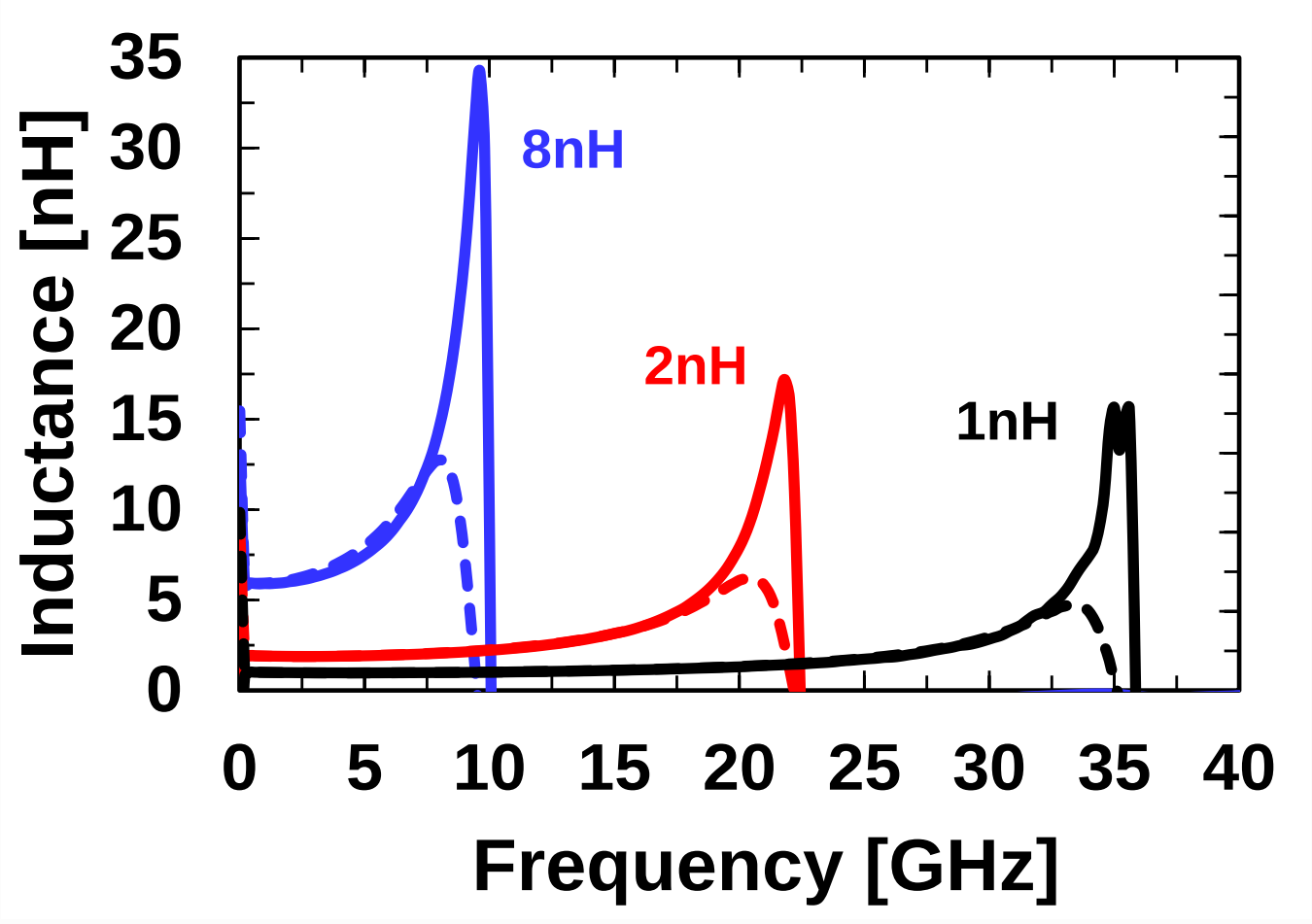
- Q improvement ratios (IR) are 54% for 1-nH inductor.
- Peak frequencies shift to higher while self-resonance frequencies not changed.



	Q(w/o)	Q(w/)	IR(%)
1nH	13.0	20	54%
2nH	11.6	16.3	38%
8nH	10.3	14.1	36%

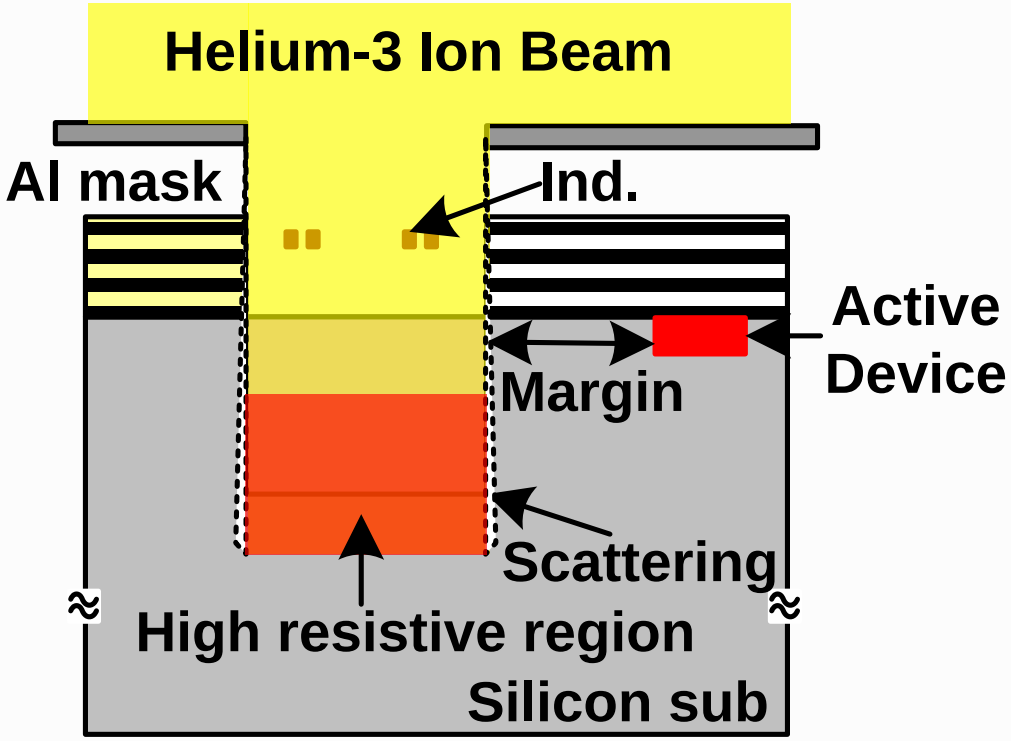
Inductor Implementation Results (Cont'd)

- Inductance only has slight change.



Reliability Test

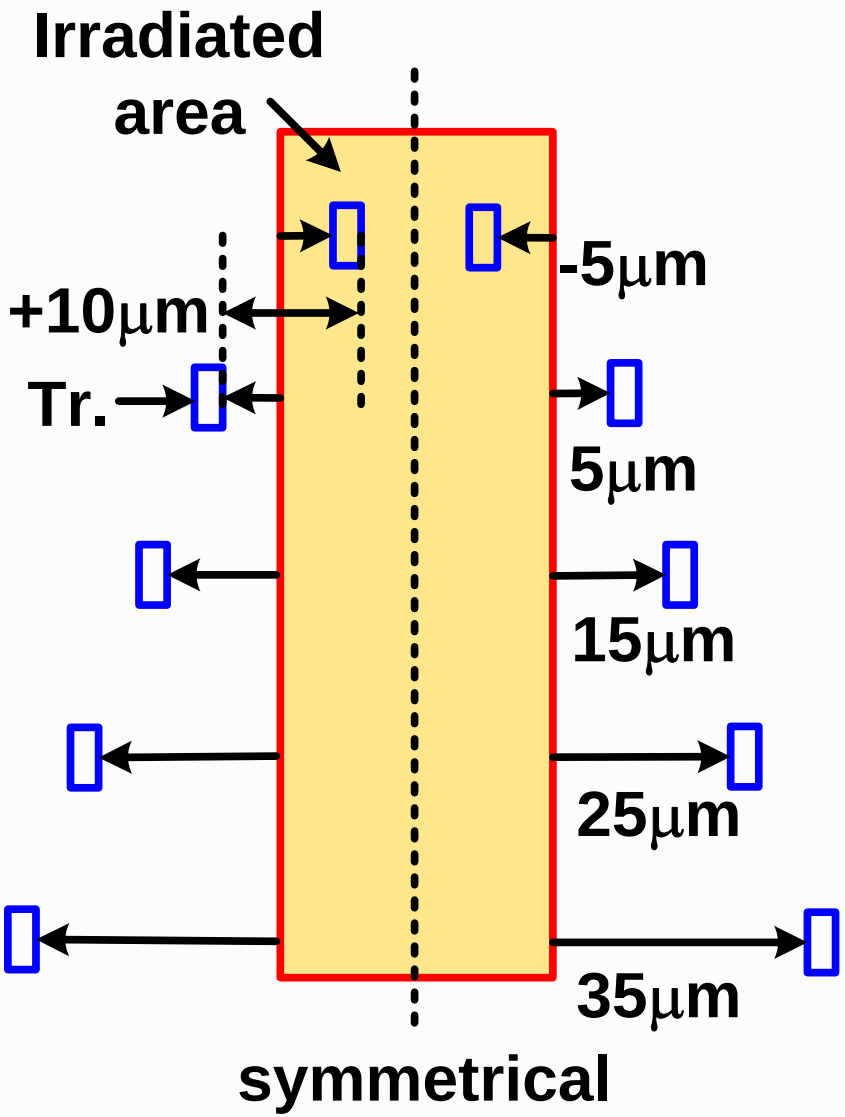
- Ion scattering and mask alignment error
- Reliability criteria of active devices



Cross section

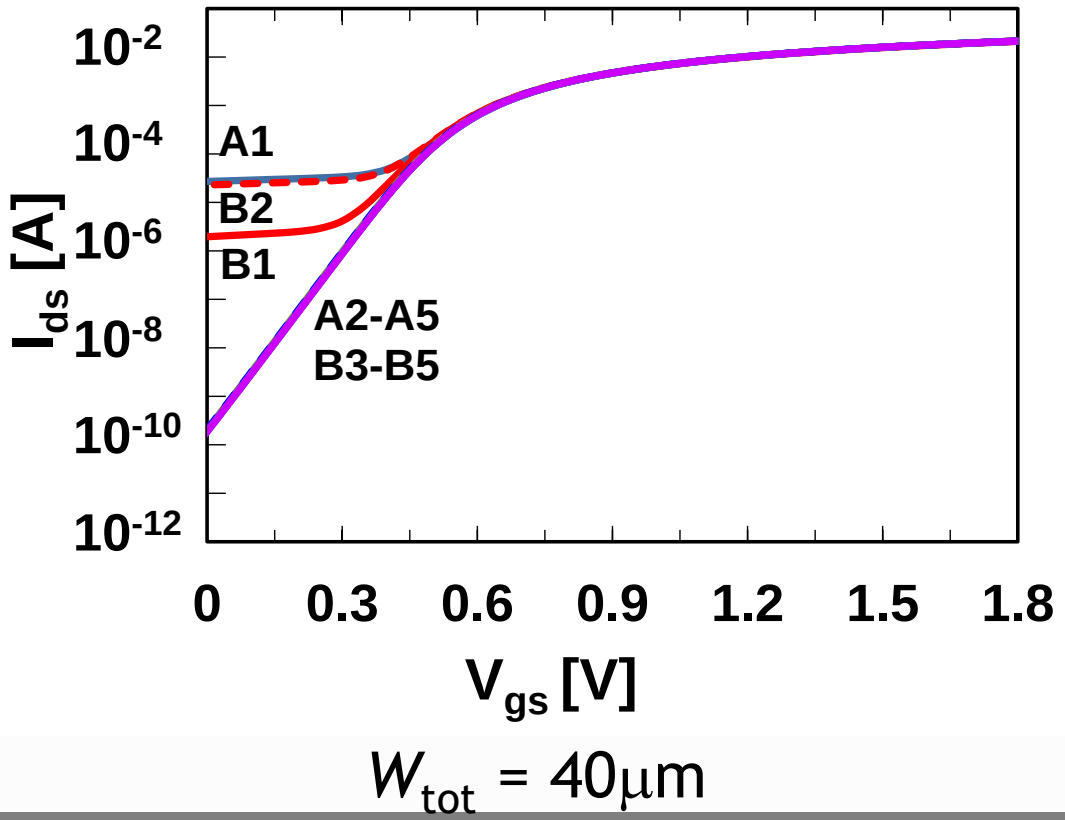
Reliability Test Structure

- Implemented in the same chip with inductors
- Symmetric transistor array
- 10-μm pitch
- The irradiated area covered the first two transistors
- Measuring leakage current

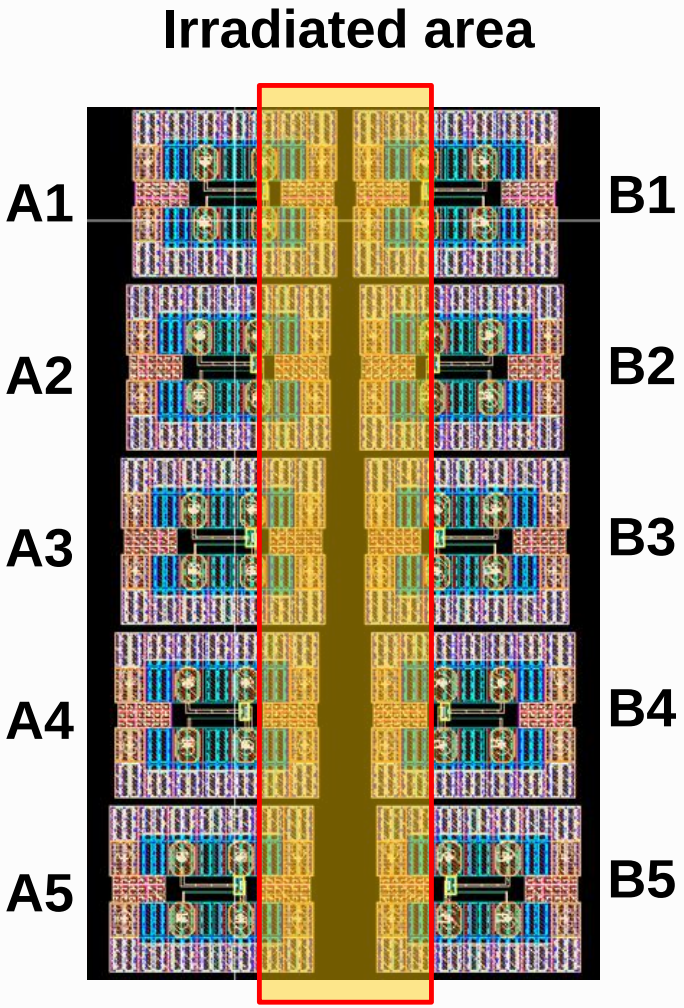


Measured Leakage Current

- DC measurement
- I-V_{gs} curve are showed.

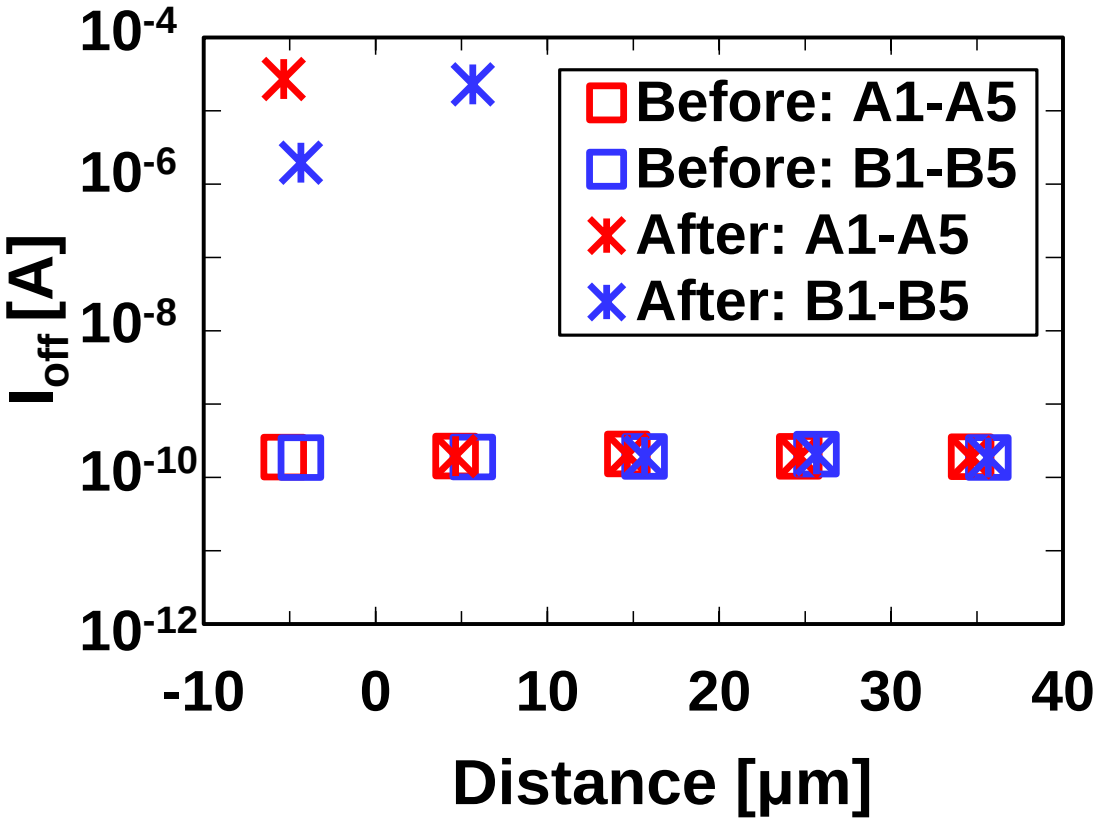


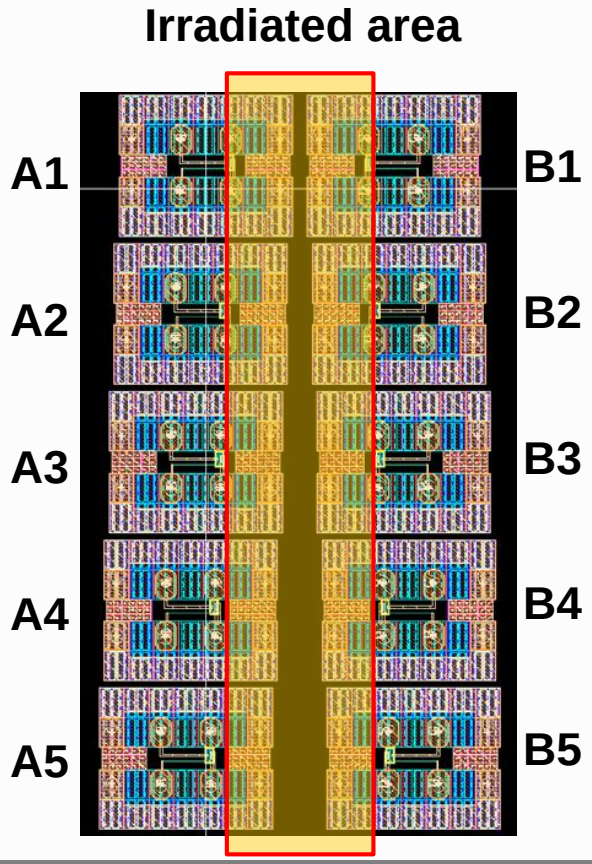
W_{tot} = 40μm



Measured Leakage Current (Cont'd)

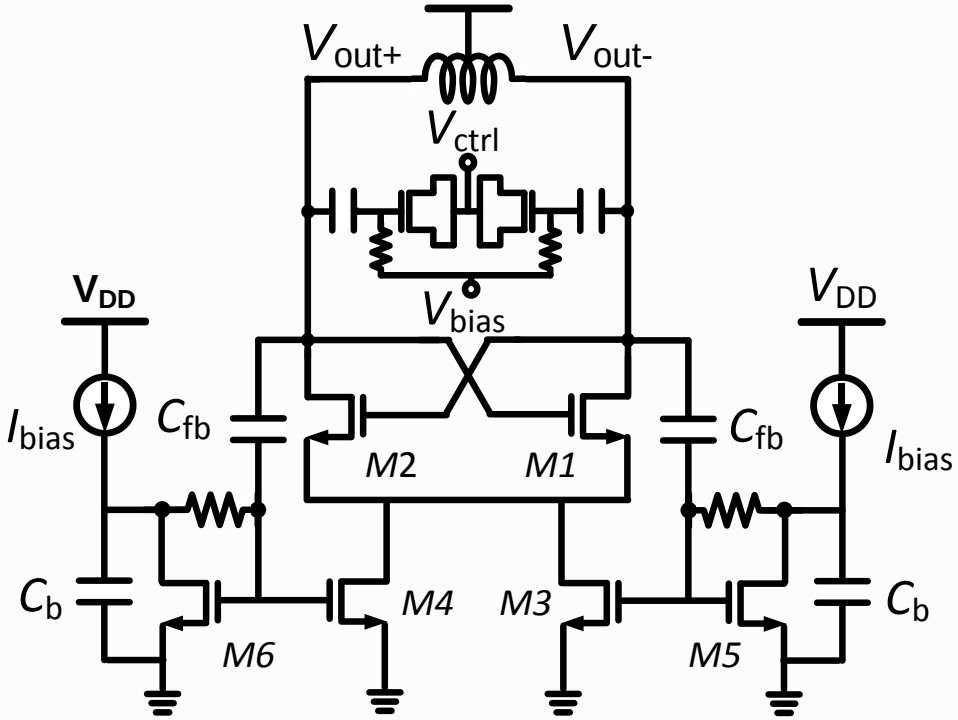
- Leakage current at V_{gs} equal to 0V
- Leakage current with distance from the mask edge
- 15μm required margin including mask alignment.



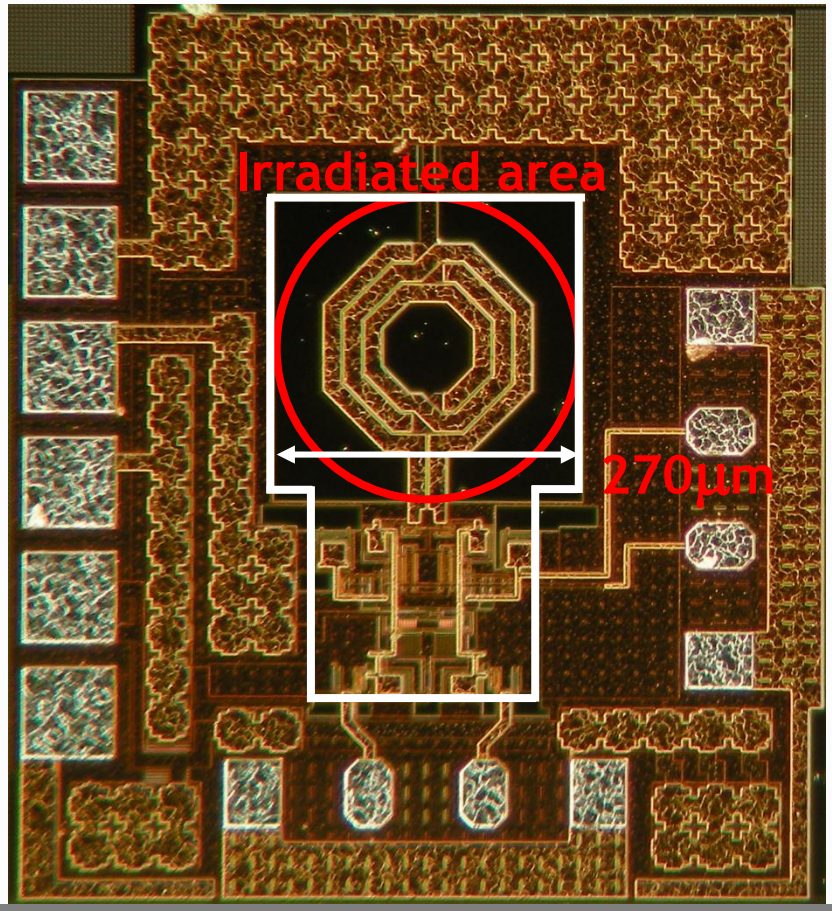


VCO Design

- 8-GHz oscillation frequency
- 180-nm CMOS process
- 6 metal layers

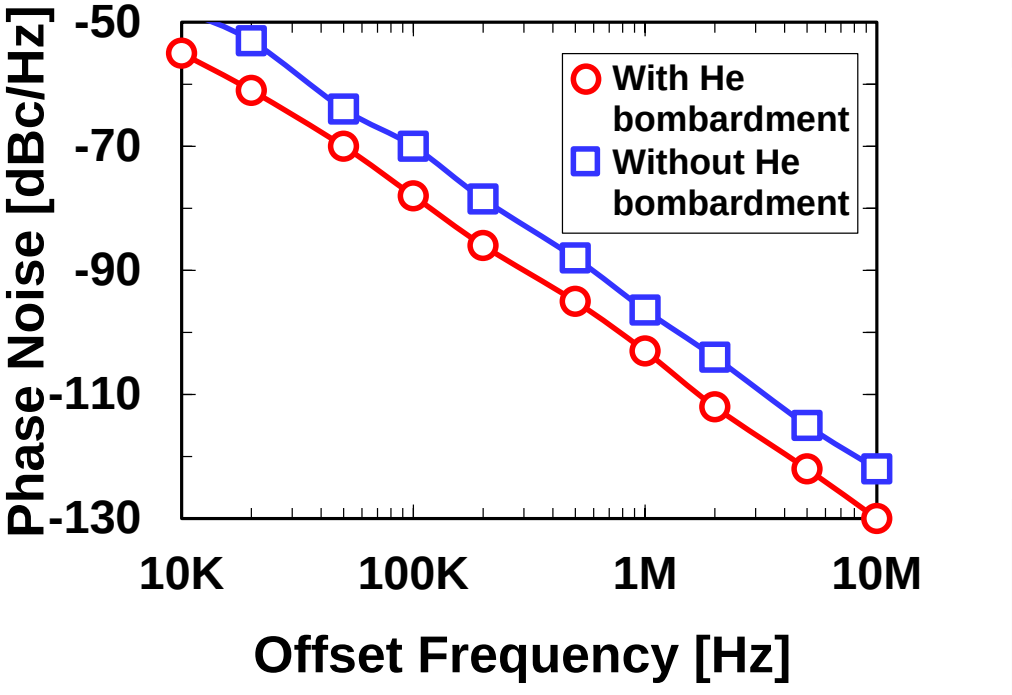


Core area: 0.13mm^2



Performance Summary

- 8.5dB improvement at almost the same power
- Power consumption decreasing 73%



	w/o ion	w/ ion
VDD (V)	1	1
P_DC (mW)	4.83	4.75
PN (dBc/Hz)	-94	-102.5
f_osc (MHz)	8027	8044

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Conclusions

- Helium-3 bombardment is proposed to create a local semi-insulated substrate of high resistibility.
- Required dose amount is about $1.0 \times 10^{13} cm^{-2}$, 100 times smaller than the conventional proton bombardment
- Q can be improved by 58% for a 1-nH Inductor.
- 15-μm placement margin from mask edge is required.
- 8.5-dB phase-noise improvement in the 8-GHz oscillator, 73% power reduction.

Acknowledgements

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