A Characterization Method of On-Chip Tee-Junction for Millimeter-Wave CMOS Circuit Design

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Abstract

A characterization method for an on-chip tee-junction is presented using two different structures. The model results show good agreement with the measurement results of verification structure from 1 to 110 GHz. This tee-junction model is further evaluated using one-stage millimeter-wave amplifier. Comparison of model and measurement results shows good agreement from 1 to 110 GHz in terms of input return loss and gain of the amplifier.

1. Introduction

The unlicensed band around 60 GHz attracts applications for high-data-rate communications. Moreover, CMOS offers the advantages of cost, and monolithic implementation for high-data-rate transceiver (TRX) systems [1]. In order to successfully implement these systems, one has to have accurate device models, beforehand. The characterization approaches for devices having two-ports, or more number of ports differ, starting from the measurement, calibration and de-embedding procedures. These phases are relatively easy for two-port measurements compared to more number of port measurements, e.g. four-port, and hence device characterizations are much more accurate [2]. Considering these issues, a simple characterization approach for an on-chip tee-junction, using two structures is developed and presented in this work.

2. Structures and Method

The illustration of tee-junction is given in Fig. 1. The structure used for tee-junction characterization is presented in Fig. 2(a). The tee-junction is connected with 90 μm TLs to probing pads at ports 1 and 2. The probing pads, and TLs are characterized using L-2L (virtual-thru) de-embedding method [3]. L-2L de-embedding method is chosen, because of its accuracy on TL and pad characterization compared to several other methods [4]. The assumed tee-junction model is represented in Fig. 2(b). Tee-junction ports 1 and 2 are assumed to be symmetric. In order to characterize tee-junction, the pads and 96 μm TL is de-embedded from both measurement ports as illustrated in Fig. 2(a), i.e. the reference ports are moved to vertical red dotted lines in Fig. 2(b). Extra TLs are de-embedded so that the remaining part of the tee-junction can be assumed as lumped constant, and calculations can be done assuming lumped constant "Z_1". Then de-embedded two-port S-parameters are converted to Z-parameters. Z_{11}- Z_{12} directly gives "Z_1" model parameter in Fig. 2(b). The port 3 of Tee-junction (Fig. 1) is terminated with 2.5 μm short-circuited TL, as shown in Fig. 2(a). Z_{12} is equal to series connection of model parameter "Z_2" and impedance of 8 μm short-circuited TL named as Z_{short} in Fig. 2(b). Again, this extra 5.5 μm TL is considered in Z_{short} for "Z_2" to be assumed as lumped constant. Hence, "Z_2" can be calculated as Z_{12}-Z_{short}. The extra de-embedded TL length (6 μm), and extra length (5.5 μm) calculated in Z_{short} are adjusted so that the model and measurement results of Fig. 2(c) have minimum possible difference.

3. Results and Evaluation with One-Stage Amplifier

The structures of Fig. 2(a), and (c) are fabricated using 65 nm CMOS process. The chip micrographs of these two structures can be found in Fig. 3. Using model and TL models, structure is reconstructed (Fig. 2(a)) and compared with measurement results from 1 to 110 GHz. Fig. 4(a) represents the input return losses (RL), and Fig. 4(b) represents the insertion losses (IL) for model and measurement results. They coincide perfectly. In order to verify the models, measurement results of Fig. 2(c) are compared in terms of input RL in Fig. 5(a) and in terms of IL in Fig. 5(b). The models are well matched in the entire frequency band. In order to further evaluate the tee-junction model, a manufactured and measured one-stage amplifier results are compared with simulation results using models. The schematic of the amplifier is presented in Fig. 6(a). In this amplifier three tee-junctions are used. The chip micrograph of the amplifier is provided in Fig. 6(b). Fig. 7(a) compares the input RL from 1 to 110 GHz; Fig. 7(b) compares the output RL from 1 to 110 GHz, Fig. 7(c) compares the gain from 1 to 110 GHz, and Fig. 7(d) compares the gain from 40 to 70 GHz for model and measurements when the gate bias is 0.8 V. Input RL is well matched in the entire frequency band; however, there is difference after around 80 GHz. The gain is also well matched. On the other hand, output RL comparison shows more difference, which is mainly because of decoupling TL modeling error.

4. Conclusion

In this work, an approach to characterize tee-junction is presented. The calculation of model parameters is done using Z-parameters. The TL lengths of the tee-junction model are adjusted such that verification structure measurement results have the least difference between model results. To further evaluate the model, measurement and model results of one-stage amplifier are compared. Input RL of the models is very similar to measurement results. The gain comparison shows good agreement.

Acknowledgements

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References

[1] K. Okada, *et al., ISSCC*, 2014 p.346
[2] K. K. Tokgoz, *et al., SSDM,* 2013, p.900
[3] N. Li, *et al., IEICE,* 2010, p.431
[4] R. Minami, *et al., EuMC,* 2011, p.381

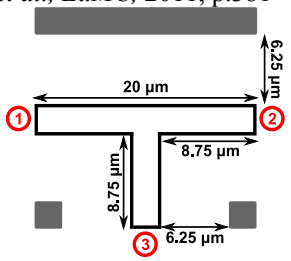


Fig. 1. Geometrical specifications and port assignment for Tee-junction (gray areas represent ground planes).

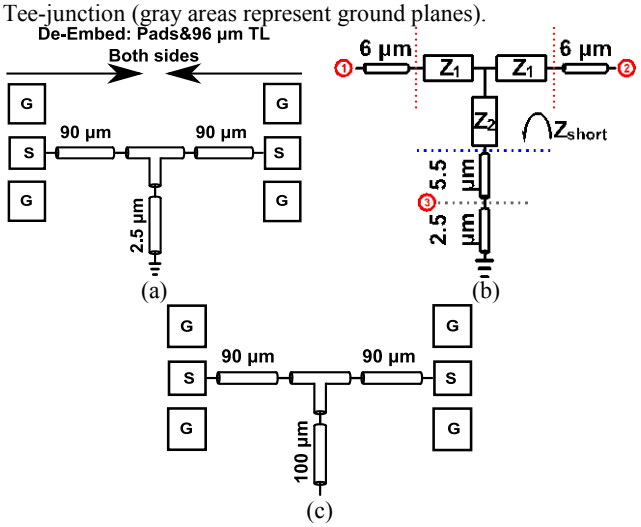
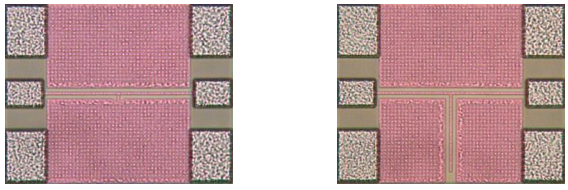
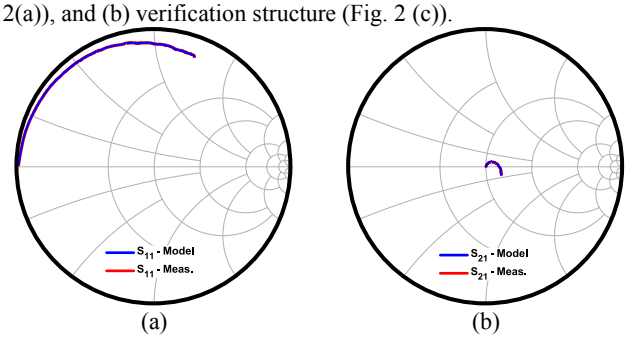


Fig. 2. Illustration of (a) manufactured structure for characterization, (b) characterization model for tee-junction, and (c) structure used for model verification.



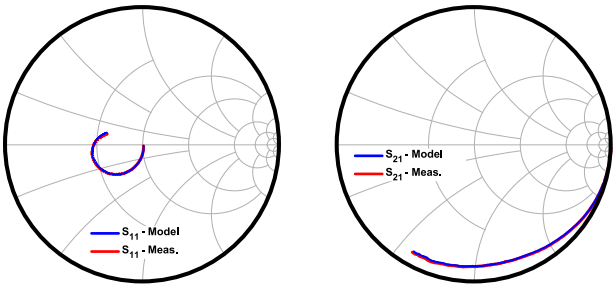
(a) (b)

Fig. 3. Chip micrograph of (a) characterization structure (Fig. 2(a)), and (b) verification structure (Fig. 2 (c)).



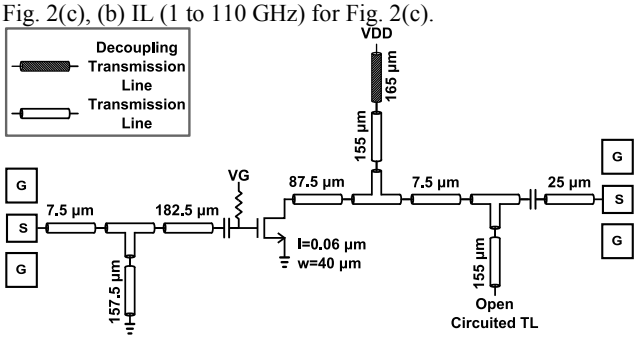
(a) (b)

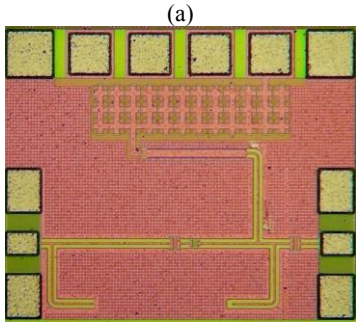
Fig. 4. S-parameter comparison between measurements (red lines) and models (blue lines); (a) input RL (1 to 110 GHz) for Fig. 2(a), (b) IL (1 to 110 GHz) for Fig. 2(a)



(a) (b)

Fig. 5. S-parameter comparison between measurements (red lines) and models (blue lines); (a) input RL (1 to 110 GHz) for Fig. 2(c), (b) IL (1 to 110 GHz) for Fig. 2(c).





(b)

Fig. 6. One-stage amplifier (a) schematic, and (b) chip micrograph

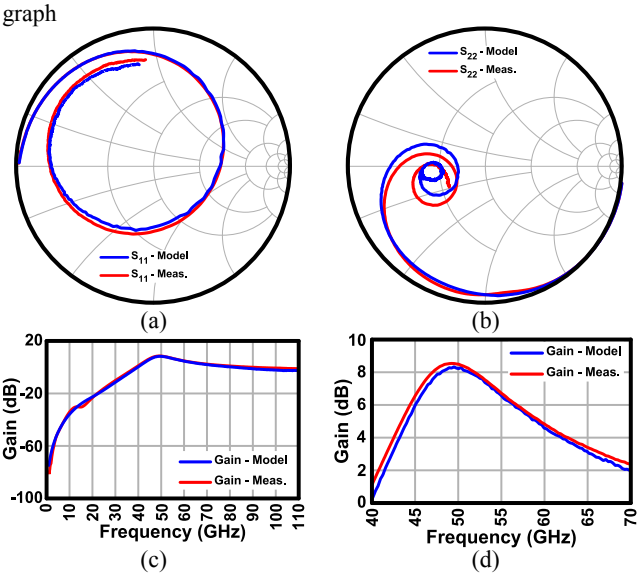


Fig. 7. S-parameter comparison between measurements (red lines) and models (blue lines); (a) input RL of amplifier (1 to 110 GHz), (b) output RL of amplifier (1 to 110 GHz), (c) gain of amplifier (1 to 110 GHz), and (d) gain of amplifier (40 to 70 GHz).