A 0.8 ps-LSB, 10-bit, 0.018 mm^2 Time-to-Digital Converter

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Abstract

A time-to-digital converter, using a charge pump to translate time interval into charge and a SAR-ADC quantizing the charge, can achieve sub-picosecond resolution. To improve the linearity and area occupation, we propose a sampling method and a layout pattern for the capacitive DAC in the SAR-ADC. The prototype chip was fabricated in 65nm CMOS. The measured DNL and INL are -0.6/0.8 ps and -2.56/2.48 ps, respectively, with the resolution of 0.8 ps, and the range of 10-bit. The measured single-shot-precision is 0.6 ps. The power consumption is 2.9 mW at the conversion rate of 50 MS/s, and the core area is 0.018 mm^2.

1. Introduction

A TDC intended to low-noise digital PLLs has to meet with stringent specifications of resolution, linear range, power, and area. Since the resolution of the TDC dominates the in-band phase noise to the PLL, various architectures have been proposed [1]-[3] to break the resolution limitation in the delay-chain TDC. However, a high resolution TDC meeting with the other aforementioned specifications remains challenge to design. Time-to-charge conversion followed by a SAR-ADC has been proved to be potential to overcome this challenge [4] [5]. This work describes an improved design to [4] achieving larger linear range and smaller area.

2. Circuit Design

The architecture of the presented TDC is shown in Fig. 1. A charge pump followed by a PFD that translates time interval into charge. The charge is accumulated on the CDAC which performs sample-and-hold for the SAR-ADC. The architecture is compact and easily achieves sub-picosecond resolution due to the equation: $t_{res} = CV_{lsb}/I$, where t_{res}, CV_{lsb}, and I represent the time resolution, the minimum resolvable charge, and the charging current, respectively. This architecture has been verified in [4], but its linear range and area occupation limit its employment in a PLL. To improve the linear range, a sampling method is proposed. To minimize the area, the CDAC is designed with proposed capacitor-switch unit, where gaps in between each unit are eliminated. The two proposals are elaborated in the following paragraphs.

In the proposed TDC, charge injections degrade the linearity when turning off UP and DN switches. Conventionally, they are turned off after a certain delay when both UP and DN signals are high. We insert a bottom-plate-sampling timing sequence into the reset path of the PFD to mitigate the charge injection, as shown in Fig. 2. Before the rising edge of UP or DN, switch RST is on resetting the output of the charge pump. When CK_1 or CK_2 is high, RST is turned off earlier than UP or DN. After both UP and DN are high, S_0, S_1, and S_2 are sequentially turned off, performing a bottom-plate sampling. Then, CLR_{pfd} also shown in Fig. 1 is generated to pull down UP and DN. When S_2 is turned off, both plates of the CDACs are float so that charge injections from UP and DN switches are mitigated.

A CDAC generally takes large area due to the gaps in between its components and interconnections. To minimize the area, a layout pattern is proposed. Fig. 3 shows a 2-bit example. A unit capacitor and a unit switch are laid out with same pitches. When the unit is combined with others, the drain (or source) regions of the switches and the top plate of the capacitor merge with its adjacent units. Thus, the gaps in between the units are eliminated. The reference lines of V_{refp} and V_{refn} can be drawn upon the switches, saving the interconnection area. Since the bottom plate of the capacitors are not necessarily connected, the placement of units can be scrambled or common-centroid, as shown in Fig. 3, to reduce the effect of process variations.

3. Experimental Results

The prototype chip was fabricated in 65nm CMOS. Two 50 MHz pulses with 50 Hz frequency difference are used as the inputs to the TDC. The two signals generate a series of time interval ramps. Using histogram method, a DNL of -0.6/0.8 ps and INL of -2.56/2.48 ps are measured, as shown in Fig. 4, where 1 LSB equals 0.8 ps and the output range is 10-bit. To measure the single-shot precision, one pulse is split into two which are fed to the TDC. The standard deviation indicates a 0.64 ps single-shot precision, as shown in Fig. 5. The power consumption is 2.9 mW, and the area is 0.018 mm^2. This performance is compared in Table I with the state-of-art TDCs. The presented TDC achieves the finest resolution and the smallest area. Its chip photo and layout is shown in Fig. 6.

4. Conclusion

We have presented a sub-picosecond resolution TDC using a charge pump and a 10-bit SAR-ADC. A sampling method is proposed so as to enlarge the linear range. A small-area CDAC in the SAR-ADC is designed with the proposed capacitor-switch unit, eliminating the gaps in be-

tween the units and reducing the interconnection area. The proposed TDC also features low power, small area, and sufficient range, which makes it suitable for digital PLLs.

Acknowledgements

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References

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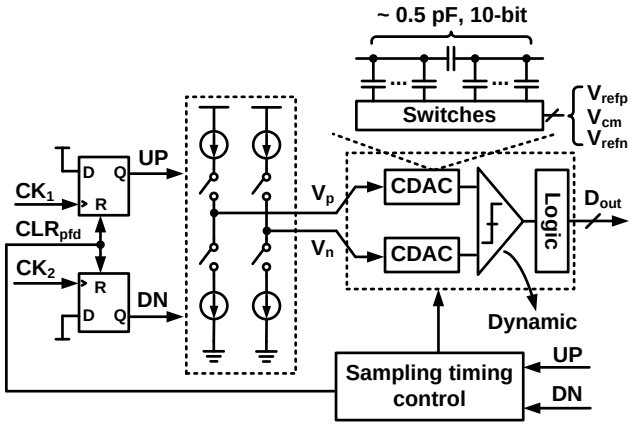

Fig. 1. Sub-picoseoncd resolution TDC using charge pump and SAR-ADC.

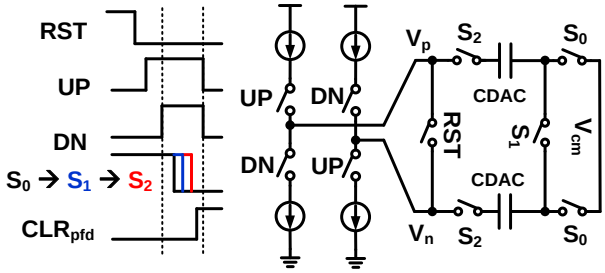

Fig. 2. Proposed sampling method to mitigte charge injection.

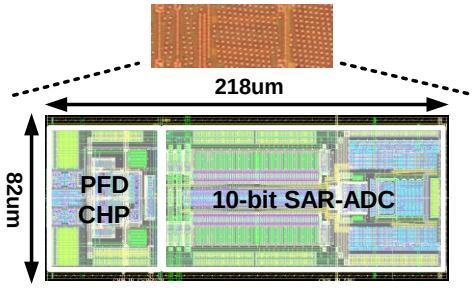

Fig. 6. Chip photo and layout.

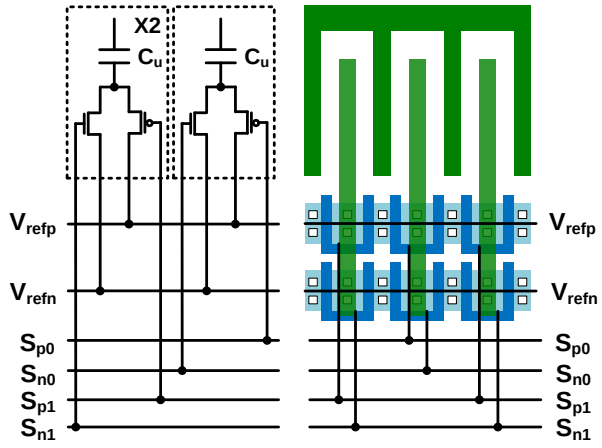

Fig. 3. Proposed layout pattern for the CDAC. A 2-bit example is shown, where capacitor-switch units are merged without gaps in between. The switches for V_{cm} are not shown for conciseness.

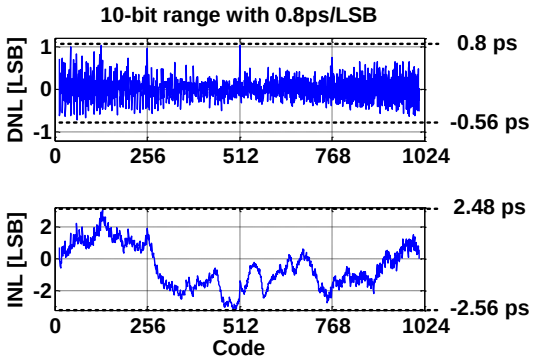

Fig. 4. Measured DNL, INL, resolution, and range.

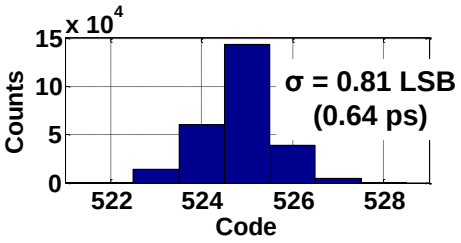

Fig. 5. Measured single-shot precision.

TABLE I. PERFORMANCE COMPARISON

	[1]	[2]	[3]	[4]	This
Type	Pipeline	Noise shaping	Stochastic	Charge	Charge
CMOS [nm]	65	130	65	65	65
Supply [V]	1.2	1.2	1.2	1.0	1.2
t_{res}[ps]	1.12	3.0	3.0	0.84	**0.80**
Range [bits]	9	11	4	8	10
DNL [LSB]	0.6	-	-	-0.7/1.0	-0.7/1.0
INL [LSB]	1.7	-	-	-2.7/1.7	-3.2/3.1
Rate [MS/s]	250	5.62	40	40	50
Power [mW]	15.4	3.2	8.0	2.47	2.9
Area [mm^2]	0.14	0.43	0.04	0.06	**0.018**