A Varactor-Less and Dither-Less LC-Digitally Controlled Oscillator with 9-bit Fine Bank, 0.26 mm^2 Area, and 6.7 kHz Frequency Resolution

Zule Xu, Mitsutoshi Sugawara, Kenji Mori, Masaya Miyahara, and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1 S3-27, Ookayama, Meguro-ku, Tokyo, 152-8552, Japan
Phone: +81-3-5734-3764 Email: xuzule@ssc.pe.titech.ac.jp

Abstract

We present a compact LC-digitally controlled oscillator (DCO). Its coarse and fine capacitor banks are both implemented using switched metal-oxide-metal capacitors, instead of varactors. We propose an architecture achieving high resolution without introducing ΔΣ-dithering noise, and a layout pattern minimizing the area. Fabricated in 65 nm CMOS, the DCO with 9-bit fine bank achieves 6.7 kHz frequency resolution, and occupies 0.26 mm^2 area. The measured phase noise at 3.3 GHz is -120.7 dBc/Hz@1MHz. The power consumption is 4.8 mW with 1.2 V power supply.

1. Introduction

All-digital phase-locked loop (ADPLL) has been gaining its popularity due to its small area and flexible configuration. A low-noise high-resolution LC-DCO is critical to the ADPLL's phase noise performance. Conventionally, the discrete frequency is realized by discrete varators featuring high capacitive density [1]-[3]. The varactor, however, is sensitive to temperature variation and supply noise from the digital-to-analog converter (DAC) shown in Fig. 1 (a), or the driving inverter shown in Fig. 1 (b). On the other hand, a switched metal-oxide-metal (MOM) capacitor shown in Fig. 1(c) is more immune to these influences. Whatever types of capacitors, the minimum capacitance is limited due to fabrication, matching, and layout complexity difficulties. Thus, the number of bits in fine bank is restricted [4], and ΔΣ-dithering is typically used for finer resolution with the penalty of high frequency noise. Addressing these issues, we propose a varator-less and dither-less DCO with 9-bit fine bank and 6.7 kHz frequency resolution.

2. Proposed DCO

An NMOS type of DCO is designed. Its equivalent model with the topology of capacitor banks is shown in Fig. 2. The coarse and fine banks are interfaced with a bridging capacitor, C_s. Sizing C_s and C_a can attenuate the gain of the fine bank so that larger unit capacitor which is helpful for matching can be used in the fine bank. The coarse and fine banks are same (though unnecessarily) with 9-bit, where two MSBs are actually thermometer coded. Two banks do not have to match with each other since the loop filter in an ADPLL tune them separately. The topology of single-ended capacitor-switch unit is shown in Fig. 3. A pull-up resistor is generally required to prevent the non-fully turn-off of switch M_1. At 3 to 4 GHz carrier frequencies, a 3 fF unit capacitor requires hundreds of kilo-ohm resistance which is area consuming if a poly resistor is implemented. Thus, a transistor in sub-threshold region, M_2, is employed for high resistance. Switch M_3 cuts off the resistor path when M_1 is on to prevent the flowing of dc current.

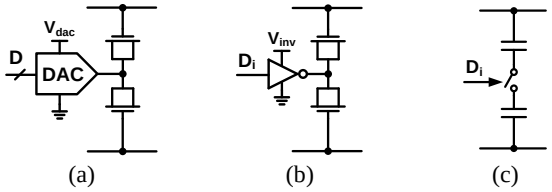

Fig. 1. Three types of discrete capacitance: (a) DAC tuned varactor, (b) varactor operating in two regions, and (c) switched MOM capacitor.

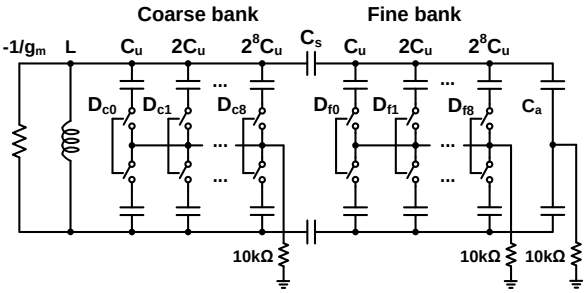

Fig. 2. Equivalenet model of the DCO with the topology of proposed coarse and fine banks.

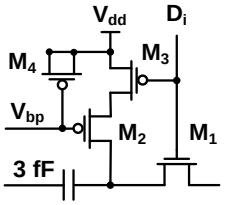

Fig. 3. Proposed capacitor-switch unit.

Higher bits of discrete capacitors are made by duplicating the capacitor-switch units. A layout pattern is proposed to minimize the resulting area occupation and the wire capacitance from interconnections. The proposed layout of the switch-capacitor unit is shown in Fig. 4 (a). Same pitches of the capacitor and transistors are made except for M_2. Fig. 4 (b) illustrates a 2-bit example with dummy units. When combing the units, the common nodes are connected by merging the sources or drains as well as the top plates,

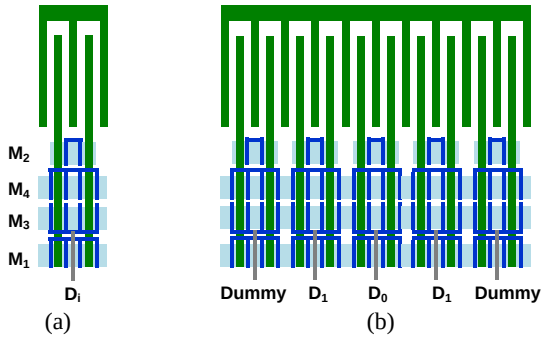

Fig. 4. A 2-bit layout example of the capacitor bank.

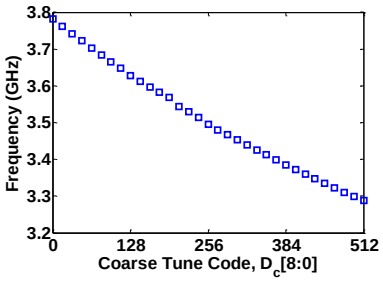

Fig. 5. Measured coarse tune curve.

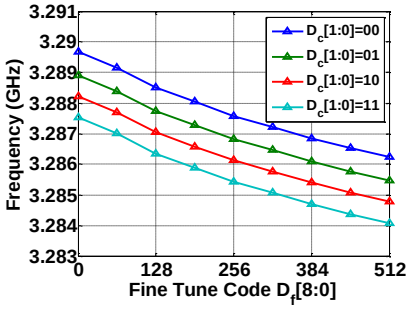

Fig. 6. Measured fine tune curve setting 2 LSBs of coarse bank.

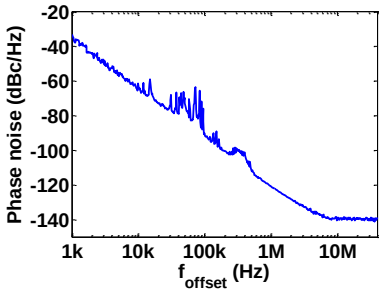

Fig. 7. Measured phase noise.

with their neighboring ones. Therefore, significant area reduction is possible and the layout mismatch is also minimized. The area of two banks is only 0.07 mm^2, differentially containing 5 pF capacitors.

3. Experimental Results

The prototype chip was fabricated in 65 nm CMOS. The measured coarse tune curve is shown in Fig. 5. The coarse tuning range is 500 MHz. The measured fine tune curve at 3.28 GHz is shown in Fig. 6. Four curves are measured setting the 2 LSBs of the coarse bank. Frequency continuity is maintained by the overlaps. The approximate frequency resolution is 6.7 kHz. The measurement of much finer points is limited by the free-running noise of the DCO and instruments. Fig. 7 shows the measured phase noise of -120.7 dBc/Hz@1MHz. The performance is compared with state-of-the-arts in Table I, where the frequency resolution without using DAC or ΔΣ-dithering is used for comparison. Although [4] achieves finest resolution but its number of bits in fine bank is only 4. The proposed DCO achieves the largest number of bits in fine bank and the smallest area. The chip photo is shown in Fig. 8.

Table I Performance Comparison

	[1]	[2]	[3]	[4]	This
CMOS (nm)	65	90	90	65	65
f_{osc} (GHz)	3	3.6	3.3	3.63	3.28
f_{res} (kHz)/bits	4.8/8	12/6	5/5	0.6/4	6.7/**9**
PN@1MHz (dBc/Hz)	-127.5	-126	-118	-131	-120.7
Supply (V)	1.8	1.4	1.2	2.8	1.2
Power (mW)	29	25.2	2.4	56.7	4.8
FoM (dBc/Hz)	-183	-183	-185	-185	-184
FoM_T (dBc/Hz)	-191	-191	-187.5	-194	-187
Cap. type	Var.	Var.	Var.	MOM	MOM
Area (mm^2)	0.32	-	-	0.33	**0.26**

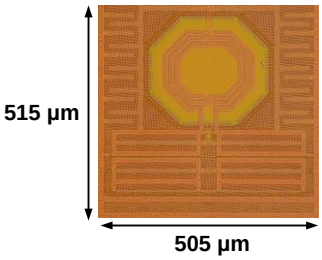

Fig. 8. Chip photo.

4. Conclusion

We have presented a DCO using MOM capacitors for both coarse and fine banks interfaced with bridging capacitors. This topology achieves high resolution without ΔΣ-dithering and large number of bits in fine bank. The proposed layout pattern minimizes the area of the capacitor banks. These techniques make the proposed DCO suitable for a low noise and low-cost ADPLL.

Acknowledgements

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