A 17-mW 5-Gb/s 60-GHz CMOS Transmitter with Efficiency-Enhanced On-Chip Antenna

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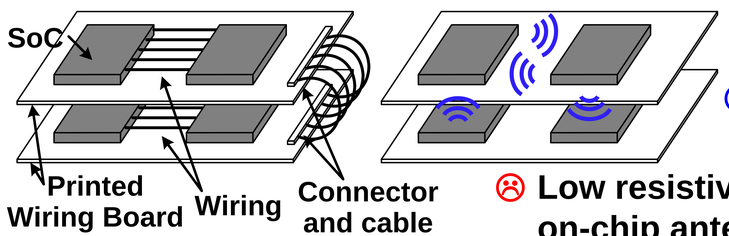
1. Research Background



[1] K. Kawasaki *et al.*, ISSCC2010

mmW Intra-connect in CMOS

☺ Low cost, no parasitic components, and flexible connection

☺ Potential for on-chip antenna and high data rate

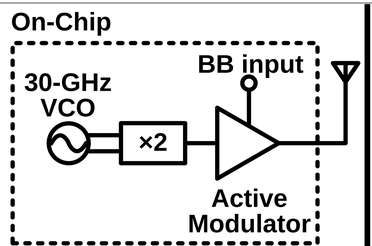
☹ Low resistivity of CMOS substrate ➔ poor on-chip antenna gain

☹ High data rate ➔ requires ultra wideband

2. Conventional CMOS mmW Intra-connect TXs

☺ High data rate

☹ Active modulators and buffers are power hungry

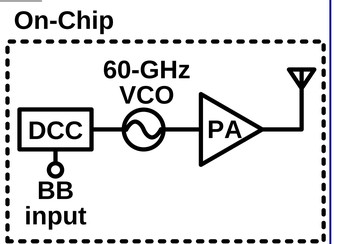


[2] C.W. Byeon *et al.*, TMTT2013

☹ Off-chip antenna increases circuit size and parasitic components

☺ On-chip antenna

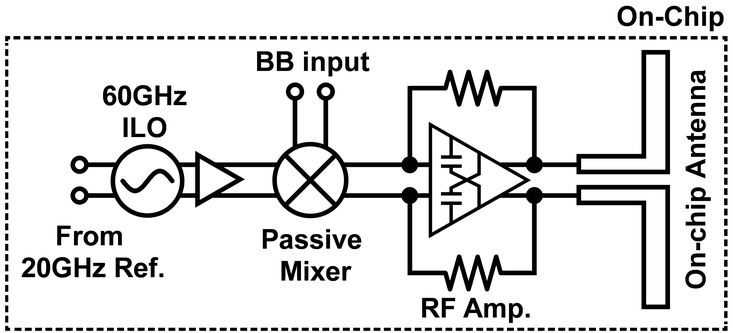
☹ Switched-LO topology limits the data rate (2.2 Gb/s)



[3] A. Siligaris *et al.*, RFIC2013

☹ CMOS SOI process is used to improve on-chip antenna gain

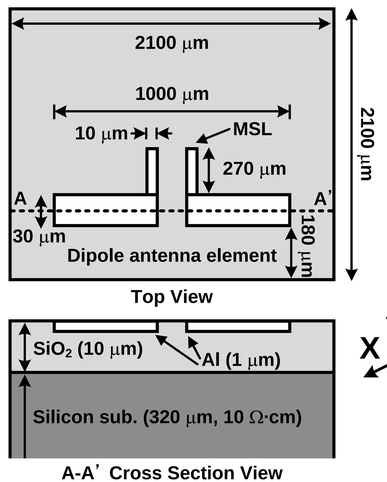
3. The Proposed Transmitter

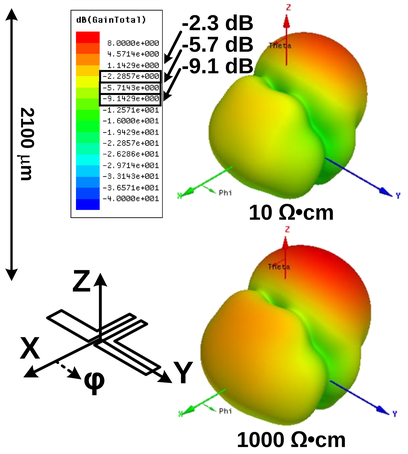


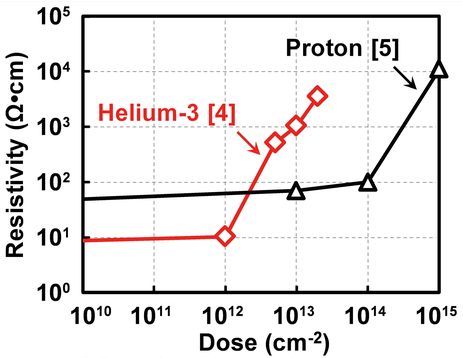
➢ On-chip ante. G_{ante}> -5 dBi (Helium-3 ion implantation)

➢ Data rate = 5 Gb/s
Power=17 mW
(Wideband, power-saving TX core design)

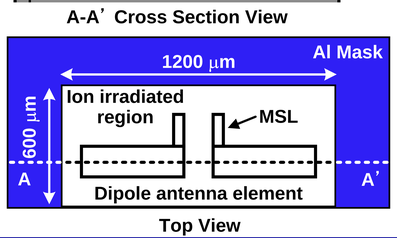
4. 60-GHz CMOS On-Chip Antenna

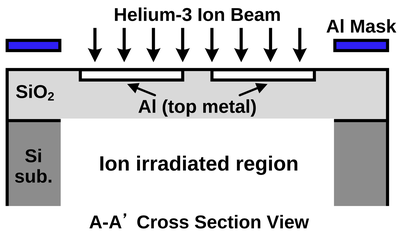


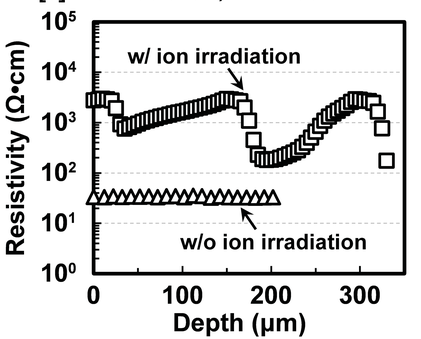




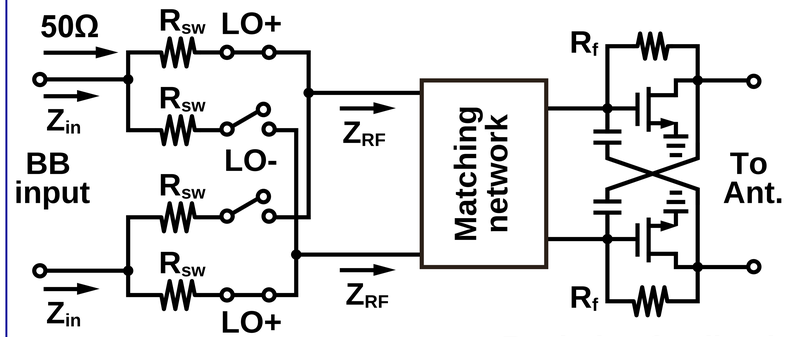
[4] N. Li *et al.*, VLSI2014
[5] L.S. Lee *et al.*, ITED2001





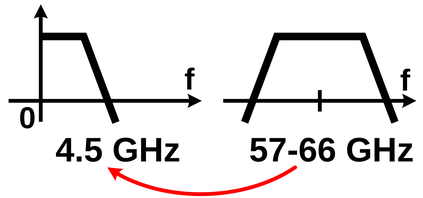


5. RF Front-End Circuit



Double-balanced passive mixer

Resistive-feedback RF amp.

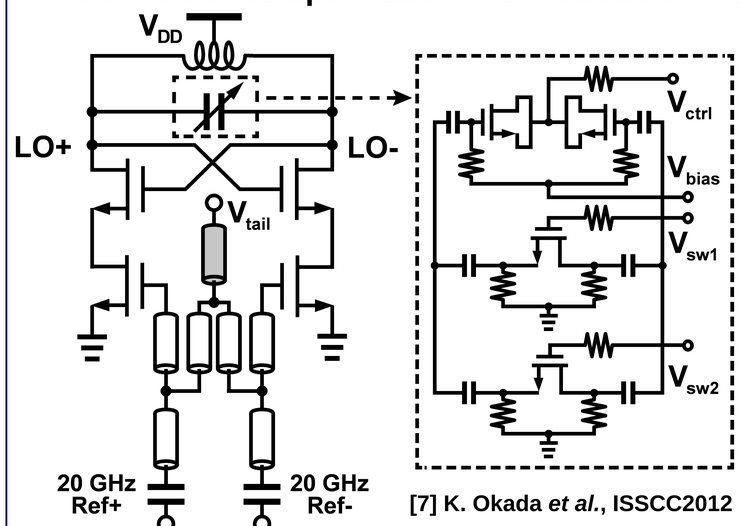


Down-converted even for Z_{RF}

$$Z_{in}(\omega) \approx R_{sw} + \frac{8}{\pi^2}\mathrm{Re}[Z_{RF}(\omega_{LO})]$$

[6] K. Okada *et al.*, ISSCC2014

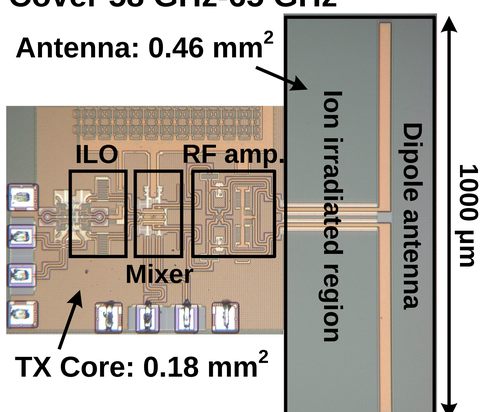
- Resistive-feedback RF amp. ➔ wideband matching@60-GHz band
- Passive mixer ➔ wideband matching@baseband
- Mixer switches optimization ➔ reduce the required LO power



[7] K. Okada *et al.*, ISSCC2012

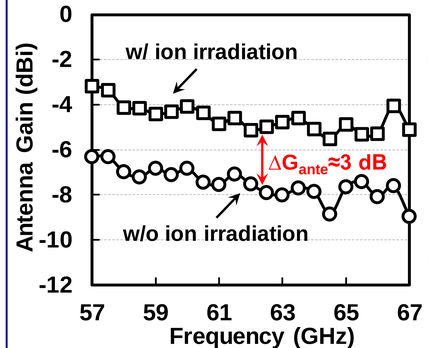
60-GHz injection-locked oscillator

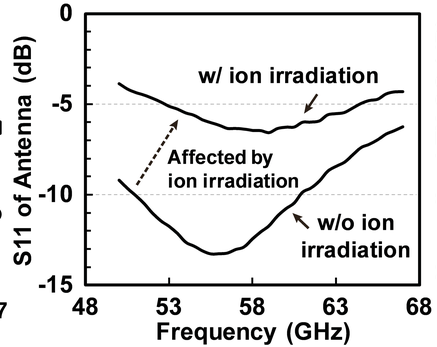
- Coarse tuning 2-bit cap. array
- Fine tuning varactors
- Cover 58 GHz-65 GHz

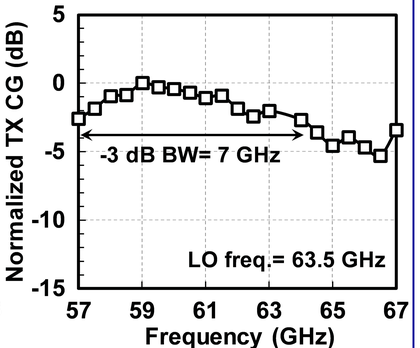


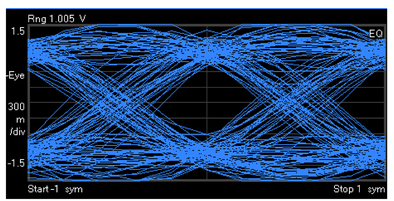
Die micro-photograph

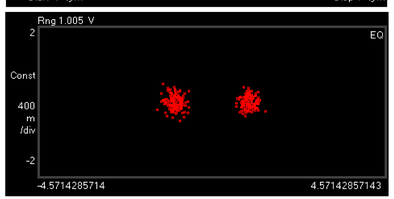
6. Measurement Results











Ref.	Process	Modulation	Data Rate	Power	Antenna	Core Aera
This work	65 nm CMOS	BPSK	5.0 Gb/s†	17 mW	**On-chip**	0.64 mm²
[1]	40 nm CMOS	ASK	11.0 Gb/s	29 mW	Off-chip	0.06 mm²
[2]	90 nm CMOS	OOK	10.7 Gb/s	31 mW	Off-chip	0.15 mm²
[3]	65 nm CMOS SOI	OOK	2.2 Gb/s	28 mW	**On-chip**	0.82 mm²*
[8]	65 nm CMOS	QPSK	10.4 Gb/s	50 mW	**On-chip**	2.15 mm²*

*Estimated from literature †Limited by the meas. equipment

Modulation: BPSK EVM: -12 dB
Data rate: 5 Gb/s (LO freq.=63.5 GHz)

[1] K. Kawasaki *et al.*, ISSCC2010 [2] C.W. Byeon *et al.*, TMTT2013
[3] A. Siligaris *et al.*, RFIC2013 [8] L. Kong *et al.*, ISSCC2013

7. Conclusions

- The gain of the CMOS on-chip antenna is improved 3 dB by using the Helium-3 ion-irradiation technique;
- The transmitter achieves 5-Gb/s data rate while consuming only 17 mW power with die area of 0.64 mm²;
- Well-suited for short-range wireless interconnect applications.