A 17-mW 5-Gb/s 60-GHz CMOS Transmitter with Efficiency-Enhanced On-Chip Antenna

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***Abstract* — A 60-GHz CMOS transmitter with on-chip antenna for high-speed short-range wireless interconnection is presented. The radiation efficiency of the on-chip antenna is doubled using substrate loss improvement techniques. The transmitter fabricated in a 65-nm CMOS process achieves over 5 Gb/s data rate with an EVM performance of -12 dB for BPSK modulation. The whole transmitter consumes 17 mW from a 1.2-V supply and occupies a core area of 0.64 mm^2 including the on-chip antenna.**

***Index Terms* — CMOS, 60-GHz transmitter, on-chip antenna, efficiency-enhanced technique**

I. Introduction

Wireless interconnects have become a field of interest with the required number and bandwidth of internal I/O in today's portable electronic systems continuously increasing [1], [2]. When the wireless interconnect is used for internal (*e.g.* chip-to-chip) data communication of portable devices, low power consumption, high data rate (*e.g.* multi-gigabit per second), full on-chip integration, and low possible external interference level are generally preferred. A 60-GHz wireless interconnect is one of the most promising candidates for the short-range internal communication considering the trade-offs mentioned above. The transmitter in [2] shows a 10.7-Gb/s 60-GHz data link in CMOS technology, but this solution is power hungry due to the existence of the active modulator and buffers. Furthermore, an off-chip antenna is adopted for the system because of the intrinsic low gain of the CMOS on-chip antenna, which dramatically increases circuit size and introduces parasitic components. Literature [3] demonstrates a fully integrated 60-GHz transmitter with 2.2-Gb/s data rate. However the use of switched pulse-injected oscillator limits the communication data rate. A phased-array 60-GHz transmitter [4] is realized to overcome the intrinsic low gain of CMOS on-chip antenna achieving over 10-Gb/s data rate.

This paper presents a 60-GHz low power multi-Gb/s transmitter with a single on-chip antenna fabricated in a 65 nm CMOS technology. The average radiation gain of -5 dBi for the on-chip antenna is achieved by using substrate loss reduction techniques. The wideband and power-saving design of the transmitter core circuit guarantee the high data rate with low power consumption. The proposed transmitter demonstrates short-range communication at a data rate of 5 Gb/s with a core area of 0.64 mm^2 (including the on-chip antenna) while consuming only 17 mW.

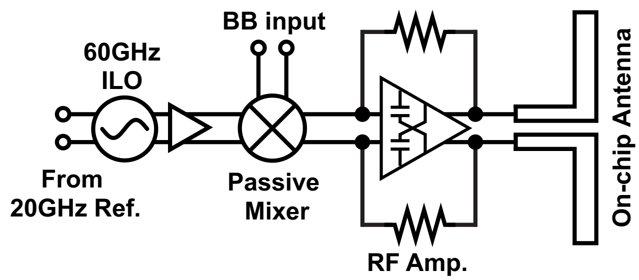


Fig. 1. System block diagram of the proposed 60-GHz fully-integrated transmitter.

II. Transmitter Architecture and Design

The system block diagram of the fully integrated 60-GHz transmitter is shown in Fig. 1. The whole transmitter is composed of an on-chip dipole antenna, a resistive-feedback RF amplifier, a double-balanced passive mixer, and an injection-locked oscillator (ILO).

A. 60-GHz CMOS On-Chip Antenna

The realization of on-chip antenna in CMOS process with reasonable radiation gain is a challenging issue due to the low-resistivity characteristics of Si substrate [5]. In order to gain a quantitative insight for the loss contribution, an analysis model of an on-chip dipole antenna is constructed as depicted in Fig. 2. The top metal layer is used for the dipole which is fed by two microstrip lines (MSLs). The silicon substrate ($\varepsilon_r = 12$) is modeled by a lossy layer with resistivity of 10 Ω·cm and 320 μm thickness. The detailed dimensions are illustrated in Fig. 2 (b). Fig. 3 shows the simulated radiation gain pattern of the dipole antenna using the model described in Fig. 2. The radiation gain of the antenna is only -30 dBi which corresponds to an efficiency of 0.1 %. It is worthy of noting that silicon substrate contributes 70 % of losses. Therefore, reducing the substrate loss is an effective solution for on-chip antenna gain enhancement. Conventionally, the proton irradiation techniques are employed to increase the substrate resistivity [6]. However, the proton bombardment suffers from poor irradiation efficiency and lateral scattering causing reliability issues and high process cost [7].

In this work, a helium-3 ion bombardment technique is employed to improve the on-chip antenna efficiency. By using the helium-3 irradiation technique, the substrate resistivity can be effectively increased from 6 Ω·cm to over 1000 Ω·cm with a small dose amount of $3\times10^{13}\mathrm{cm}^{-2}$. Meanwhile, helium-3 ion has less lateral scattering than proton. Therefore, a high-reliability low-process-cost technique can be utilized to increase the substrate resistivity. Fig. 4 shows the proposed technique for the efficiency improvement of the CMOS on-chip antenna. The antenna configuration is the same as in Fig. 2 except the $600\,\mu\mathrm{m}\times1200\,\mu\mathrm{m}$ white area around the antenna indicates the ion irradiated zone. Simulations results demonstrate that the radiation efficiency is increased by 62 % when the technique in Fig. 4 is applied.

B. RF Front-End Circuit Design

The wideband characteristic and low power consumption are important for the design of 60-GHz wireless interconnect transmitter. However, an baseband input buffer, which achieves 50-Ω impedance matching, generally has a narrow-band characteristic. In this work, the wideband input impedance matching is realized by using the double-balanced passive mixer and resistive-feedback RF amplifier as demonstrated in Fig. 5. The wideband input impedance flatness of the RF amplifier is implemented by a resistive-feedback matching technique [8]. The input impedance of the RF amplifier (Z_{RF}) is down-converted to the baseband. The baseband input impedance (Z_{in}) is determined by Z_{RF} and the on-resistance (R_{SW}) of the switches used for the passive mixer, which maintains the wideband matching for the baseband input.

$$Z_{\mathrm{in}}(\omega) \approx R_{\mathrm{SW}} + \frac{8}{\pi^2}\mathrm{Re}[\mathrm{Z}_{\mathrm{RF}}(\omega_{\mathrm{LO}})] \tag{1}$$

The finger width and numbers of the passive mixer switches are also optimized for reducing the required power from local oscillator (LO). The energy efficient LO is realized by an injection-locked solution [9]. Fig. 6 shows the schematic of the 60-GHz injection-locked oscillator (ILO). A 2-bit capacitor array for coarse tuning and varactors for fine tuning are used to cover 58 GHz–65 GHz frequency range.

III. Measurement Results

To verify our design, the proposed low power high data rate 60-GHz transmitter with on-chip antenna is fabricated

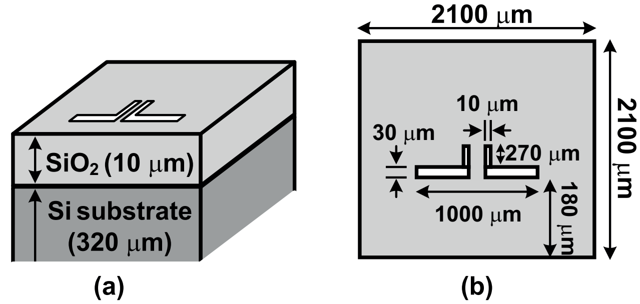


Fig. 2. Analysis model of an on-chip dipole antenna (a) 3-D view; (b) top view with antenna configurations.

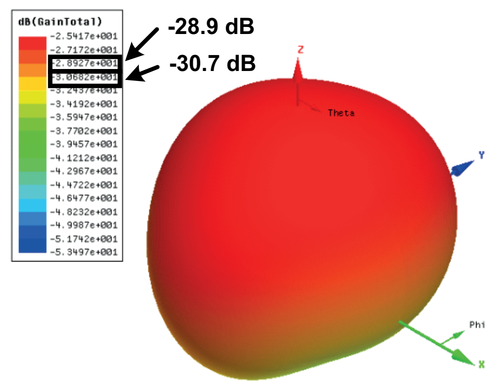


Fig. 3. Simulated 3-D radiation pattern of the dipole antenna with the lossy layers.

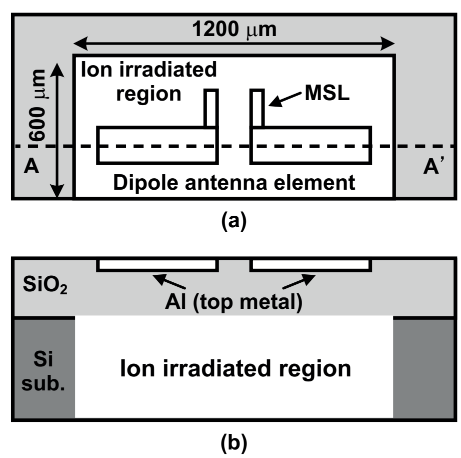


Fig. 4. The proposed efficiency-enhanced on-chip dipole antenna (a) top view; (b) A–A' cross-section view.

in a 65 nm CMOS technology. Fig. 7 shows the die microphotograph of the whole transmitter. The areas of the transmitter core and the on-chip antenna are $0.18\,\mathrm{mm}^2$ and $0.46\,\mathrm{mm}^2$, respectively. The stand-alone test chips for on-chip antenna characterization are also fabricated. There are

TABLE I
60-GHz Low-Power High-Data-Rate TX Performance Comparison.

Ref.	CMOS Process	Modulation	Data Rate	Power	Antenna	Core Area
This work	65 nm	BPSK	5.0 Gb/s†	17 mW	**On-chip**	0.64 mm^2
[1]	40 nm	ASK	11.0 Gb/s	29 mW	Off-chip	0.06 mm^2
[2]	90 nm	OOK	10.7 Gb/s	31 mW	Off-chip	0.15 mm^2
[3]	65 nm SOI	OOK	2.2 Gb/s	28 mW	**On-chip**	0.82 mm^2*
[4]	65 nm	QPSK	10.4 Gb/s	50 mW	**On-chip**	2.15 mm^2*

* Estimated from literature † Limited by the measurement equipments

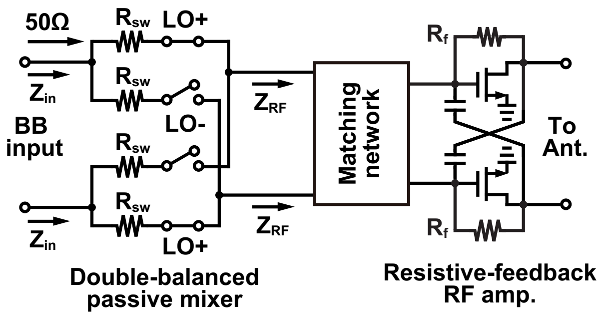


Fig. 5. The topology of the double-balanced passive mixer and resistive-feedback RF amplifier.

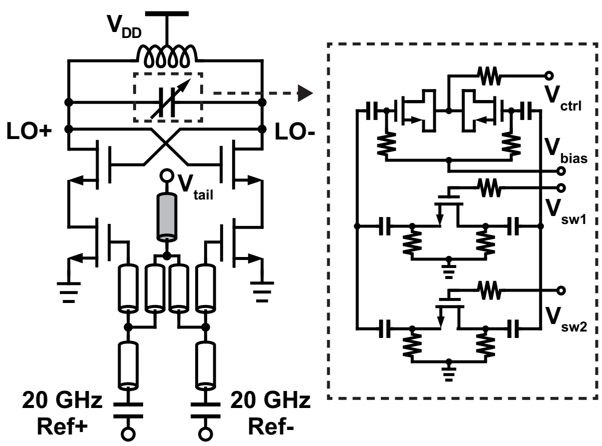


Fig. 6. 60-GHz injection-locked oscillator topology.

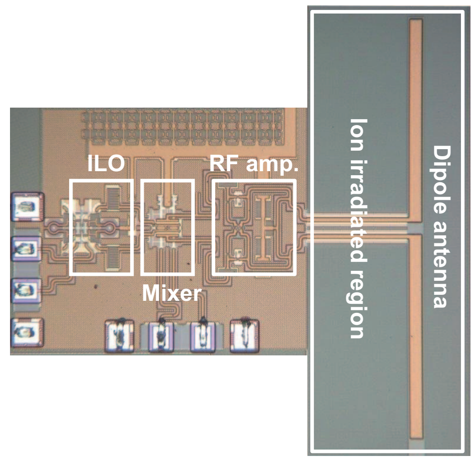


Fig. 7. Die micro-photograph. Antenna: 0.46 mm^2, TX core: 0.18 mm^2.

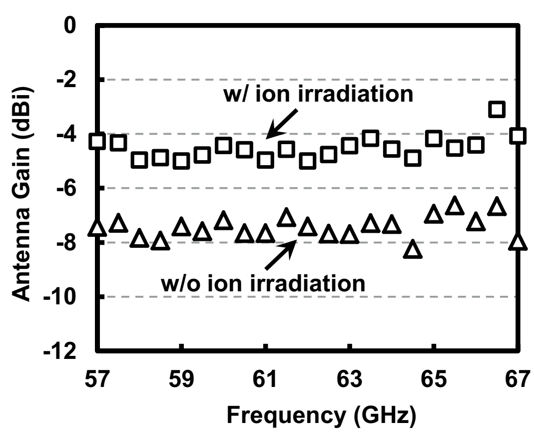


Fig. 8. Measured antenna gain versus frequency for two types of test chips.

two types of test chips. One type is processed by helium-3 ion bombardment technique over the region indicated in Fig. 7, while the other type has no ion-irradiated area.

Fig. 8 shows the measurement results of the antenna gain versus frequency for the two types of test chips. When the ion irradiation is not applied, the radiation gain of over -8 dBi is achieved from 57 GHz to 67 GHz with the gain variation of less than 2 dB. After the ion bombardment, the radiation gain is improved to be higher than -5 dBi which corresponds to around 30 % efficiency. The average gain improvement is 3 dB over the 10-GHz band of interest. The wideband characteristic of the on-chip antenna is maintained after the ion-irradiated processing.

The conversion gain (CG) of the transmitter with the efficiency-enhanced antenna is also measured when the LO is operating at 63.5 GHz. Fig. 9 shows the normalized CG

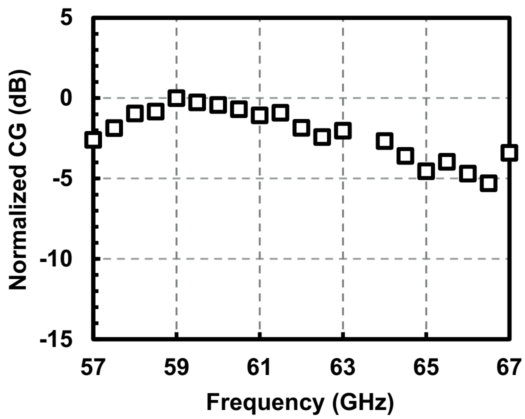
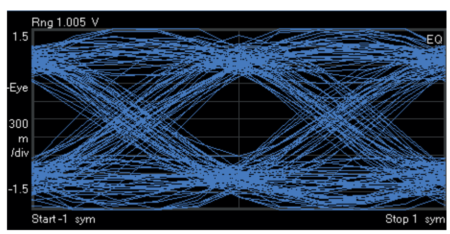


Fig. 9. Measured transmitter conversion gain (including on-chip antenna) versus frequency.



Modulation	**BPSK**
Data rate	**5 Gb/s**
EVM	**-12 dB**

Fig. 10. Measured eye diagram at 5 Gb/s data rate for BPSK modulation (Limited by measurement equipments).

versus frequency. The -3 dB bandwidth is 7 GHz (57 GHz–64 GHz) referred to the peak gain at 59 GHz.

The data communication performance of the proposed transmitter is evaluated by applying a BPSK modulation signal to the baseband input with a data rate of 5 Gb/s which is limited by the measurement equipments. The frequency of the LO is 63.5 GHz, which consumes 10 mW power from a 1.2-V supply. The eye diagram is demonstrated in Fig. 10 showing an EVM performance of -12 dB.

Table I summarizes and compares the performance of the proposed transmitter with that of the state-of-the-art low-power high-data-rate TXs at 60 GHz in CMOS processes. The proposed transmitter shows the lowest power consumption, comparable data rate, and the smallest area with respect to the full on-chip solution.

IV. Conclusion

This paper presents a 60-GHz low-power high-data-rate transmitter with an efficiency-enhanced on-chip antenna in a 65-nm CMOS process. The radiation gain of the on-chip antenna is improved 3 dB by using the ion-irradiation techniques. The transmitter achieves 5-Gb/s data rate while consuming only 17 mW power with the area occupation of 0.64 mm^2, which is well-suited for the short-range wireless interconnection applications.

Acknowledgment

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