22.6 A 2.2GS/s 7b 27.4mW Time-Based Folding-Flash ADC with Resistively Averaged Voltage-to-Time Amplifiers

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High-speed low-resolution ADCs are widely used for various applications, such as 60GHz receivers, serial links, and high-density disk drive systems. Flash architectures have the highest conversion rate without employing time-interleaving. Moreover, flash architectures have the lowest latency, which is often required in feedback-loop systems. However, the area and power consumption are exponentially increased by increasing the resolution since the number of comparators must be 2^N. A folding architecture is a well-known technique to reduce the number of comparators in an ADC while maintaining high sampling rate and low latency [1, 2]. Folding architectures were previously realized by generating a number of zero crossings with folding amplifiers. However, the conventional folding amplifiers consume a large power to realize a fast response. In contrast, a folding ADC with only dynamic power consumption and without using amplifiers was reported [3]. However, only a folding factor of 2 is realized, therefore the number of reduced comparators is half.

This paper presents a 2.2GS/s 7b time-based folding ADC with resistively averaged voltage-to-time amplifiers (V-T amps). This time-based folding architecture consists of simple logic cells with a folding factor of 8 instead of the conventional static amplifiers. This reduces the number of comparators from 128 to 32 for a 7b resolution. Resistively averaged V-T amps have a low offset voltage and a high conversion gain to relax the offset requirement for the SR-latch. This ADC achieves an SNDR of 37.4dB at Nyquist frequency without any calibration technique.

Figure 22.6.1 shows the block diagram of the ADC. The input signal is sampled on passive S/H circuits with the total sampling capacitance of 300fF. An array of 25 V-T amps, 10 of which are dummies to generate extra folding points and overcome the edge effects in resistive averaging networks, converts the sampled voltages into pulse signals that have a delay time depending on input voltage levels. Next, pulse signals are inputted to the coarse SR latch and the time-based folder (TF) blocks. The coarse SR latches compare the delay time and determine the upper 4b digital code. Four TF output folded delay signals to the fine interpolated SR latches. The fine interpolated SR latches convert the delay signal to the lower 4b digital code. The encoder corrects coarse and fine digital codes and converts 7b data with 1b redundancy. Finally, 7b data are retimed by D-FFs.

Figure 22.6.2 shows the dynamic V-T amps with resistive averaging. The V-T amp is based on the dynamic preamp of double-latch-type comparator [4] with a positive feedback circuit. During the reset phase (ϕ_L =0), M_7 and M_8 pre-charge the D_P and D_N nodes to the supply voltage. After the reset phase, ϕ_L turns to high, M_7 and M_8 are turned off and M_9 is turned on. At D_P and D_N nodes, the voltage drop with a rate determined by the input differential voltage and an input dependent Δt_d will build up in a short time around 100ps. M_5 and M_6 form a positive feedback circuit to enhance the gain of the V-T conversion. M_3 and M_4 control the positive feedback to a suitable ratio because too much positive feedback degrades the linearity of the V-T conversion. In this design, the gains of the V-T conversion with and without positive feedback are 1.1ps/mV and 0.24ps/mV, respectively. The V-T conversion gain with positive feedback is enough to eliminate an offset calibration technique for coarse and fine SR latches. A resistive averaging technique is a well-known technique used to reduce the mismatch of conventional static amplifiers [5]. This architecture is also effective in a dynamic amplifier without increasing power consumption because it has no static current path. The offset voltage of the dynamic amplifier can be reduced to about 1/3.

Figure 22.6.3 shows the TF architecture and the circuit implementation. Delay times of V-T amps are slightly different depending on each reference voltage. The first mountain fold can be realized by using OR gates to select the faster delay signals, D_{1_1} is D_{N0} OR D_{P2} and D_{1_2} is D_{N4} OR D_{P6}. The second valley fold can be realized by using an AND gate to select the slower delay signals, D_{2_1} is D_{1_1} AND D_{1_2}. Finally, D_{F1} can be realized by D_{2_1} AND D_{2_2}. These logic cells have symmetrical input to obtain the same transition time from D_1 or D_2 to output. This architecture consists of simple logic cells with only dynamic power consumption. Moreover, this TF performs in very short time, about 100ps, because only three-cascaded OR and AND cells are required to realize the folding factor of 8. TF block outputs four folding signals, D_{F1}, D_{F2}, D_{F3} and D_{F4}, to realize interpolated signals in the following fine SR latch block.

Figure 22.6.4 shows the fine SR latch circuit with a phase interpolator [6]. Firstly, to realize the time-domain interpolation, the rising slope of the folding signal is moderated. A 3b phase interpolator consists of 2-stage cascaded inverters. The interpolation ratio of the 2b stage is realized by changing the number of the inverters, such as one-three, two-two and three-one ratios. Next interpolator has a fixed ratio of one-one. Finally, the phase-interpolated delay signal is converted into a digital code by the SR latch, which consists of NAND gates. The coarse SR latch has the same structure without interpolators. The offset voltage of the SR latch is negligible because the steep rising signals are less sensitive to Vt mismatch of the transistor. Moreover, the gain of V-T amps effectively reduces the input-referred offset voltage of the SR latch. Therefore, no offset calibration technique is required in this design.

The chip is fabricated in a digital 40nm LP CMOS technology and the occupied area is 0.052mm^2, as show in Figure 22.6.7. The supply voltage is 1.1V with a power consumption of 27.4mW (3.3mW for reference ladder, 19.4mW for analog and 4.7mW for digital) at a sampling rate of 2.2GS/s. The input signal range is 1.0Vpp in the differential. The output code is decimated by 8 in the measurement. The measured DNL and INL are +0.6/-0.6 and +1.0/-1.0 LSB, respectively. Figure 22.6.5 shows the measured SNR, SFDR and SNDR *vs.* sampling rate and input frequency. An SNDR of 38.3dB is measured up to 2.2GS/s with a 100-MHz input frequency. Also, an SNDR of 37.4dB is obtained at 2.2GS/s with Nyquist frequency of 1.1-GHz input frequency. The FoMw of 210fJ/conv.-step and the FoMs of 143.3dB at Nyquist frequency are achieved, respectively.

Figure 22.6.6 shows the performance summary and comparison of flash and folding ADCs achieving a conversion rate of several GS/s [7-9].

Acknowledgments:
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References:
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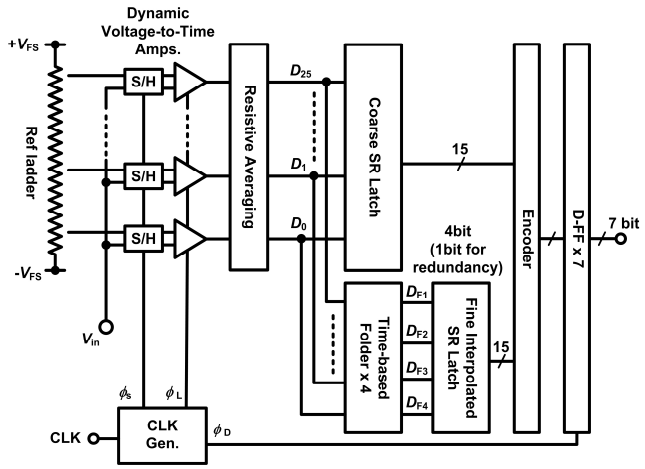


Figure 22.6.1: Block diagram of the time-based folding flash ADC.

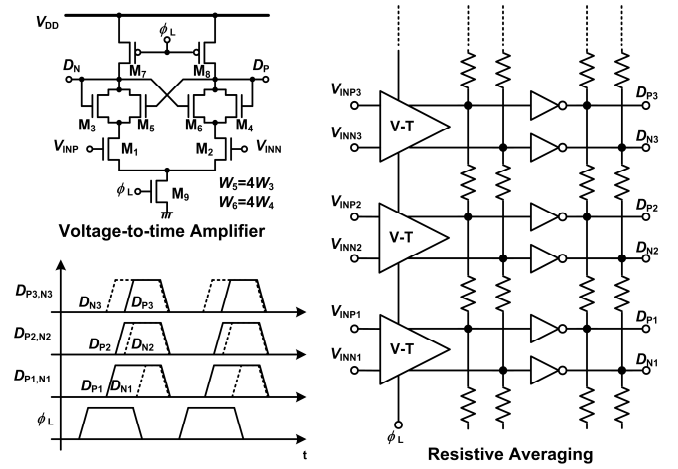


Figure 22.6.2: Voltage-to-time amplifier with positive feedback for gain boosting and resistive averaging.

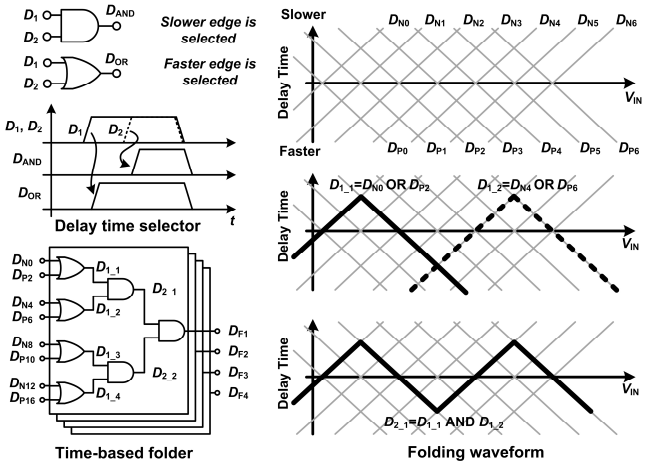


Figure 22.6.3: Time-based folder architecture and circuit implementation.

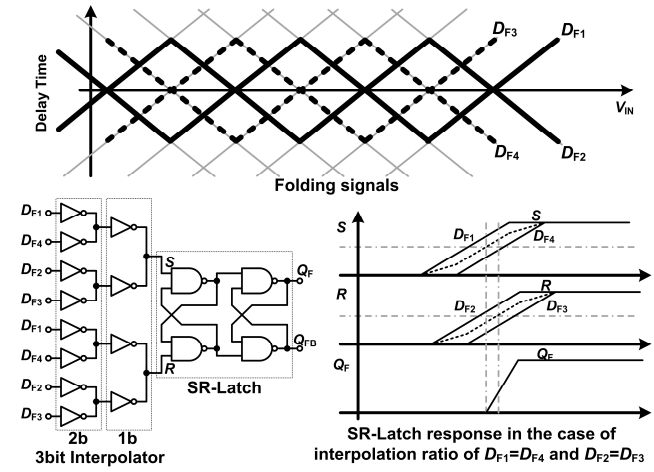


Figure 22.6.4: Interpolated fine SR latches.

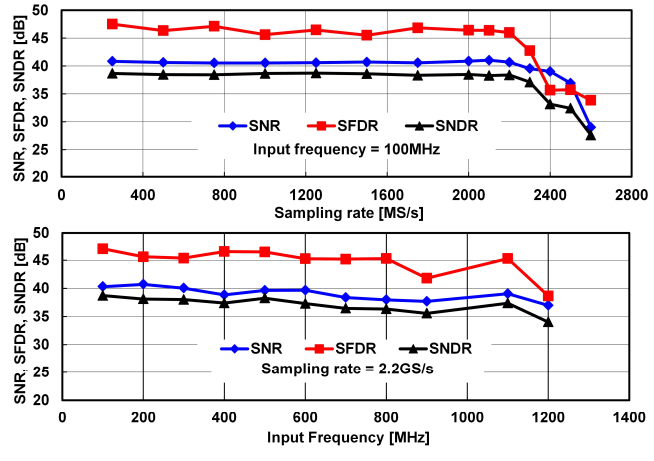
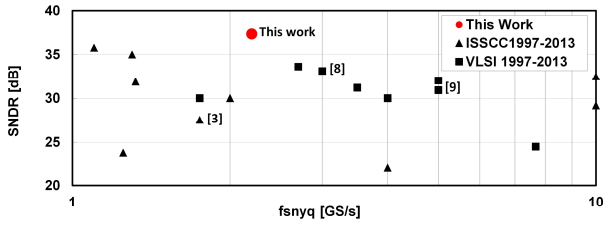


Figure 22.6.5: Measured SNDR vs. sampling frequency and input frequency.



	ISSCC 2008 [3]	VLSI 2012 [8]	VLSI 2013 [9]	This work
Technology	90nm	40nm	32nm SOI	40nm LP
Resolution [bit]	5	6	6	7
Power Supply [V]	1	1.1	0.85	1.1
Sampling Frequency [GS/s]	1.75	3	5	2.2
Power Consumption [mW]	2.2	11	8.5	27.4
SNDR @Nyquist [dB]	27.6	33.1	30.9	37.4
FoMw [fJ/conv.-step]	64.5	99.3	59.4	210
FoMs [dB]	143.5	144.4	145.6	143.3
Core area [mm^2]	0.0165	0.021	0.02	0.052
Calibration	Off chip	Foreground	Off chip	No need

Figure 22.6.6: Performance comparison of flash and folding ADCs with sampling rate of several GS/s.

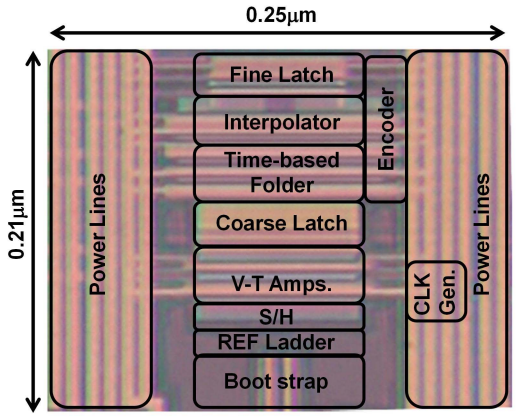


Figure 22.6.7: Die micrograph.