A 2.2GS/s 7b 27.4mW Time-Based Folding-Flash ADC with Resistively Averaged Voltage-to-Time Amplifiers

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Outline

- Motivation
- Design concepts
  - Time-based folding architecture
  - Voltage-to-time amplifier
- Measurement results
- Conclusion

Motivation

Flash ADCs

- ☺ Highest conversion rate and lowest latency
  - ⇒ High speed feedback-loop systems
- ☹ Power and area are proportional to the number of comparators

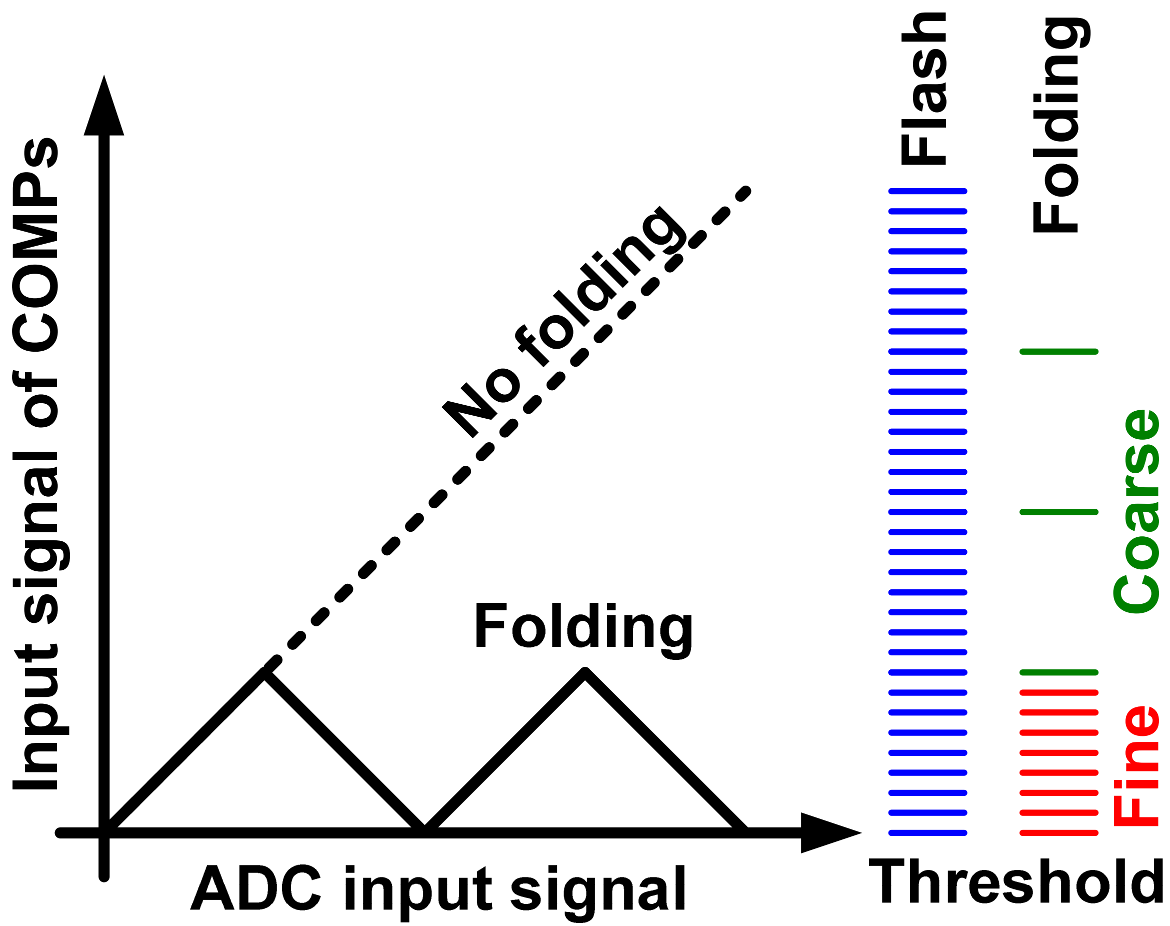
Folding-Flash ADCs

- ☺ Less number of comparators
- ☹ Power consuming of amplifiers in the folding circuit[1, 2]

New efficient folding architecture is required

[1] Y. Nakajima, *et al.*, JSSC 2010 [2] T. Yamase, *et al.*, VLSI symp. 2011

Conventional Folding-Flash ADC



N : Resolution [bit]

Folding times

2^M-1

Number of Comps

2^M + 2^{N-M+1}

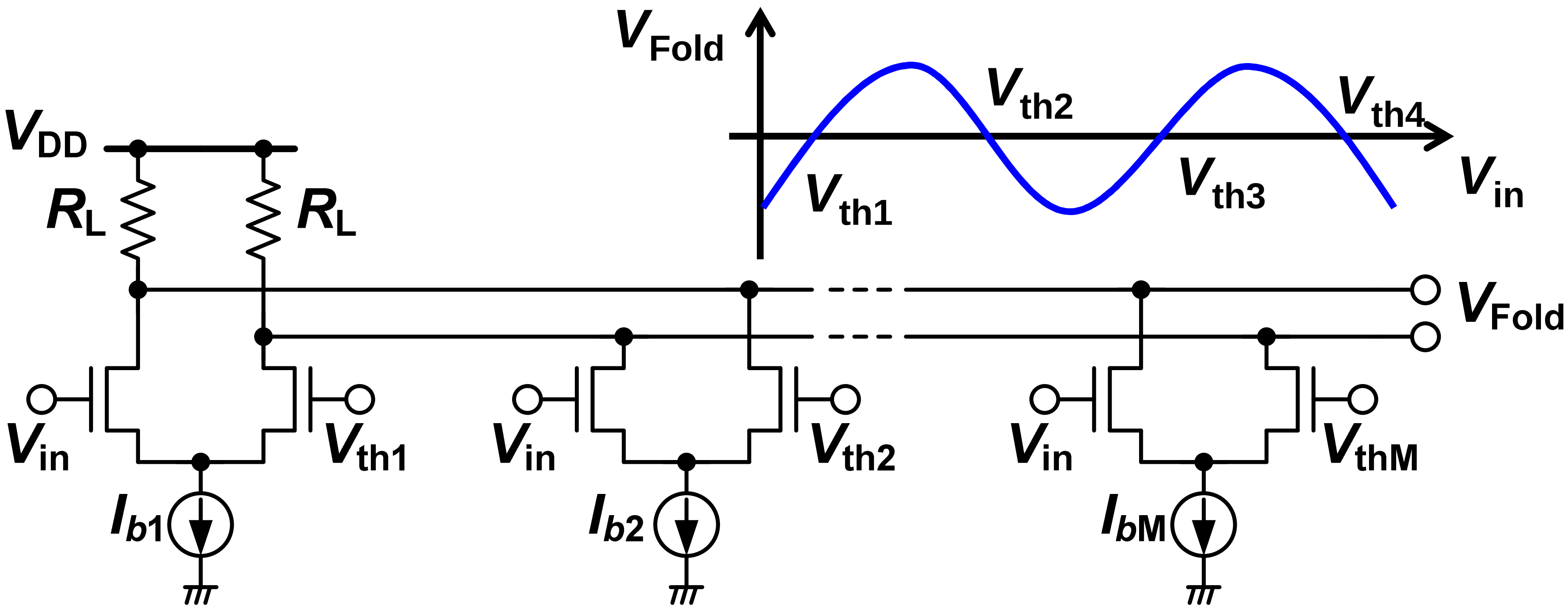
Coarse Fine

N=7bit, *M*=4

128⇒32

Conventional Folding Circuit

- Large current is needed for high speed
- Voltage gain is reduced by technology scaling



New Design Concepts

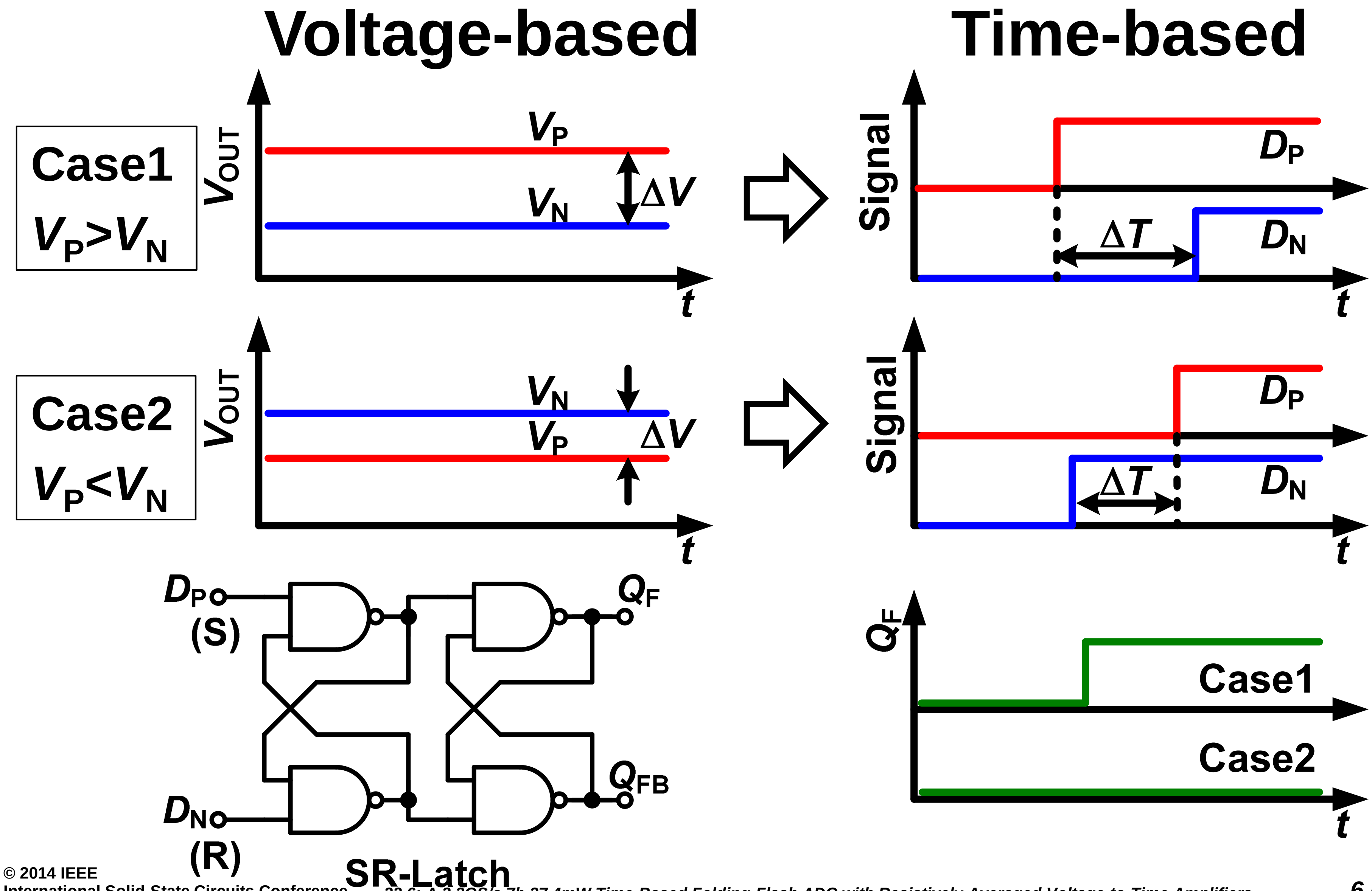
Time-based-folding architecture

- Voltage-based ⇒ Time-based Folding
  - ☺ More suitable for finer process
- Simple logic circuits can realize folding signal of the timing edge
  - ☺ No static current

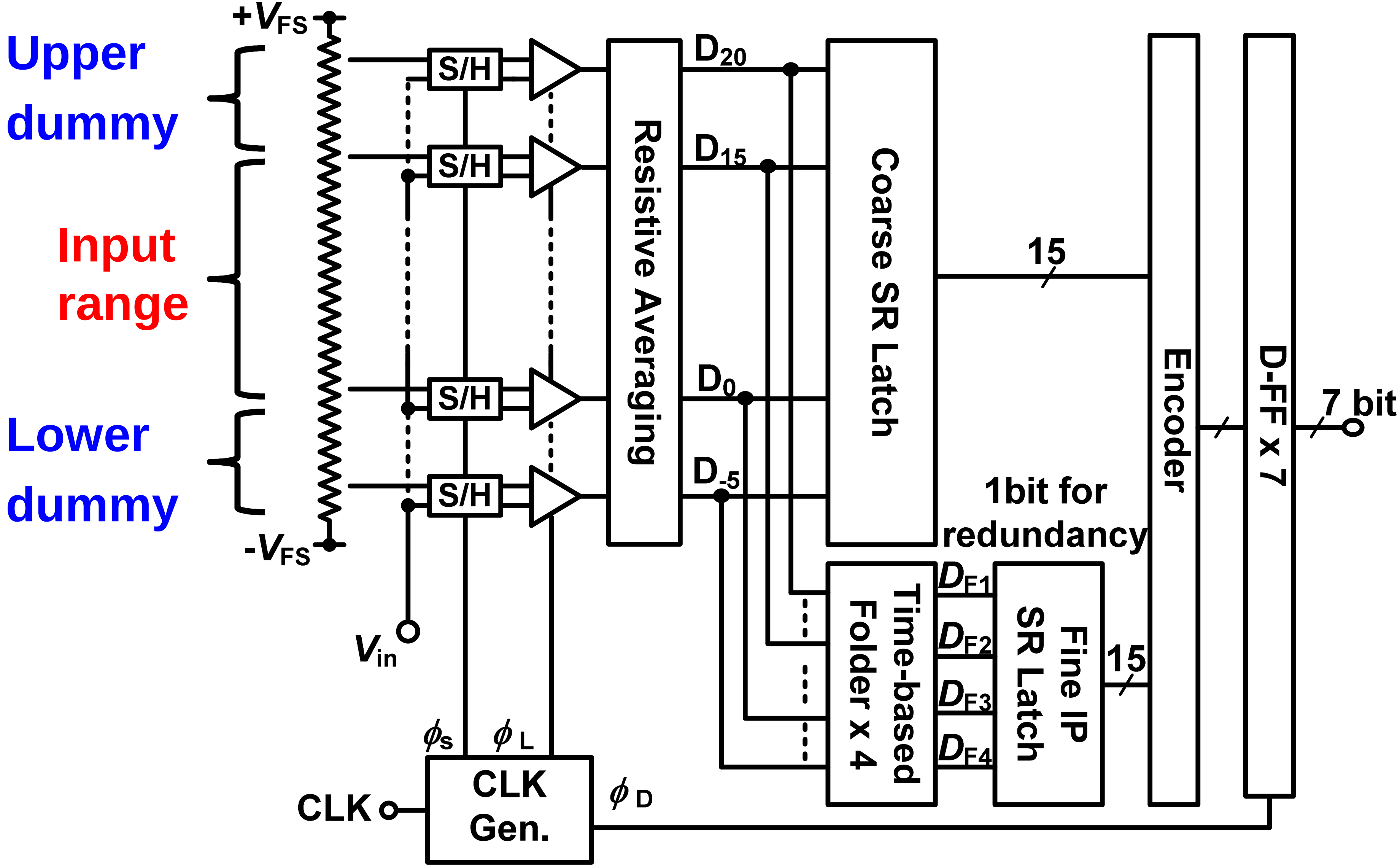
Voltage-to-time amplifier

- Dynamic amplifier with resistive averaging
  - ☺ No static current
  - ☺ No need of calibration

Voltage to Time Conversion

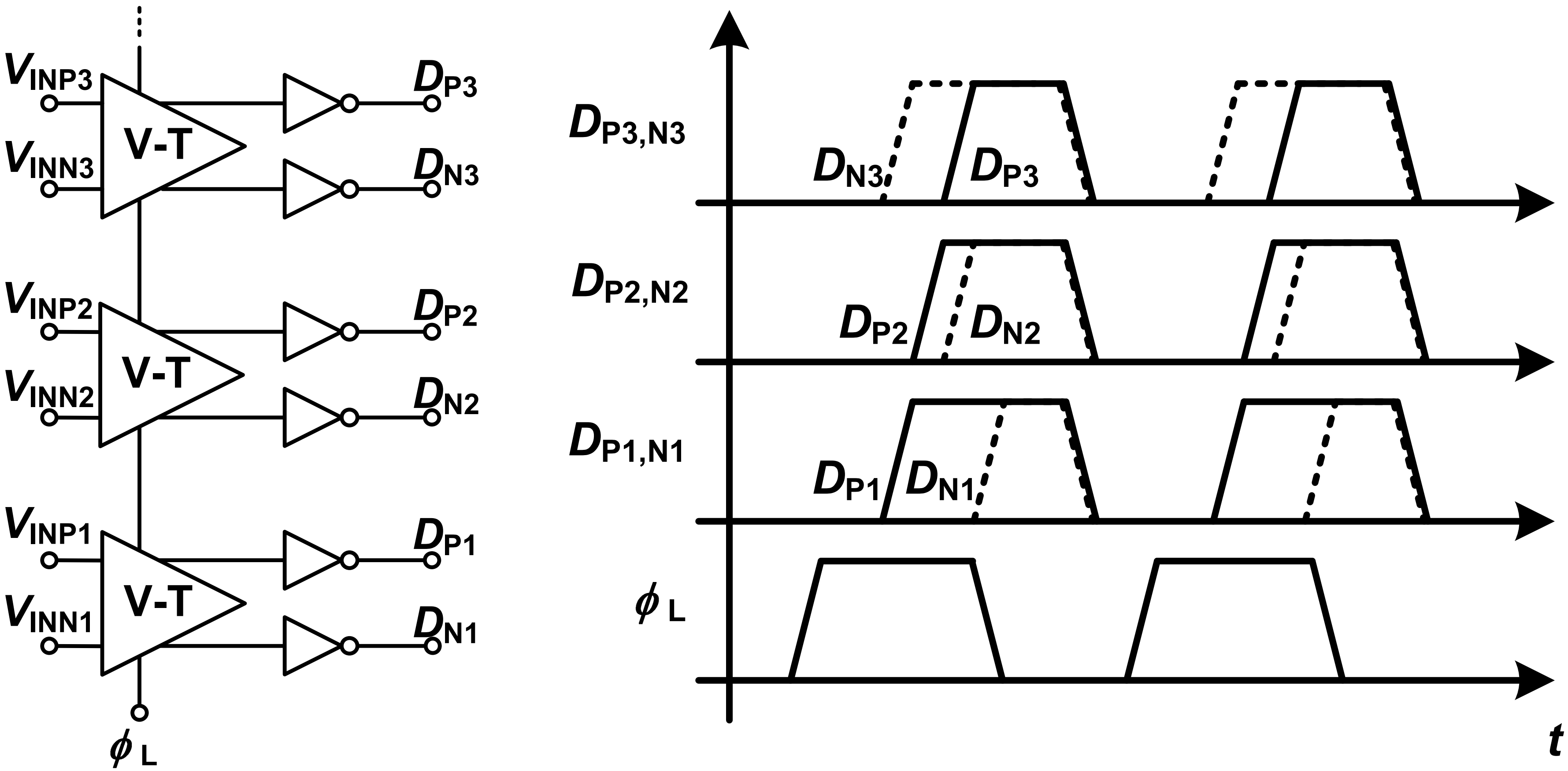


Block Diagram



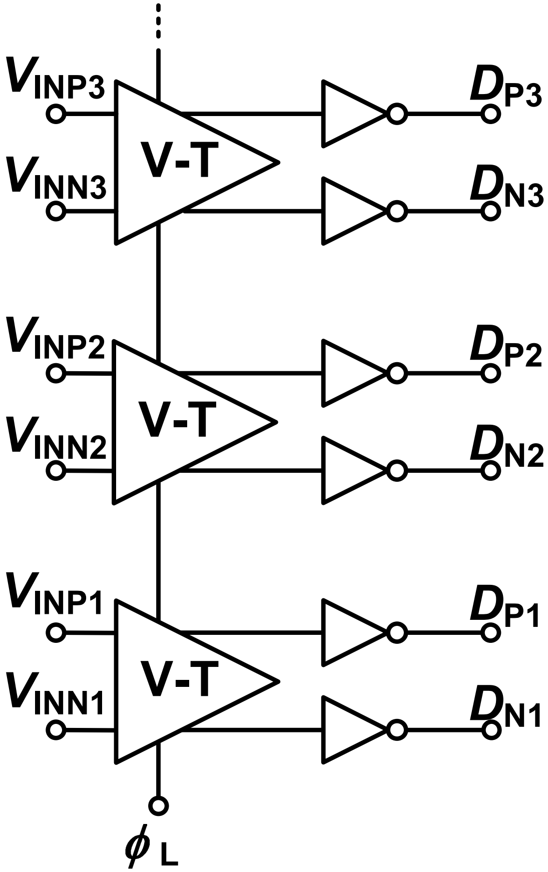
Output of VT Amps

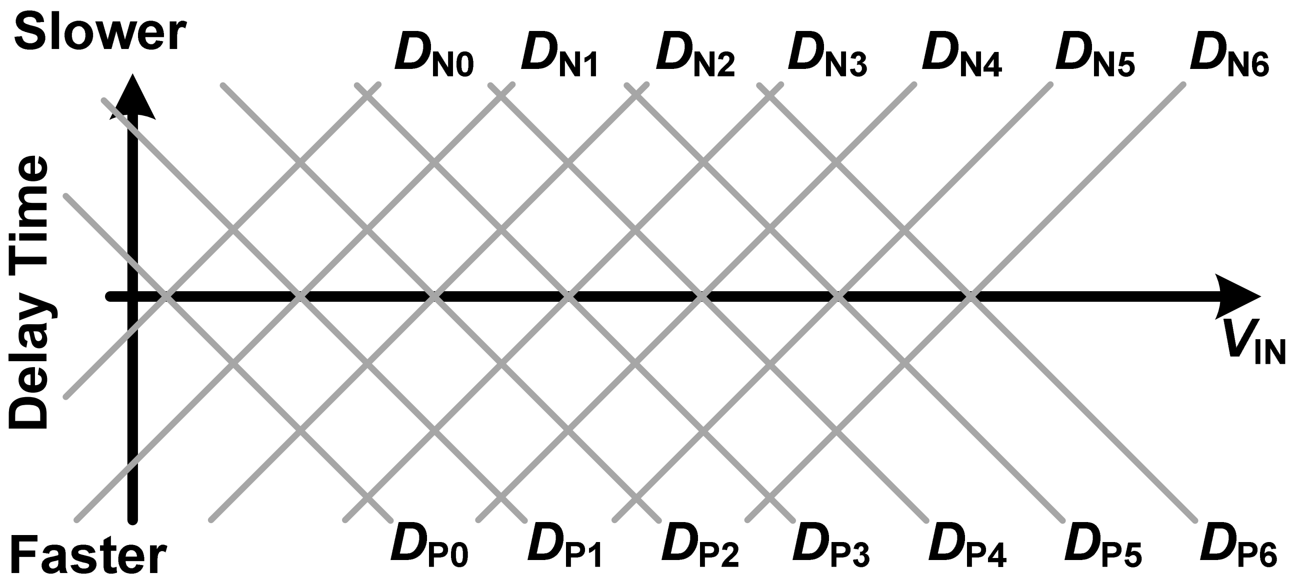
Each VT Amp generates pulse signal which has delay time depending on input signal.



Output of VT Amps

How is the folding signal generated in time domain?

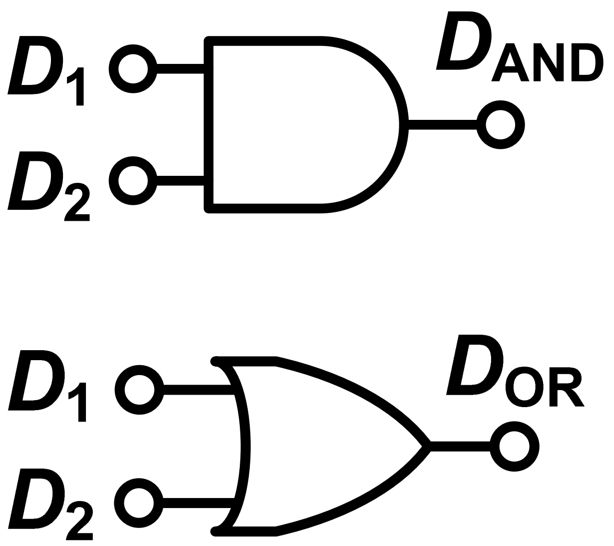


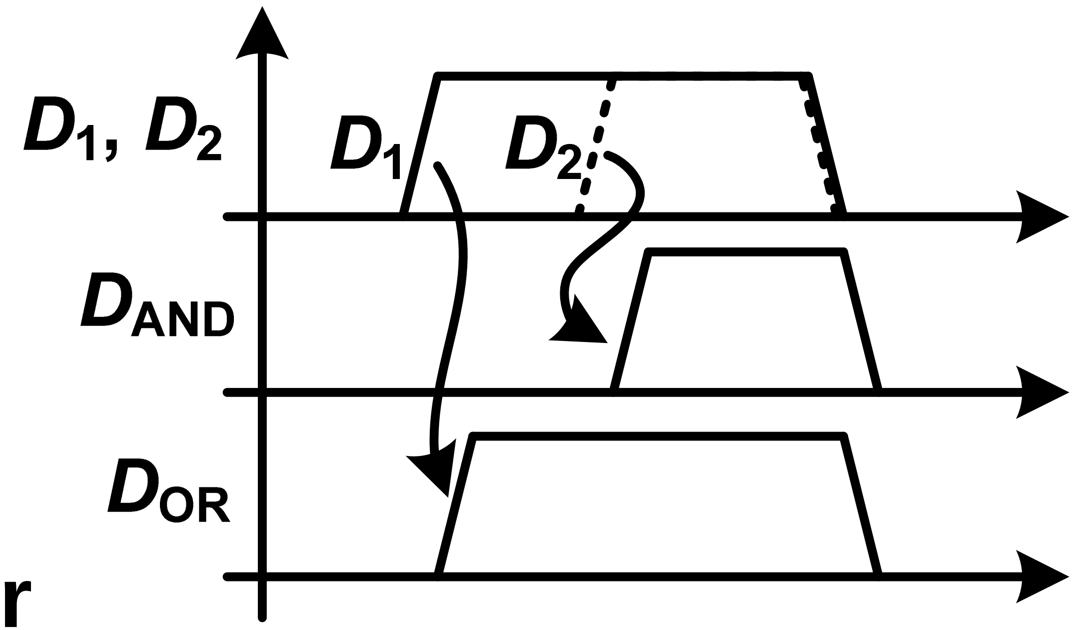


Delay Time Selector

Slower signal ⇒ AND Gate

Faster signal ⇒ OR Gate

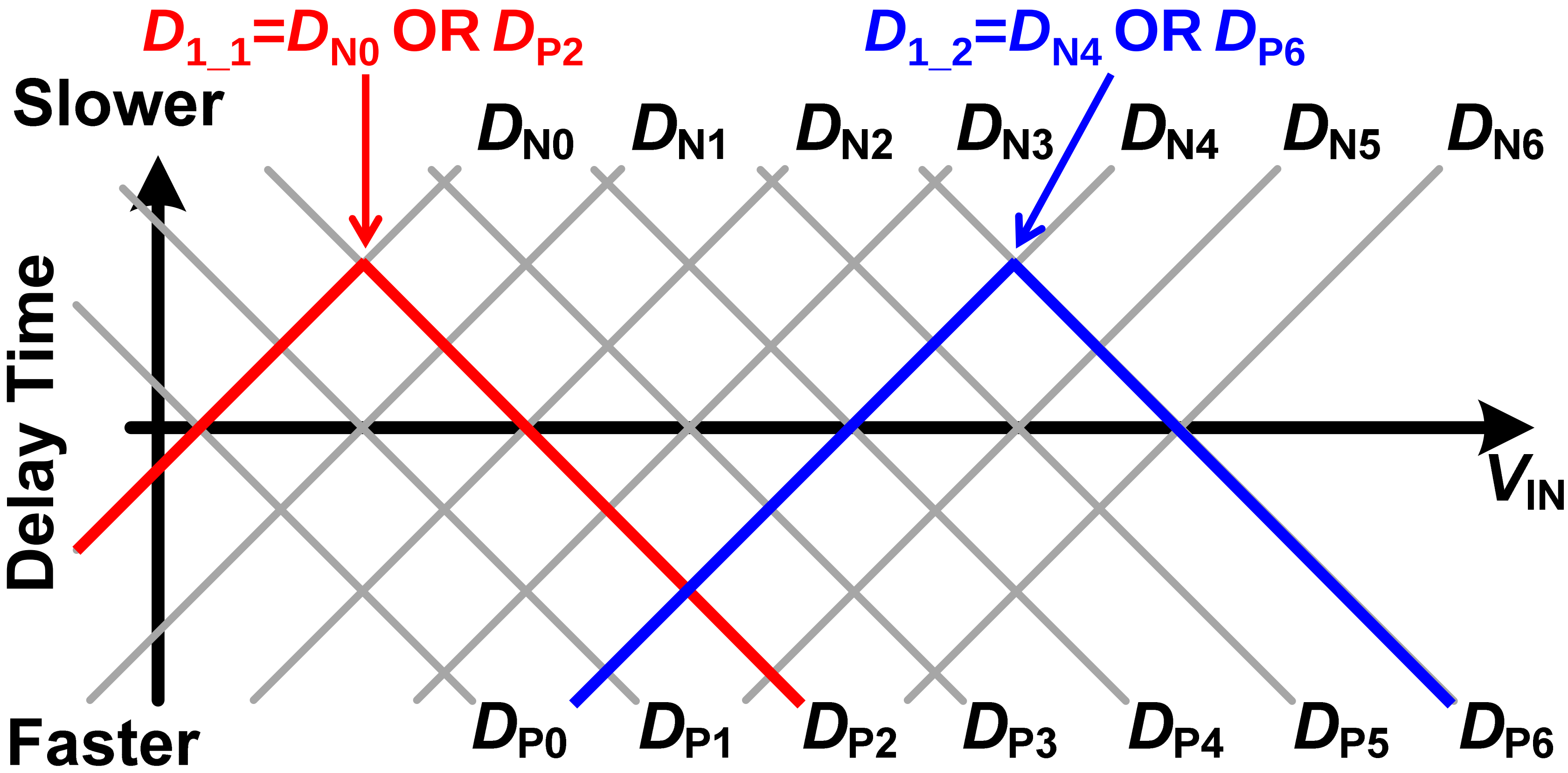




Delay time selector

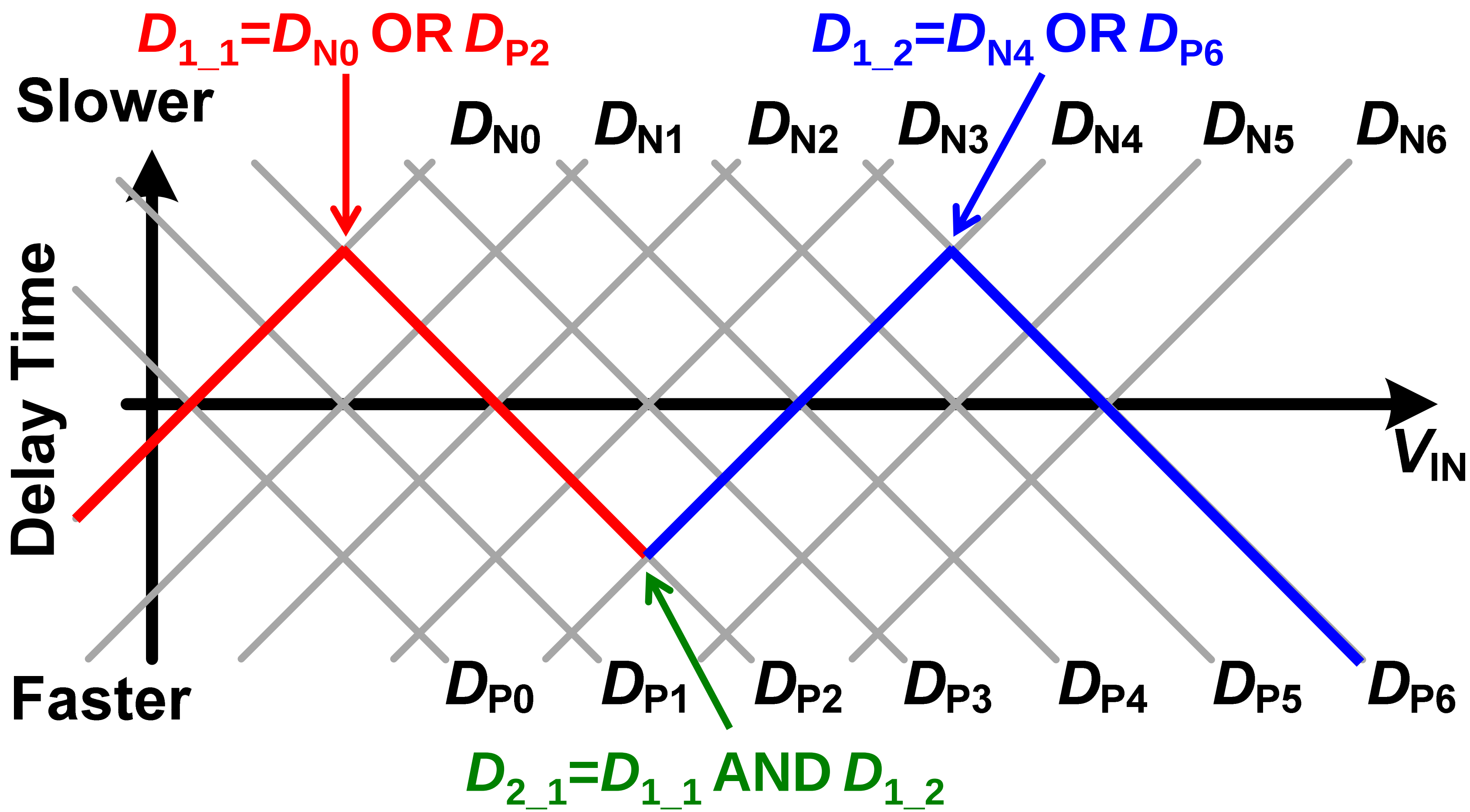
Time-Based-Folding

Peak fold ⇒ OR gate



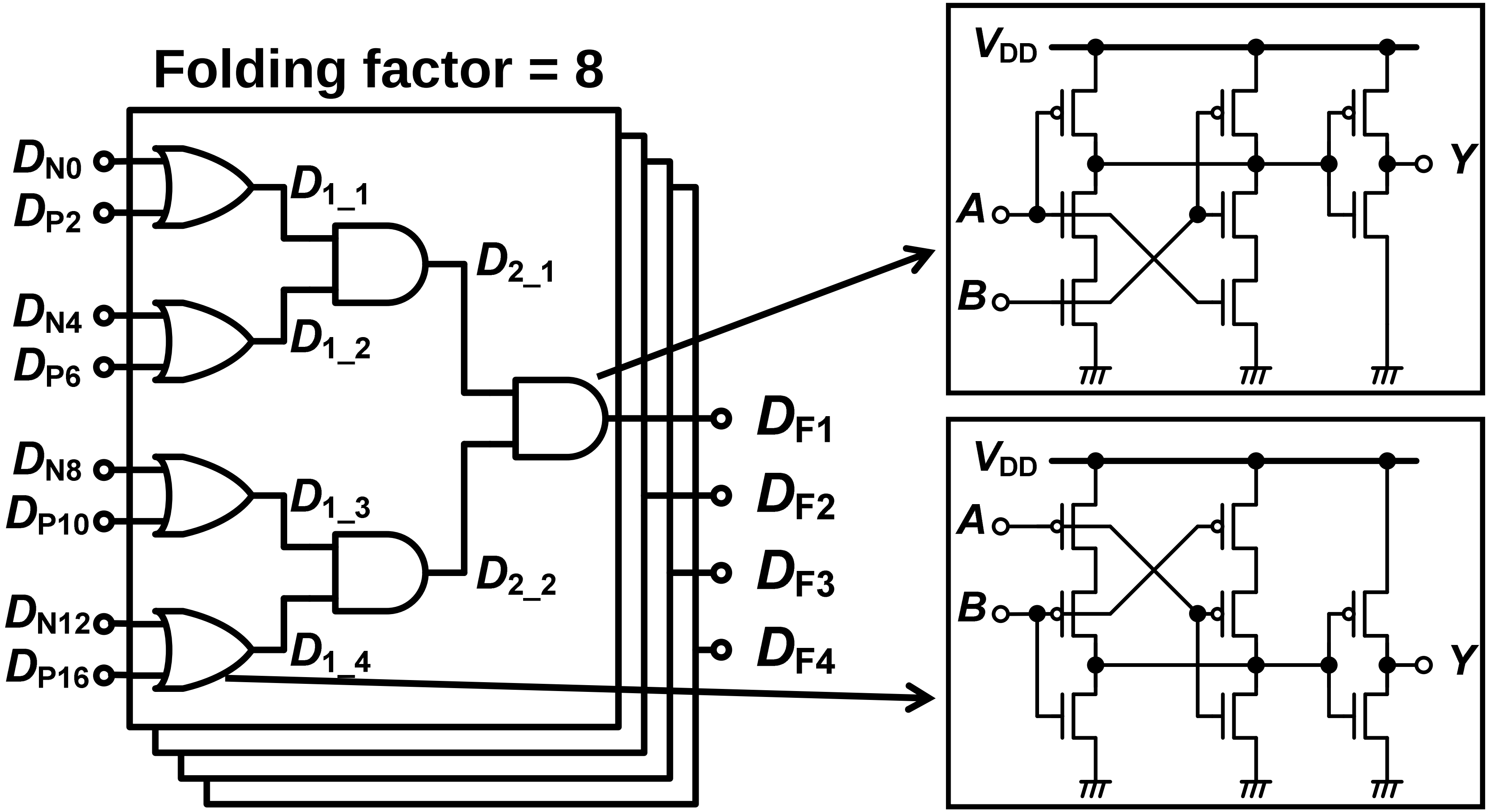
Time-Based-Folding

Valley fold ⇒ AND gate



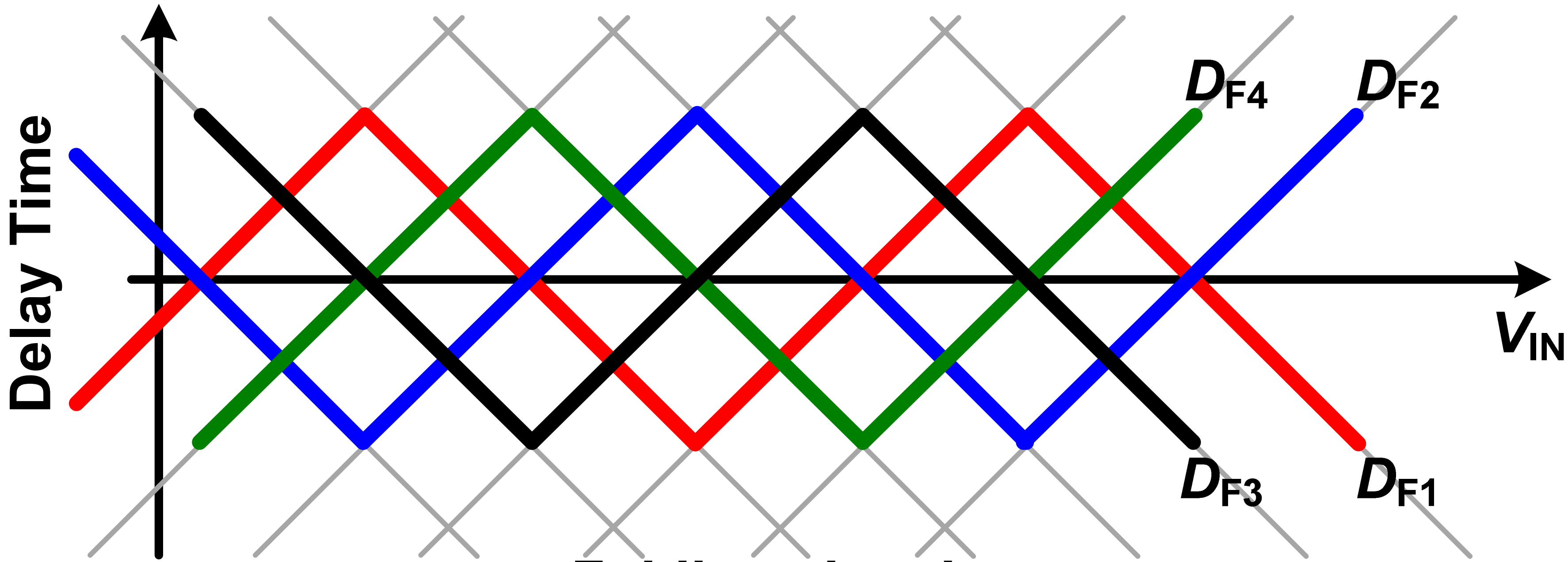
TF Circuit Implementation

Symmetrical input logic cells are used for realizing same transition time.



TF output for interpolation

Time-based folder outputs four signals to interpolate in the fine SR latches.



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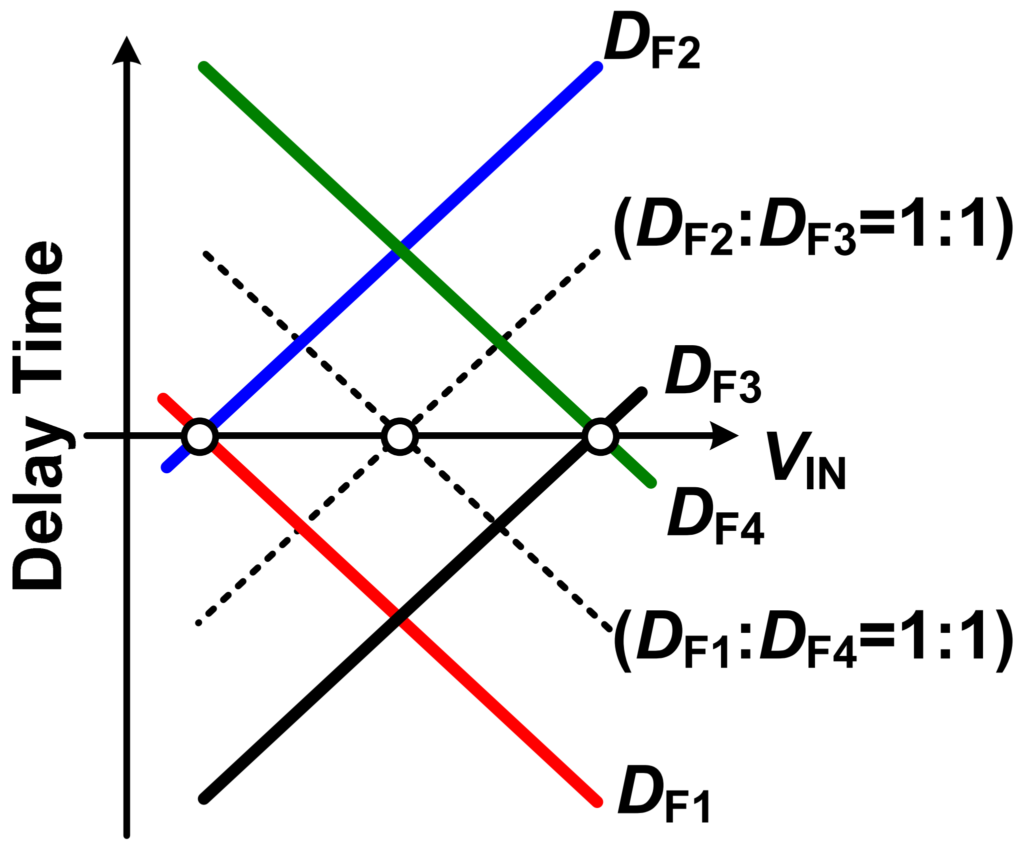

TF output for interpolation

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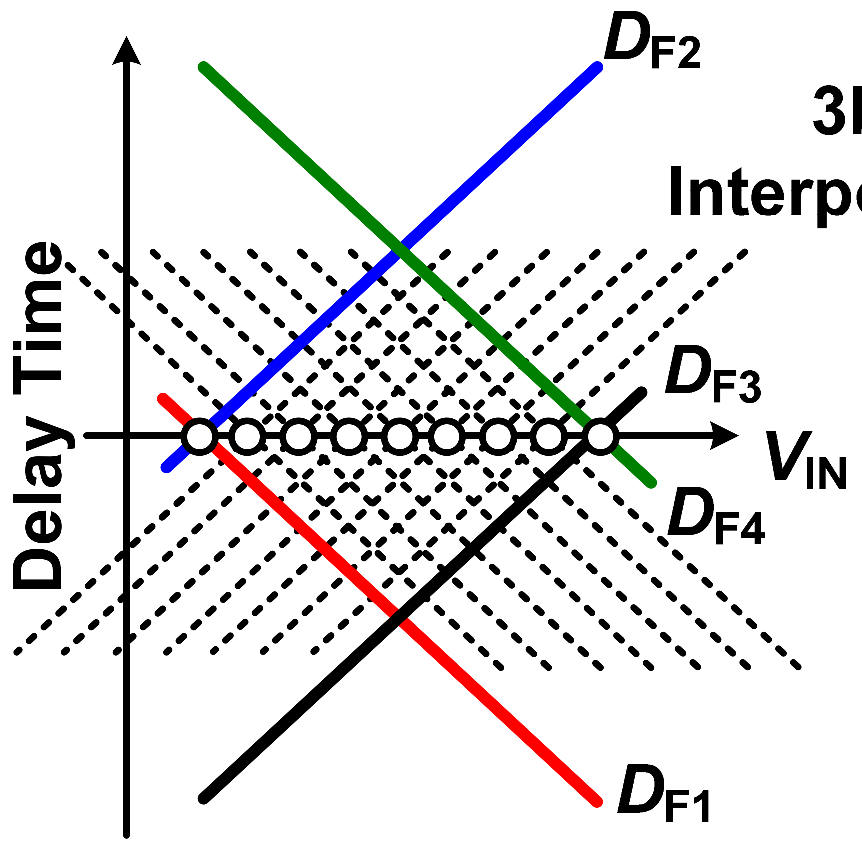
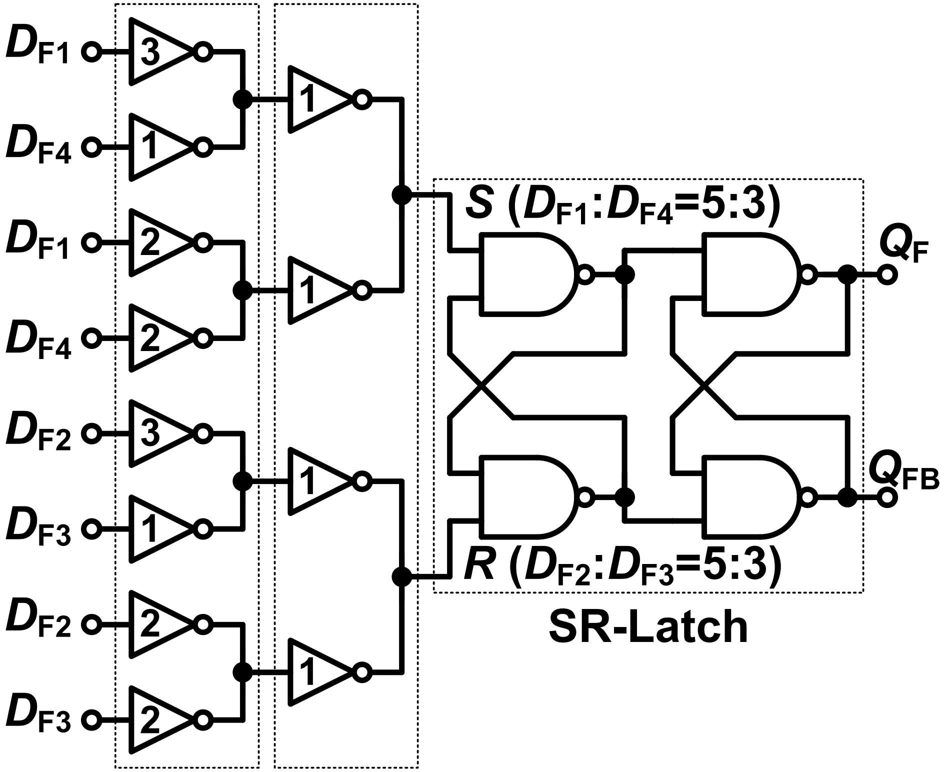
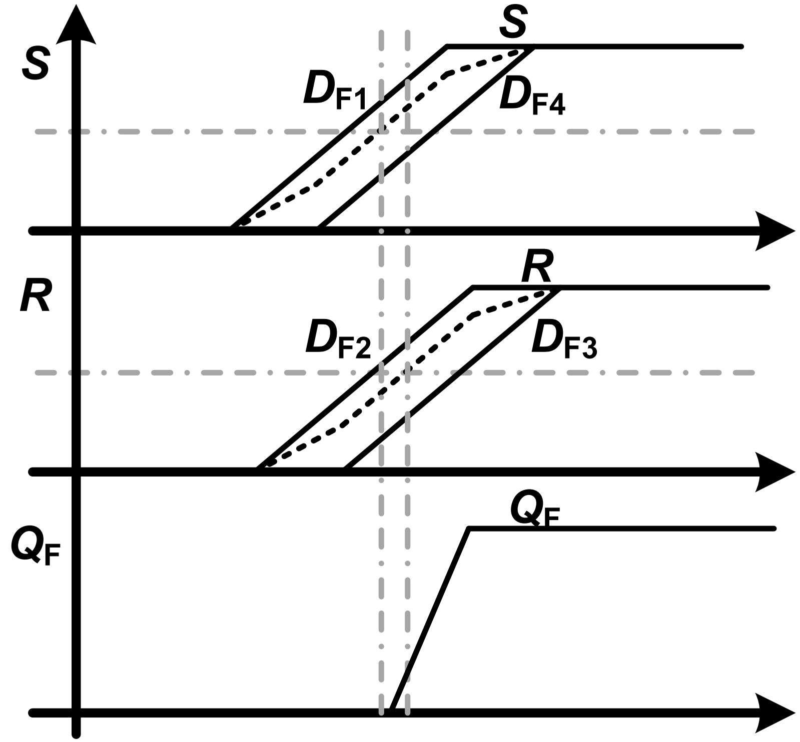


Interpolated SR Latch

Gate weighted inverter realizes interpolated signal [6]

⇒No need of reference signal in fine SR latches.





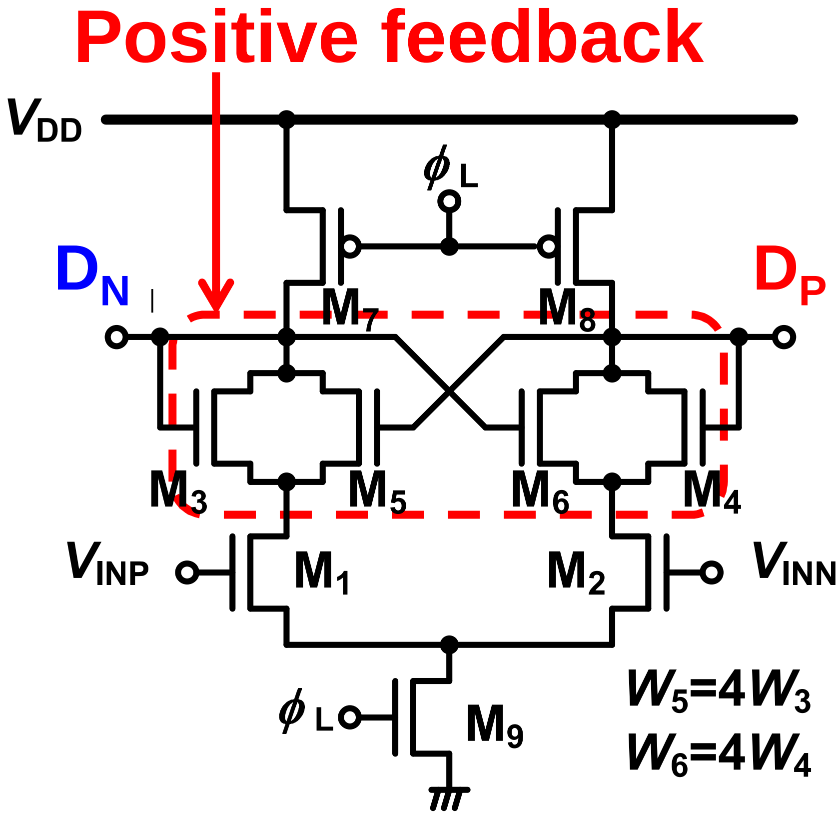
SR-Latch response in the case of interpolation ratio of 5:3

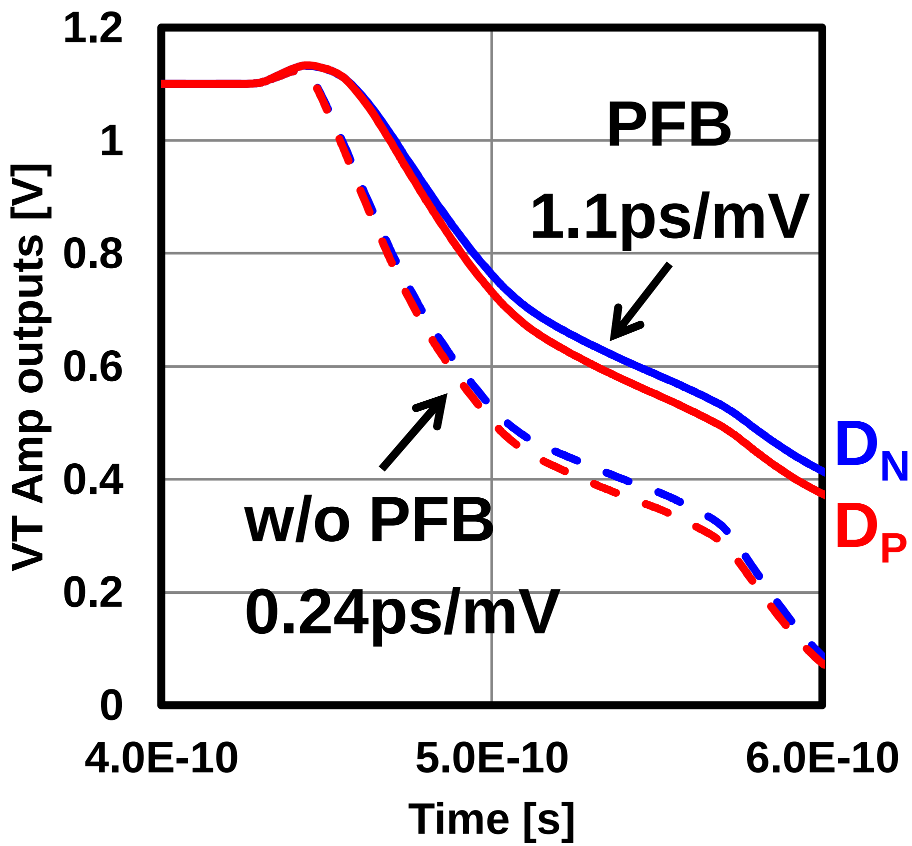
[6] D. Miyashita, *et al*., VLSI symp. 2011

Voltage-to-Time Amplifier

PFB can increase the gain by about 4 times.

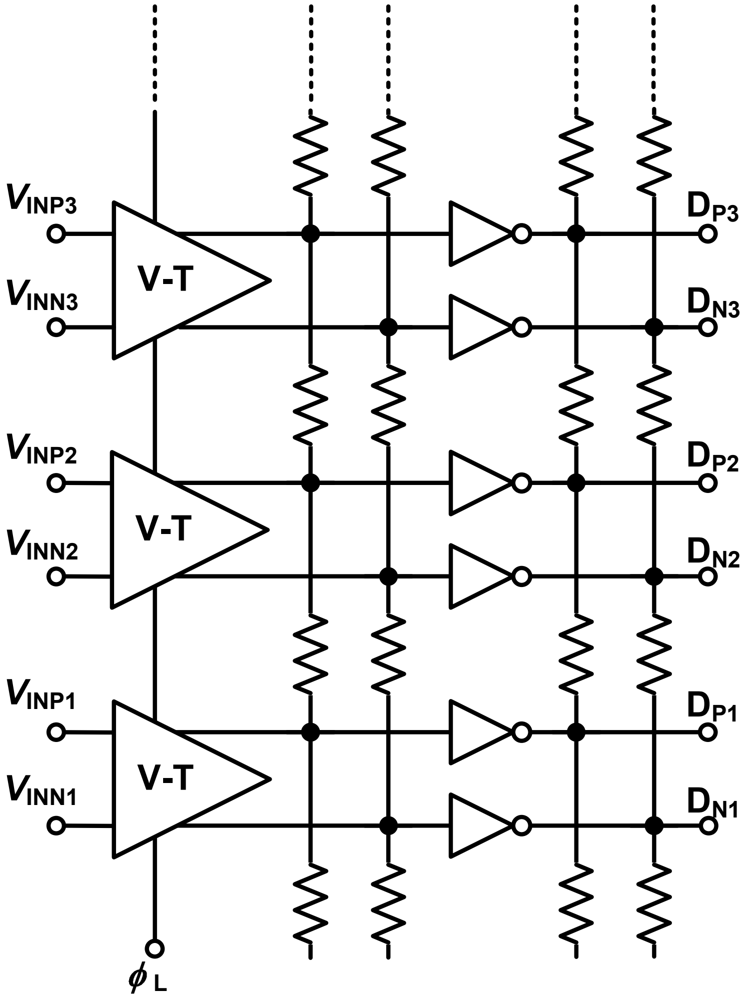
⇒No need calibration in coarse and fine Latches.



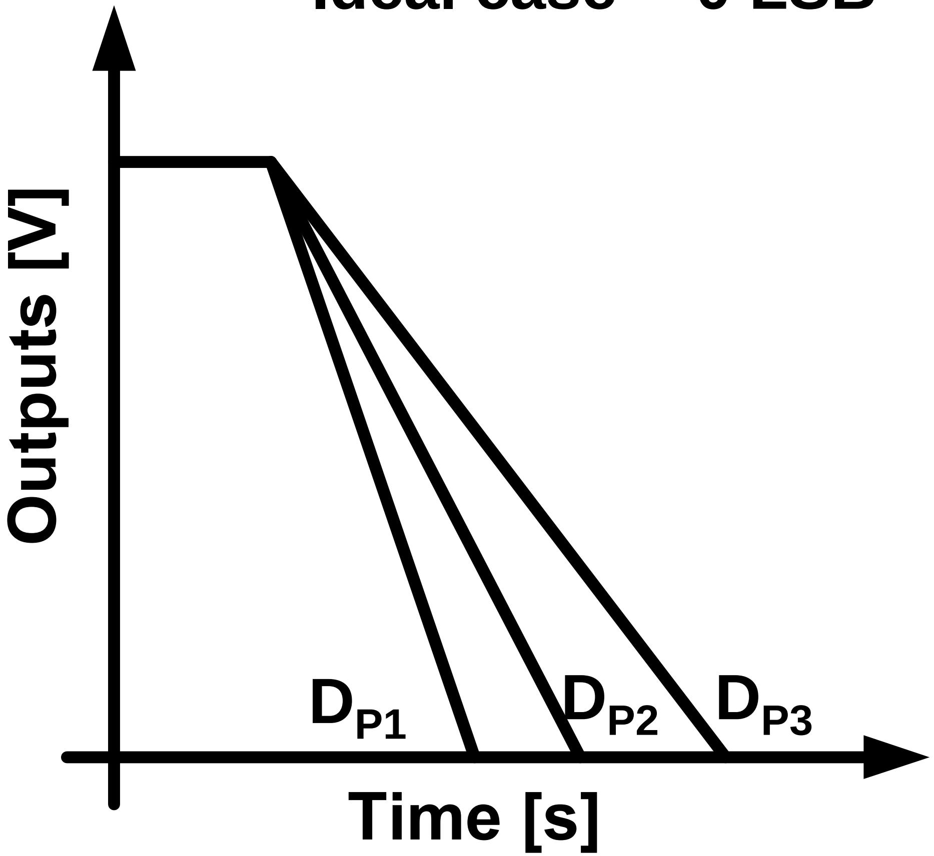


Resistively Averaged VT Amps

Resistive averaging reduces the mismatch voltage.



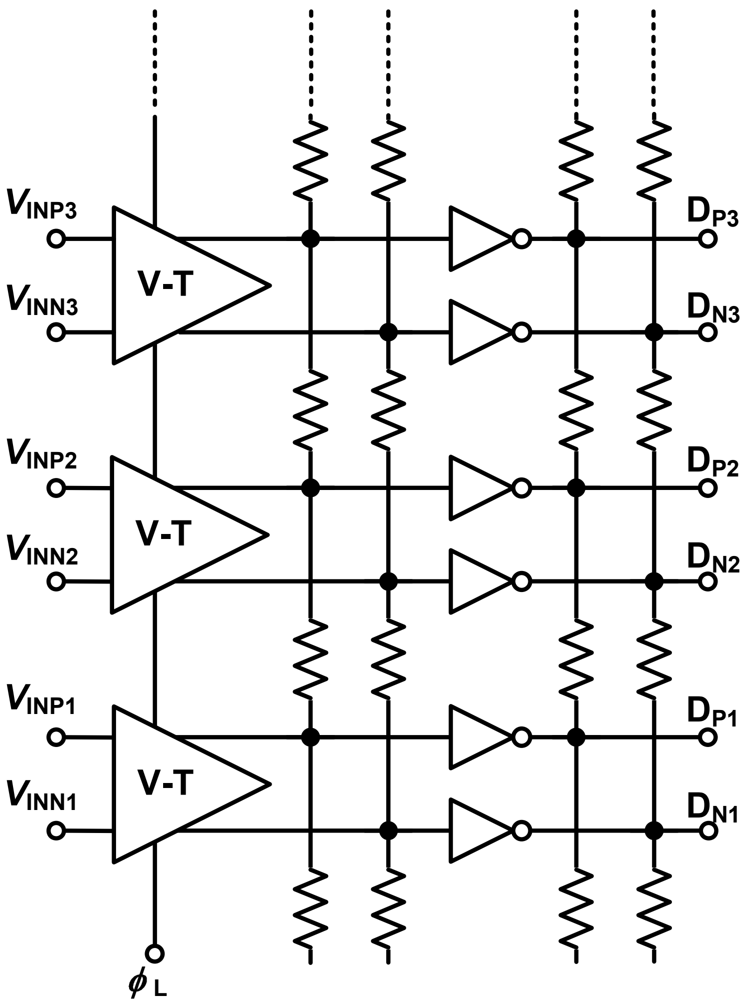
	DNL(σ)
Ideal case	0 LSB

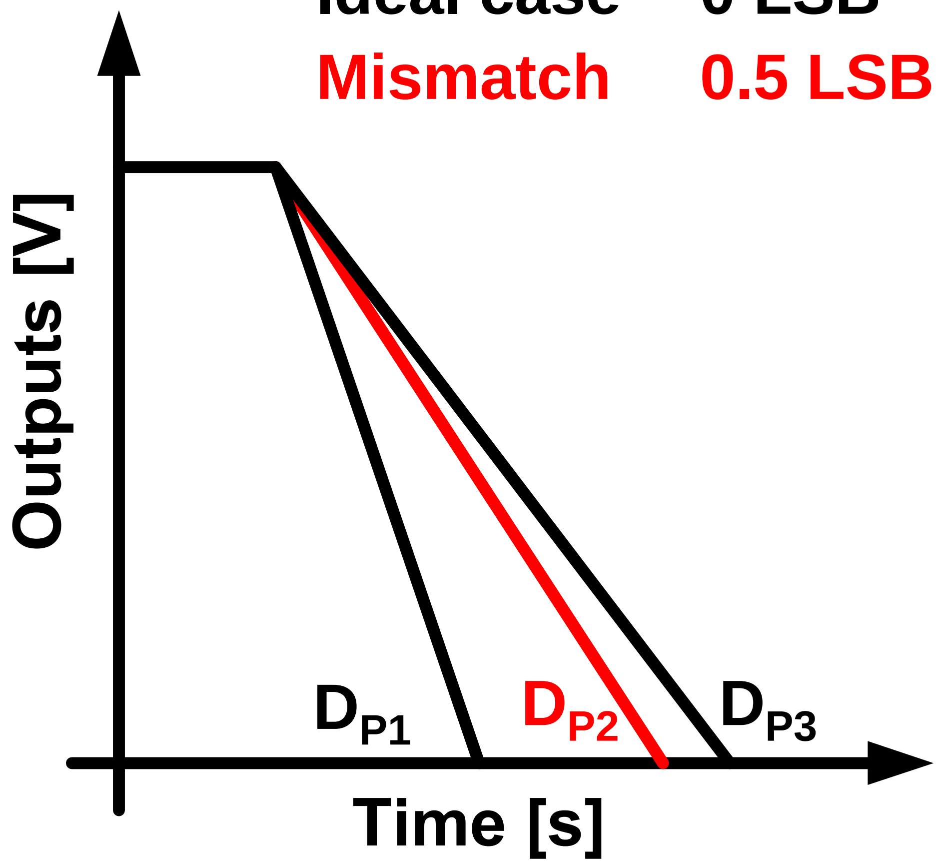


Resistively Averaged VT Amps

Resistive averaging reduces the mismatch voltage.

	DNL(σ)
Ideal case	0 LSB
Mismatch	0.5 LSB





Resistively Averaged VT Amps

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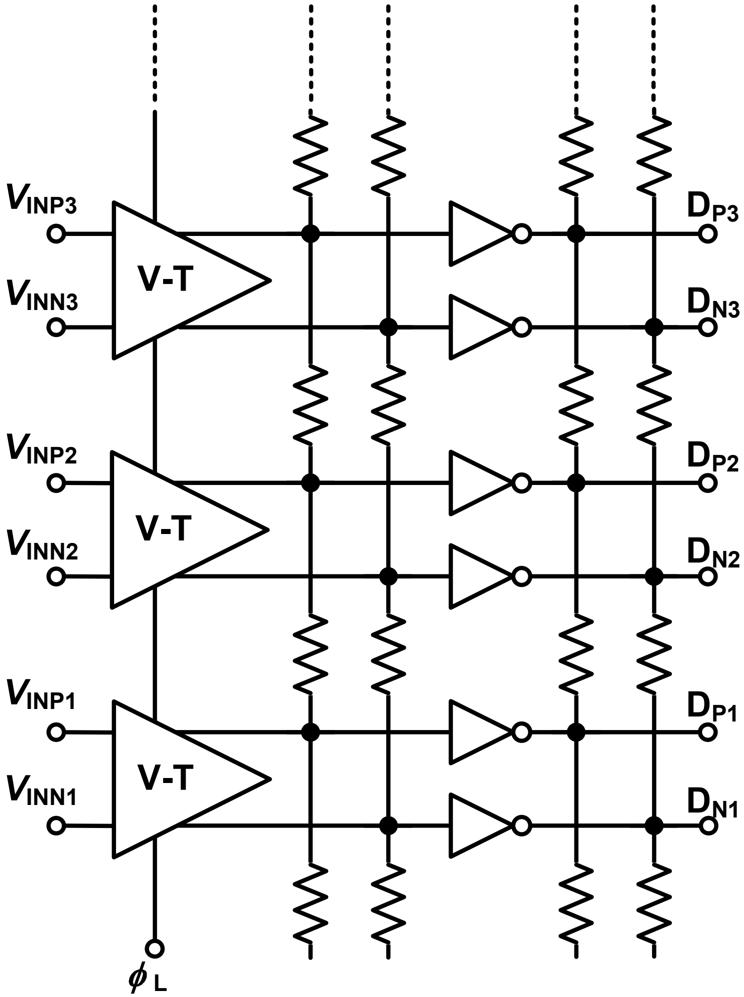
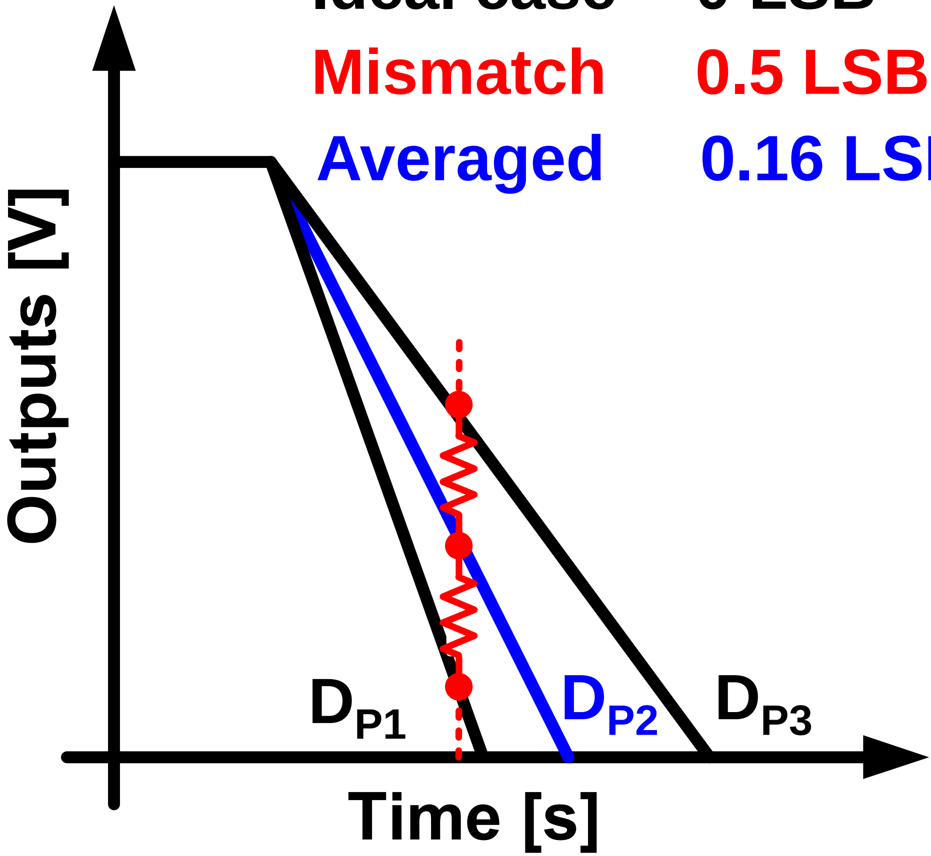
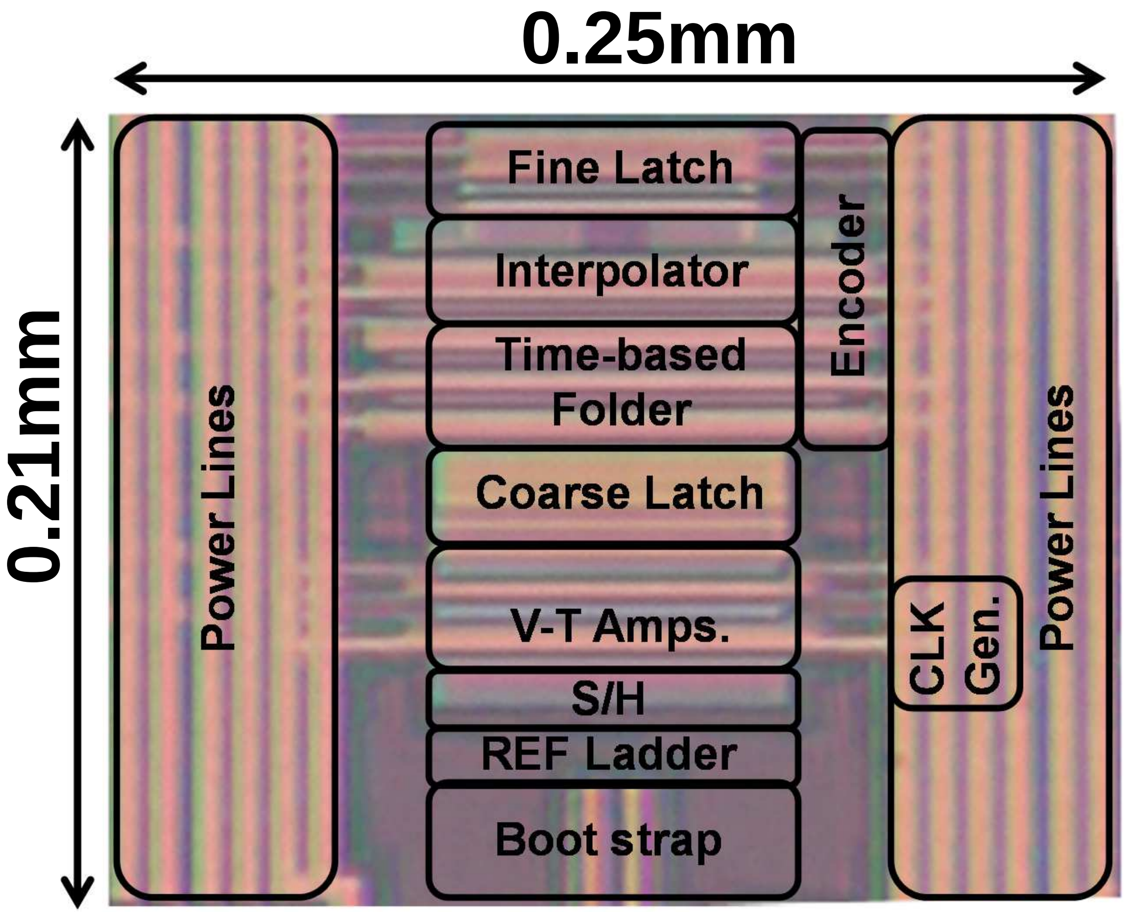


	DNL(σ)
Ideal case	0 LSB
Mismatch	0.5 LSB
Averaged	0.16 LSB

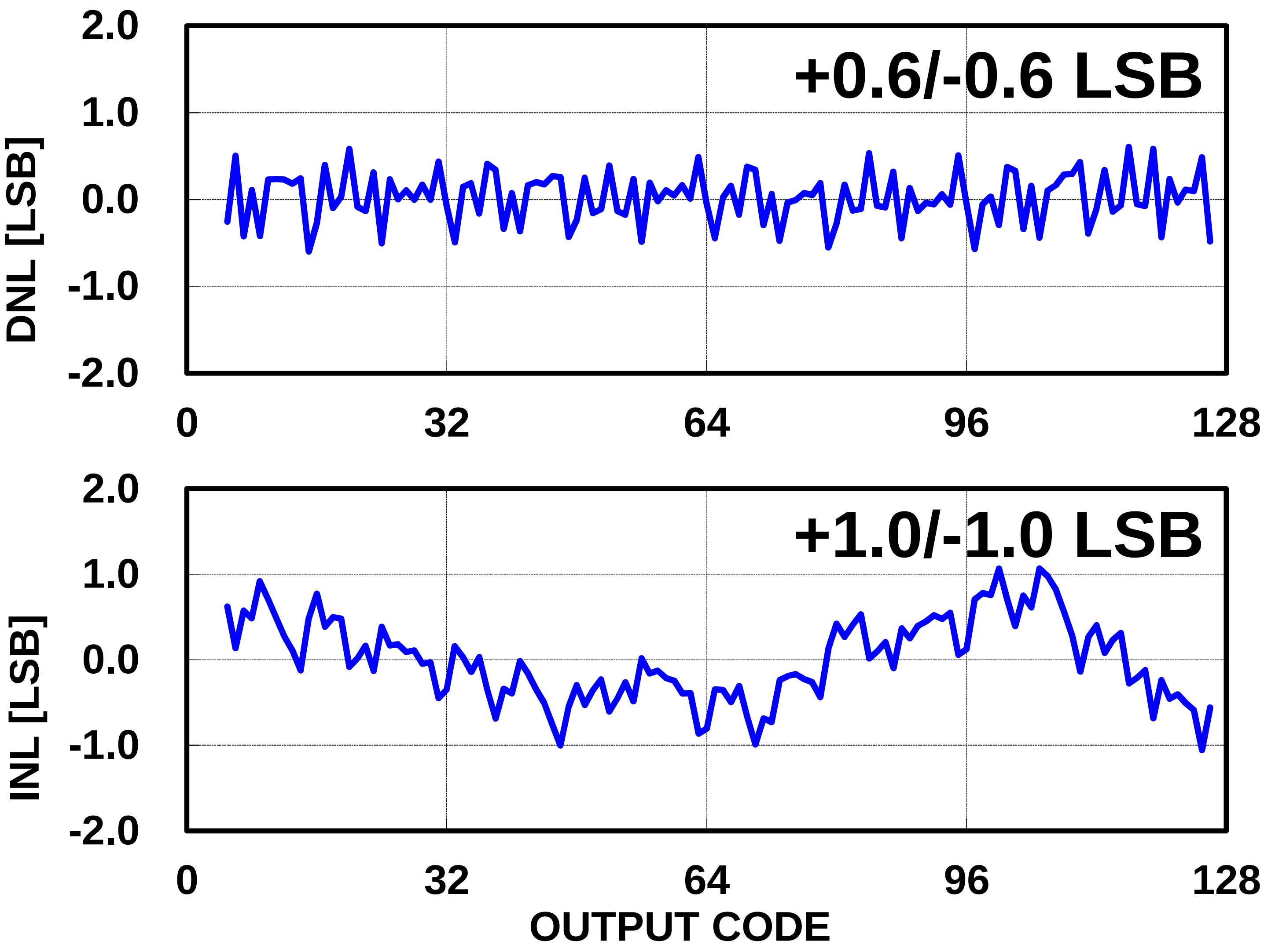


Chip photo

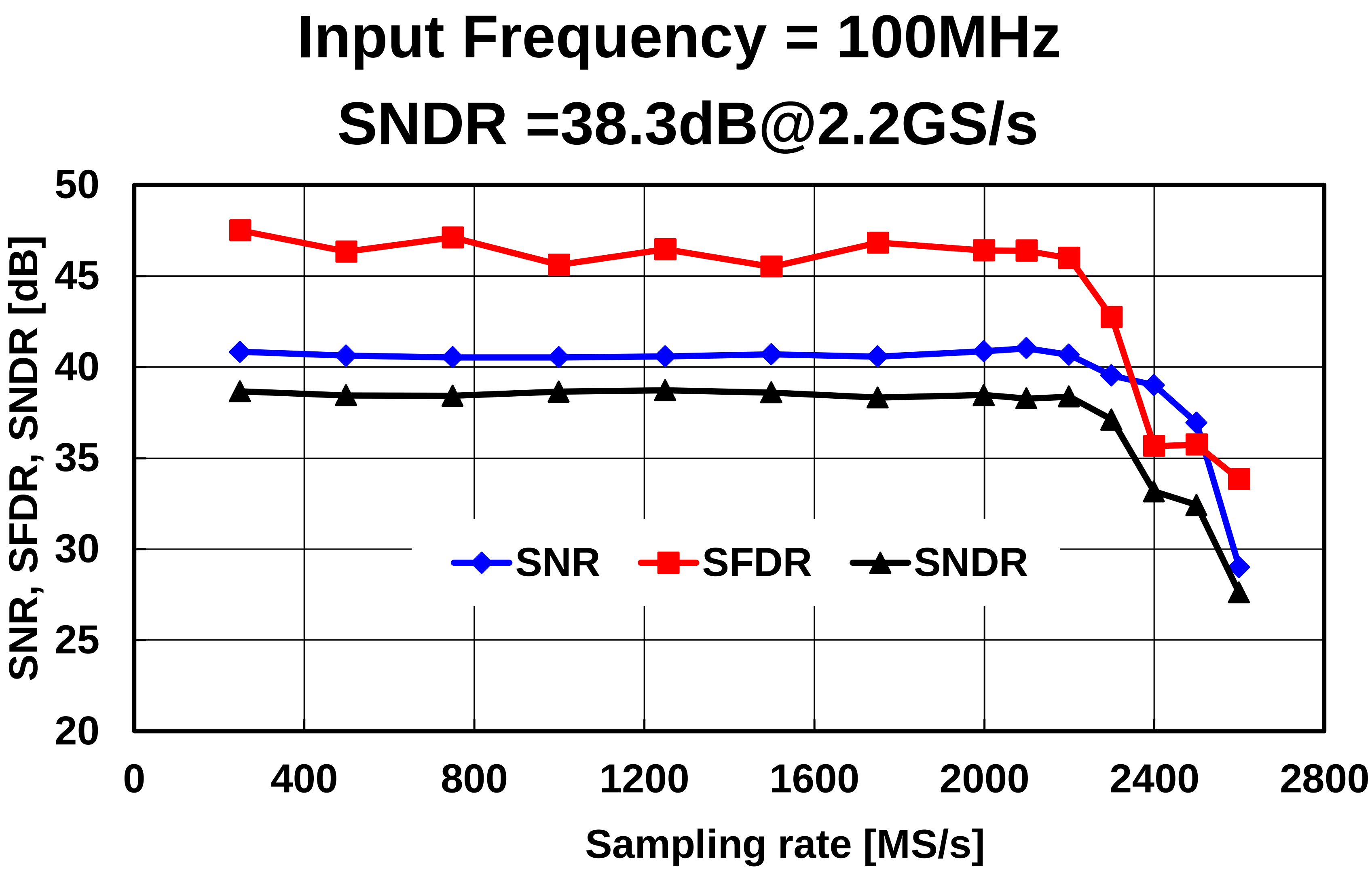
- 40nm LP 8M1P CMOS technology
- Chip area of $0.052mm^2$



Measured DNL, INL



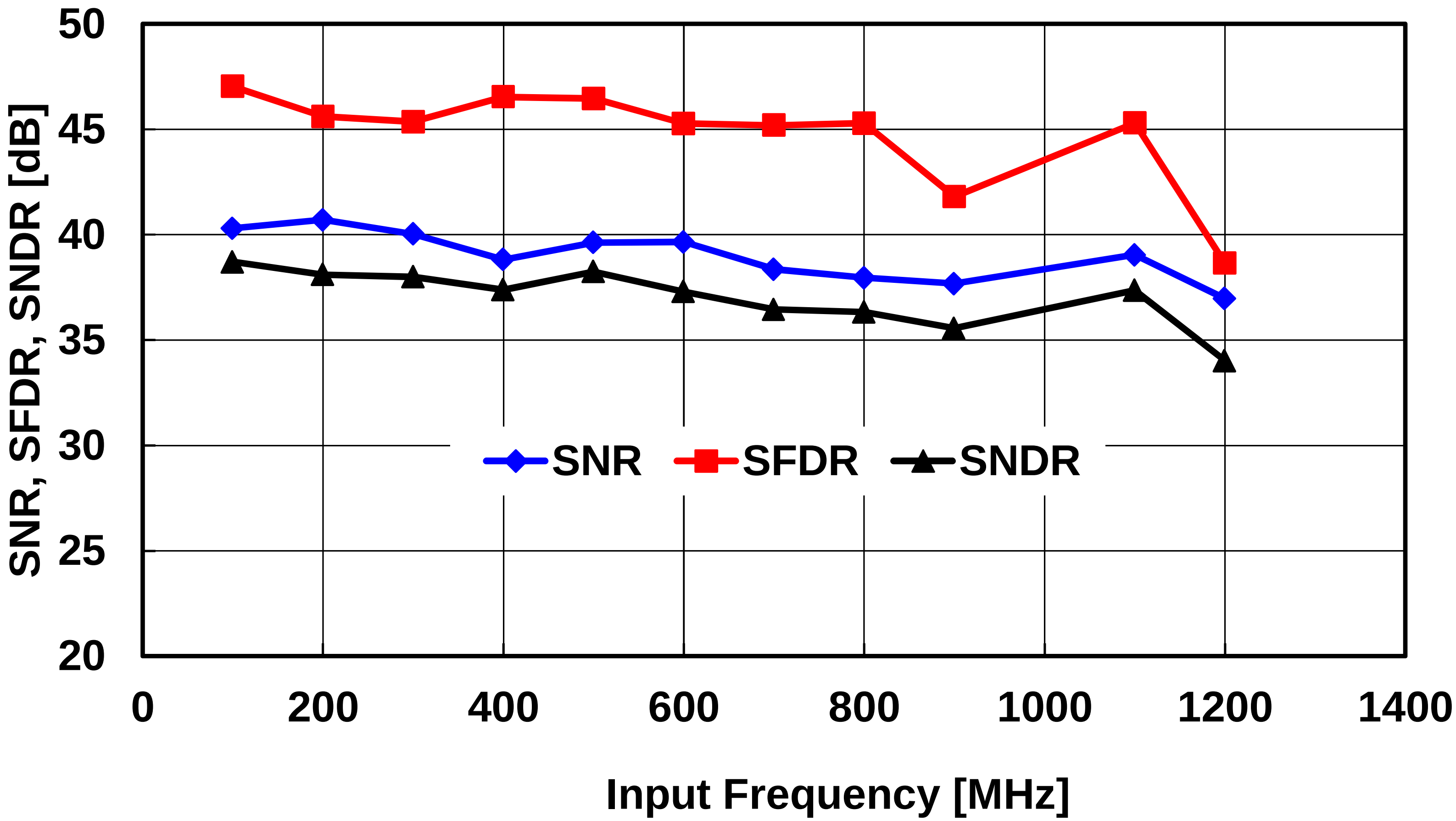
Sampling rate vs. SNDR



Input Frequency vs. SNDR

Sampling rate = 2.2GS/s

SNDR =37.4dB@1.1GHz

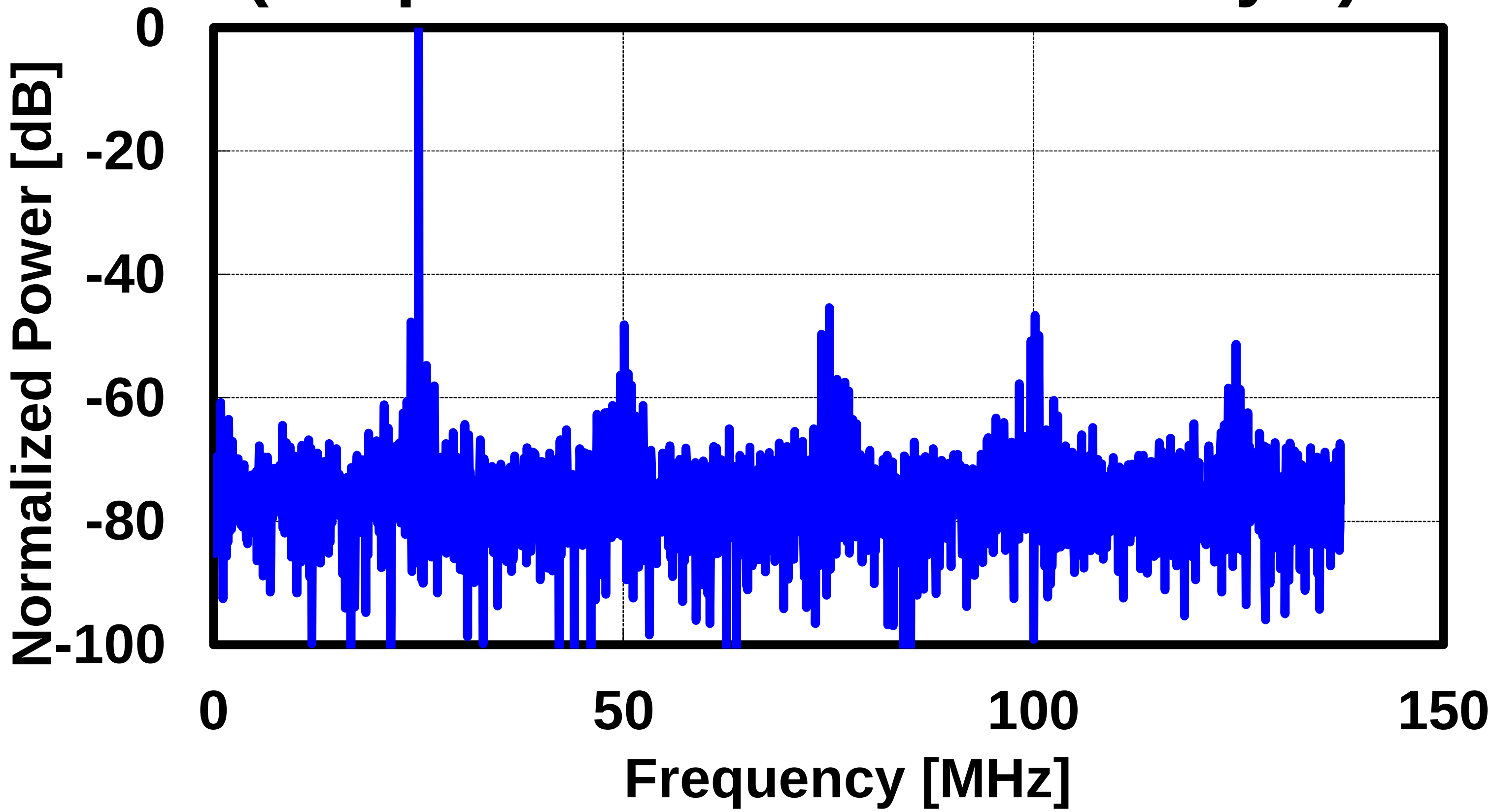


Measured Spectrum

Sampling rate = 2.2GS/s

Input frequency = 800MHz

(Output code is decimated by 8)



Performance Summary

- **The highest SNDR in Flash ADCs exceeding 2 GS/s**
- **No need of calibration**

	ISSCC 2008 [3]	VLSI 2012 [8]	VLSI 2013 [9]	This work
Technology	90nm	40nm	32nm SOI	40nm LP
Resolution [bit]	5	6	6	7
Power Supply [V]	1	1.1	0.85	1.1
Sampling Frequency [GS/s]	1.75	3	5	2.2
Power Consumption [mW]	2.2	11	8.5	27.4
SNDR @Nyquist [dB]	27.6	33.1	30.9	37.4*
FoMw [fJ/conv.-step]	64.5	99.3	59.4	210
FoMs [dB]	143.5	144.4	145.6	143.3
Core area [mm^2]	0.0165	0.021	0.02	0.052
Calibration	Off chip	Foreground	Off chip	No need

*3.3mW for reference ladder, 19.4mW for analog and 4.7mW for digital

Conclusion

- Time-based-folding architecture
  - ☺ More suitable for future process
  - ☺ No static current
- Voltage-to-time amplifier
  - Dynamic amplifier with resistive averaging
    - ☺ No static current
    - ☺ 1/3 offset voltage, no need of calibration
- A 7b 2.2GS/s 27.4mW Folding Flash ADC is realized

Acknowledgement

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References

[1] Y. Nakajima, *et al*., "A Background Self-Calibrated 6b 2.7GS/s ADC With Cascade-Calibrated Folding-Interpolating Architecture," *IEEE J. Solid-State Circuits*, vol. 45, pp. 707-718, Apr. 2010.

[2] T. Yamase, *et al*., "A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-bit/stage Folding Converter Architecture," *Symp. VLSI Circuits*, pp. 124-125, June 2011.

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[5] K. Makigawa, *et al*., "A 7bit 800Msps 120mW Folding and Interpolation ADC Using a Mixed-Averaging Scheme," *Symp. VLSI Circuits*, pp. 124-125, June 2006.

[6] D. Miyashita, *et al*., "A -104dBc/Hz In-Band Phase Noise 3GHz All Digital PLL with Phase Interpolation Based Hierarchical Time to Digital Convertor," *Symp. VLSI Circuits*, pp. 112-113, June 2011.

[7] B. Murmann, "ADC performance survey 1997-2013," [Online]. Available: http://www.stanford.edu/˜murmann/adcsurvey.html.

[8] Y. -S Shu, "A 6b 3GS/s 11mW Fully Dynamic ADC in 40nm CMOS with Reduced Number of comparators," *Symp. VLSI Circuits*, pp. 26-27, June 2012.

[9] V. H. -C. Chen and L. Pileggi, "An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI," *Symp. VLSI Circuits*, pp. 264-265, June 2013.