Anatomy of Innovation: Bug or Feature?

"Interpolation techniques" in ADCs

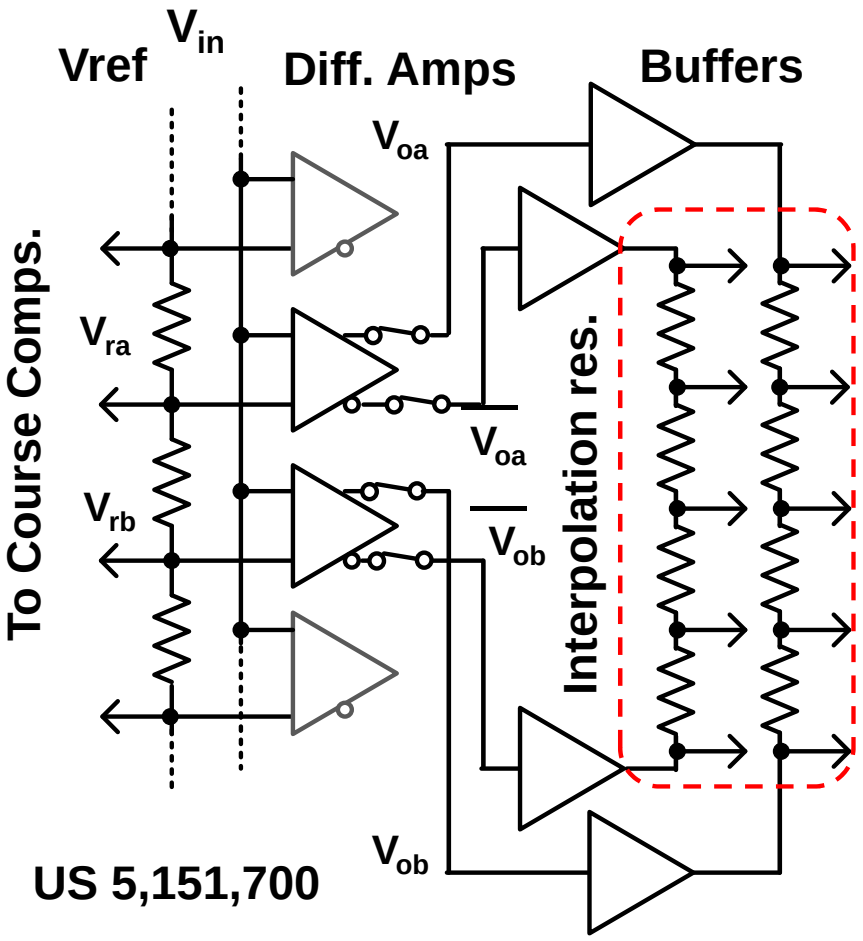
Akira Matsuzawa

Tokyo Institute of Technology

Bug triggered to find the “interpolation”

Bug!!

I have **failed** to develop a sub-ranging ADC.
I had only **Three weeks** from idea to tape-out for the new ADC.
I founded the most **robust** ADC architecture; “Interpolation”

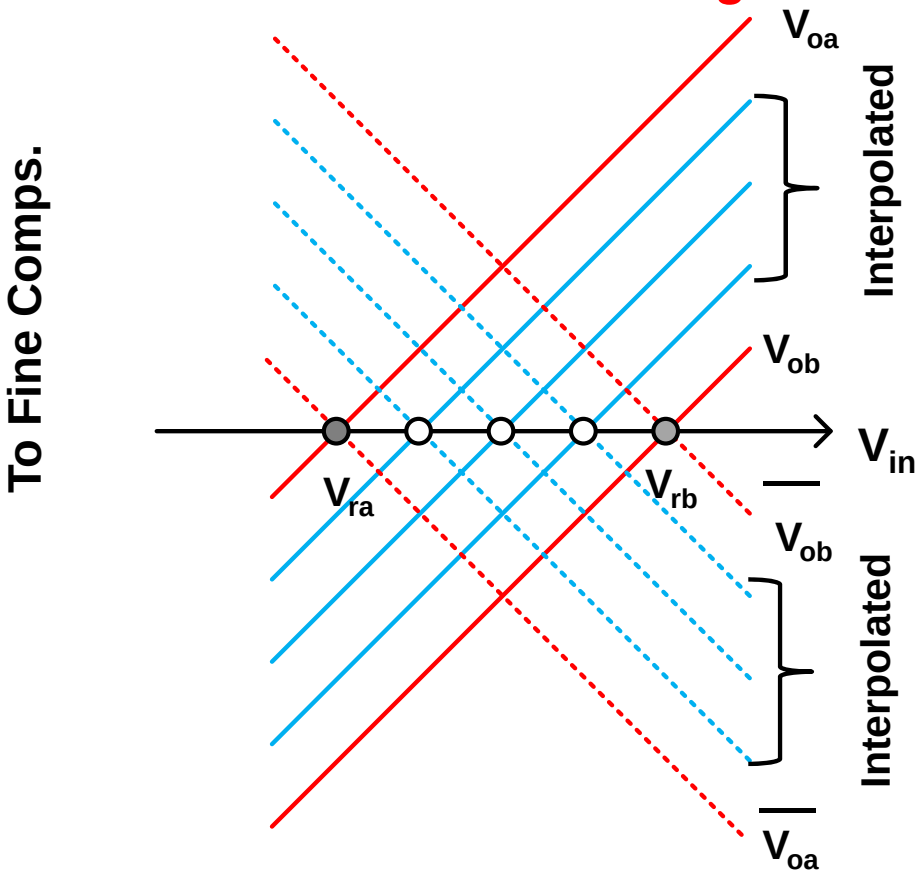


US 5,151,700

A. Matsuzawa, et al., “A 10b 30MHz Two-Step Parallel BiCMOS ADC with Internal S/H,” ISSCC, pp.162-163, Feb. 1990.

Compare the two signals (Reference is involved)

Free from the course-fine gain matching



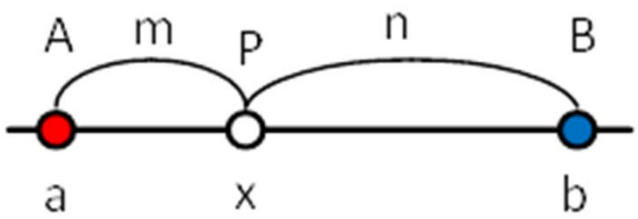
The original interpolation technique in ADC must be
R. E. J. Van de Grift, et al., J.S.C. pp. 944-953, Dec. 1987.

Feature reveals the essence of “interpolation”

The interpolation is not the equal division between the two voltages, but the internal division; weight and sum of the two values.

Many implementation methods are possible

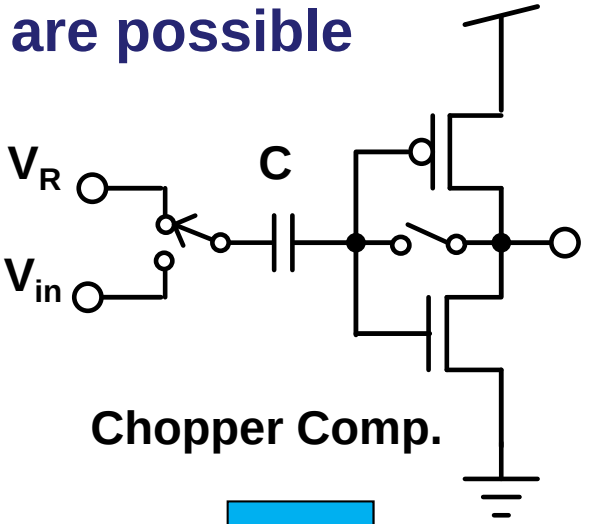
Internal division method



Essence

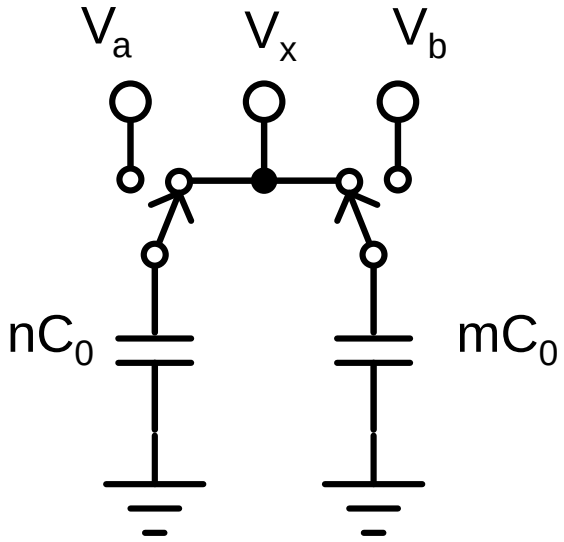
weight and sum

$$x = \frac{na + mb}{m + n}$$

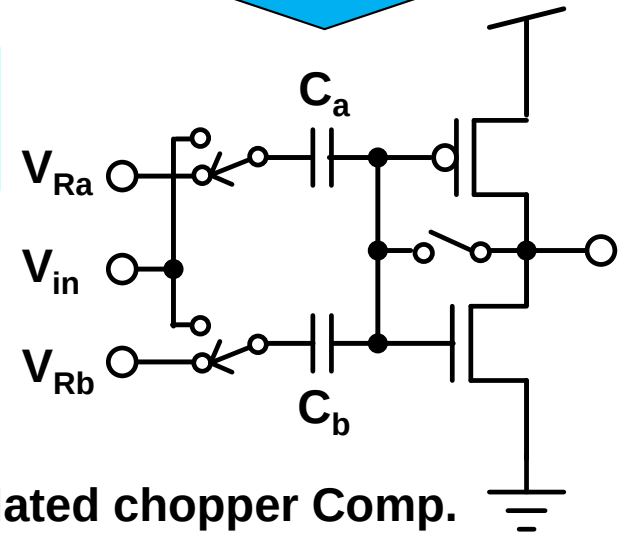


Chopper Comp.

Capacitive method is possible



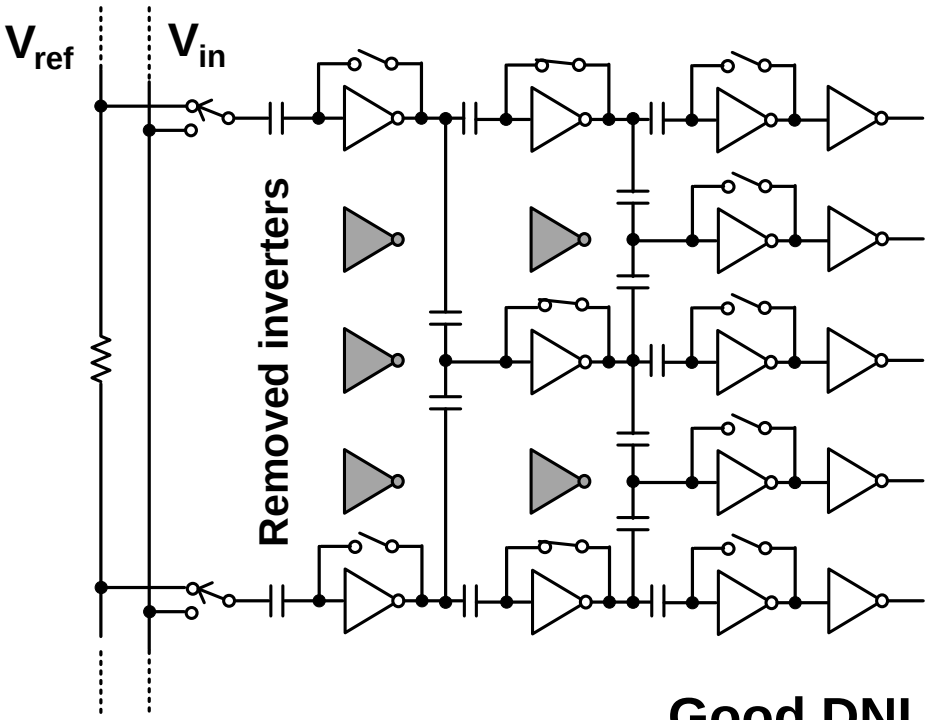
$$V_x = \frac{nV_a + mV_b}{m + n}$$



Interpolated chopper Comp.

Invention of the capacitive interpolation

An ultra-Low FoM CMOS 10b ADC (1/8 to others) has been realized.

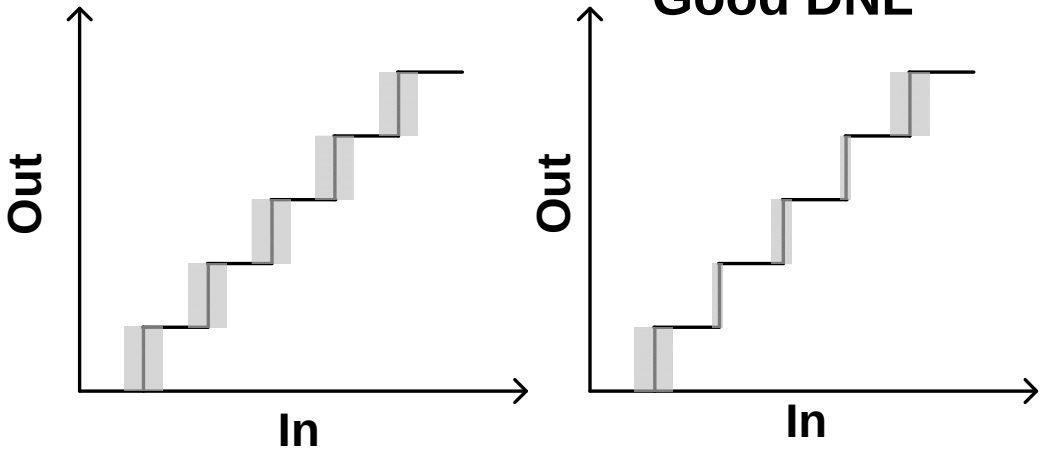


Capacitive interpolation
Chopper comparator
Pipelining

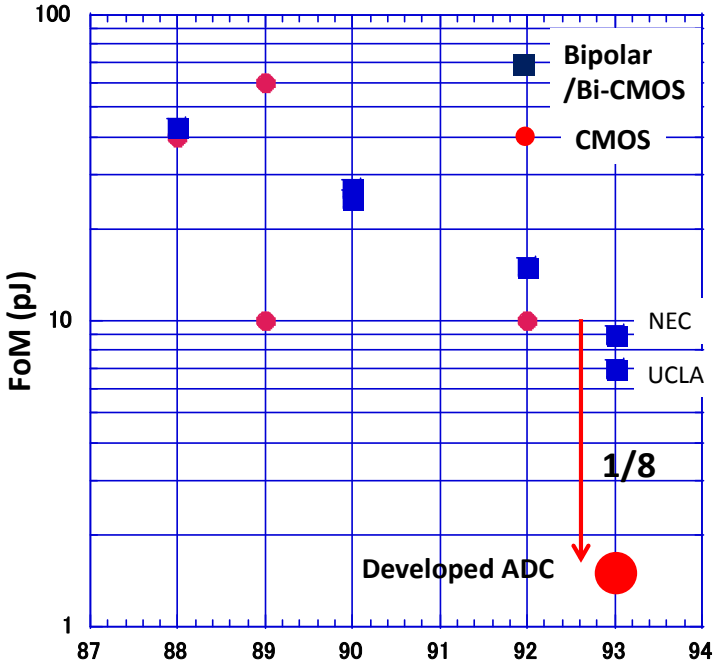
K. Kusumoto, A. Matsuzawa, K. Murata, "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," J.S.C., pp.1200-1206, Dec. 1993. ISSCC 1993.

US 5,465,093

Good DNL

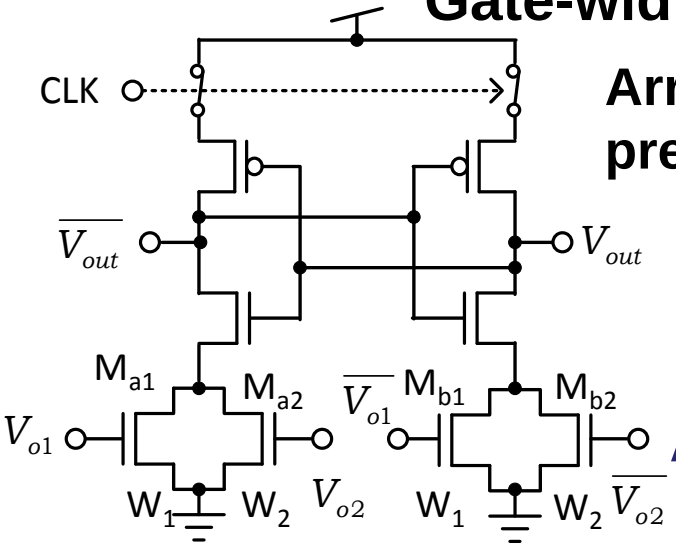


FoM of 10b ADC



Gate-width weighted interpolation

Gate-width can be used for the weighting



Array of gate-width weighted dynamic comparators with preamplifiers realizes high speed and low power ADC

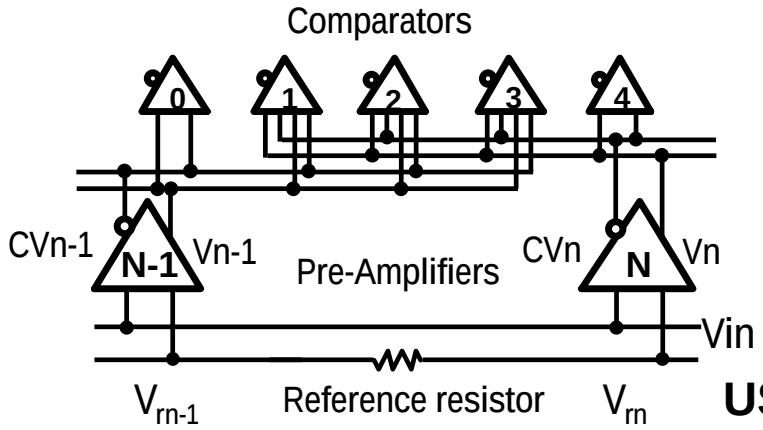
Effective threshold voltage condition

$$W_1V_{o1} + W_2V_{o2} > W_1\overline{V_{o1}} + W_2\overline{V_{o2}}$$

An ultra-low power (1/10 to others) and high speed ADC

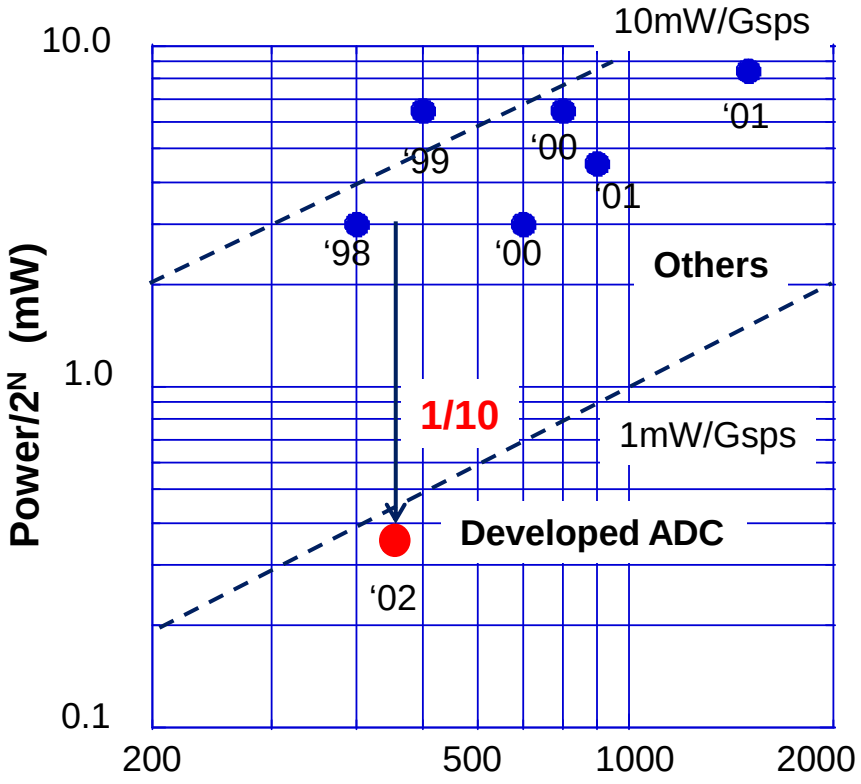
T. B. Cho and P. R. Gray, "A 10b 20 Msample/s, 35 mW Pipelined A/D Converter," J.S.C, pp166-172, March 1995.

But, no use for the interpolation



US 6,707,413 B2

K. Sushihara, A. Matsuzawa, "A 7b 450MSample/s 50mW CMOS ADC in 0.3mm², " ISSCC 2002.



Position statement

- **Bugs are always the triggers for innovative ideas.**
  - **unexpected bad result, a failure of development, a high pressure for development schedule, and tough performance targets**

- **The innovative ideas are created from the logical thinking. Seeking the essence of technology leads us to the novel view.**
  - **What is an analog to digital conversion?**
  - **Why a reference voltage is needed?**
  - **What is an interpolation?**

- **High level abstraction of the system, such as mathematical model sometimes reveals the essence. If we can find it, we can create many implementation methods easily.**

- **The other important factor is a sense of beauty.**
  I believe an essential feature is always beautiful.