A 0.0066mm^2 780μW Fully Synthesizable PLL with a Current Output DAC and an Interpolative Phase-Coupled Oscillator using Edge Injection Technique

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Tokyo Institute of Technology, Japan

Outline

- Motivation
- Concept of synthesizable analog circuits
- Synthesizable PLL
  - Interpolative phase-coupled oscillator
  - Standard-cell I-DAC
  - Standard-cell varactor
  - Edge injection
- Measurement Results
- Conclusion

Motivation

- **Synthesizable analog circuits**
  - **Portability**
  - **Scalability**
  - **Layout issues above 20nm**
- **Potential applications**
  - **PLL**
  - **ADC, DAC**
  - **Wireless/Wireline transceivers**

Synthesizable Analog Circuits

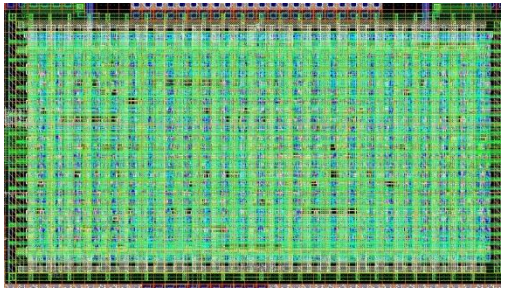
HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

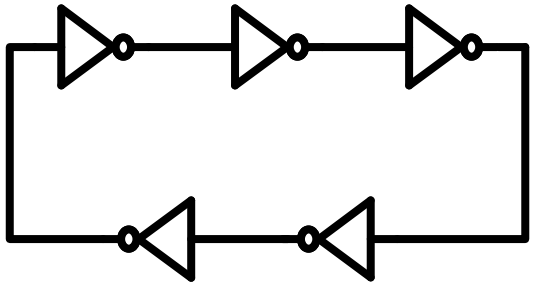
Commercial P&R tools…

GDS

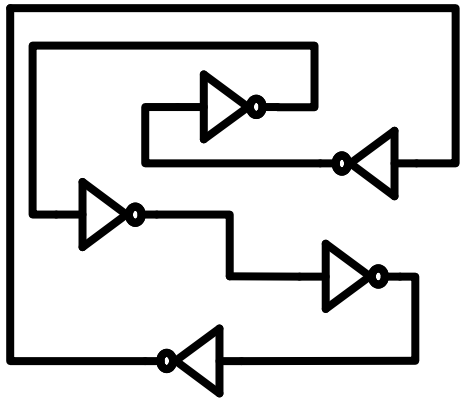


with a standard-cell library
without any custom-designed cells
without manual placement

Issue: Layout Uncertainty



Ideal placement



Actual placement

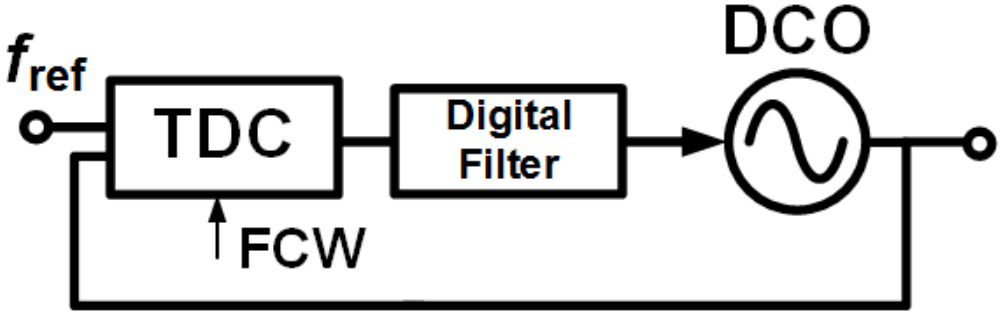
➔Unbalanced loading

No layout symmetry

A new analog-circuit architecture is required, which tolerates layout impairment/uncertainty.

Conventional All-digital PLLs

- **TDC-based architecture**



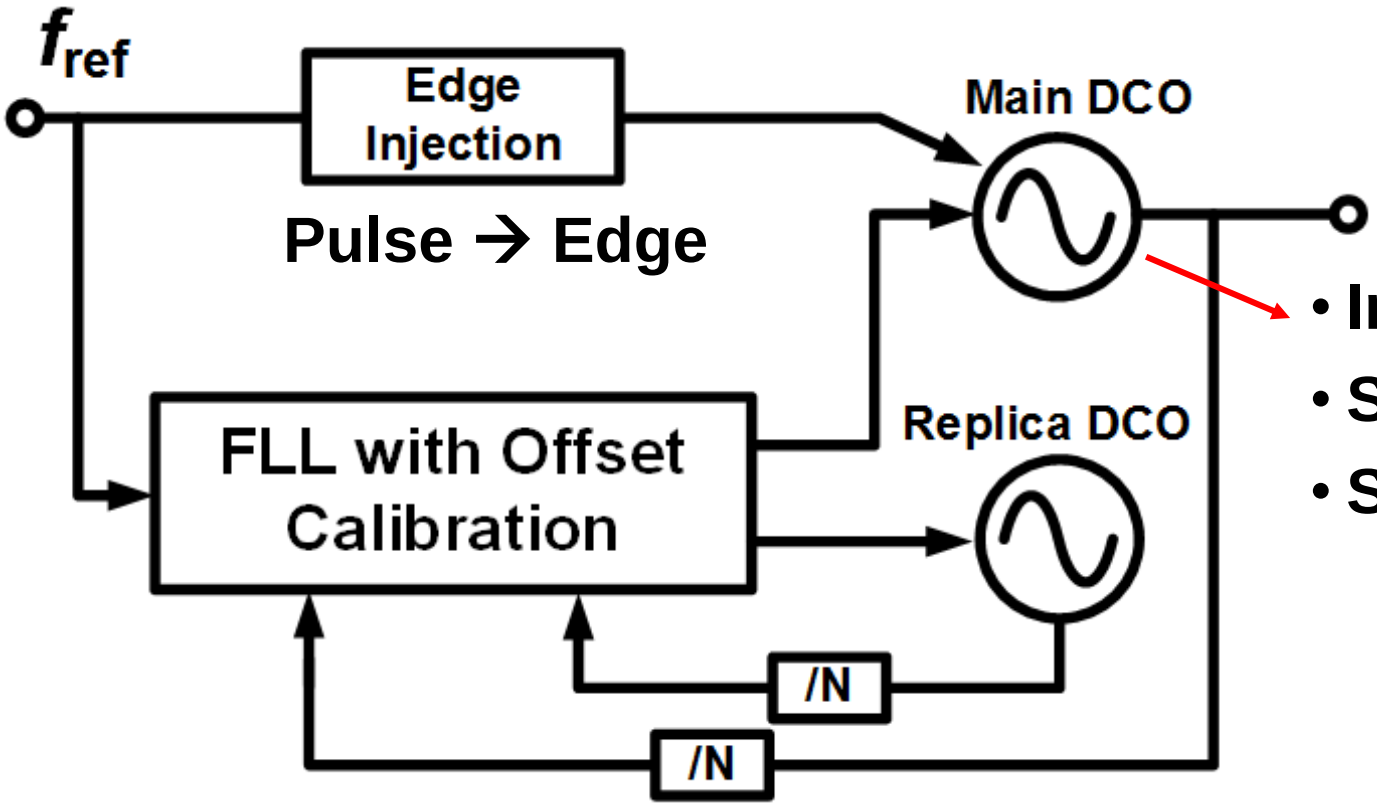
  - **The layout uncertainty degrades TDC and DCO linearity.**
  - **Poor frequency resolution by standard-cell design.**

- **Trade-off between layout integrity and jitter performance**

Proposed Synthesizable PLL

- **Injection-locking topology**
  - **Avoid TDC issues (linearity, power-resolution trade-off)**
- **Circuit techniques**
  - **Interpolative phase-coupled osc. & I-DAC**
    - **Overcome phase imbalance**
  - **A new varactor for fine resolution**
    - **Low spur level**
  - **Edge injection technique**
    - **Relax severe timing design**

TOP Block Diagram

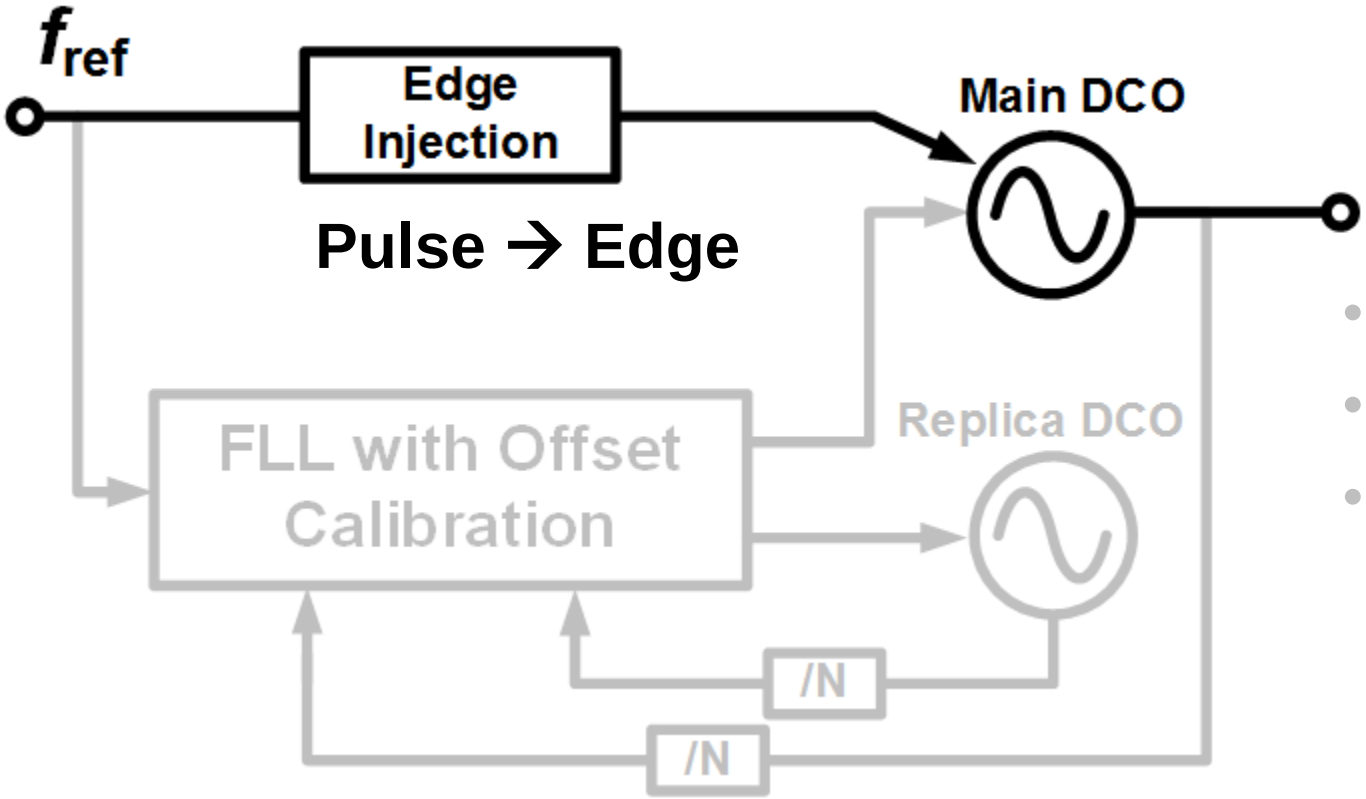


- Interpolation
- Stdcell varactor
- Stdcell I-DAC

[W. Deng, *et al.*, ISSCC 2013]

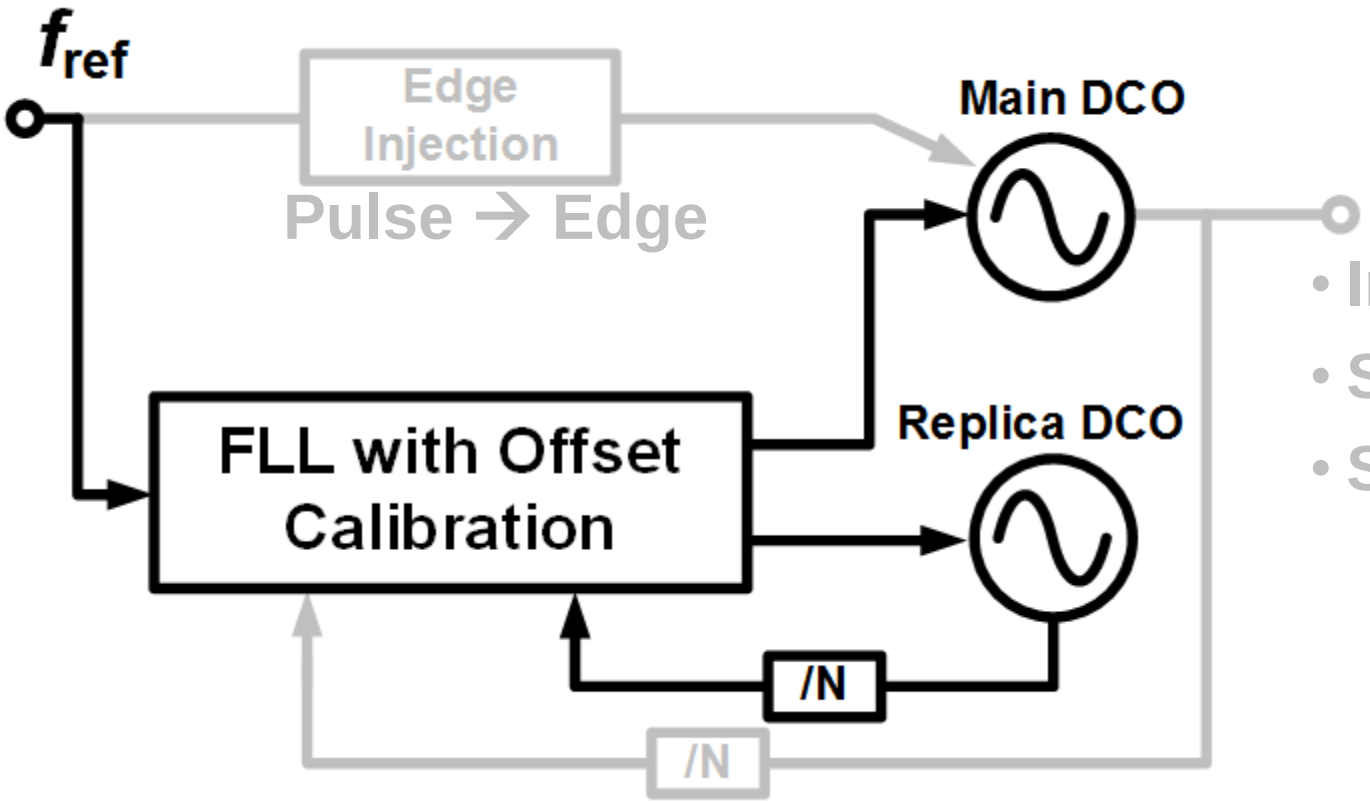
TOP Block Diagram

Feedforward phase locking



- Interpolation
- Stdcell varactor
- Stdcell I-DAC

TOP Block Diagram



- Interpolation
- Stdcell varactor
- Stdcell I-DAC

Feedback FLL for frequency tracking

[W. Deng, *et al.*, ISSCC 2013]

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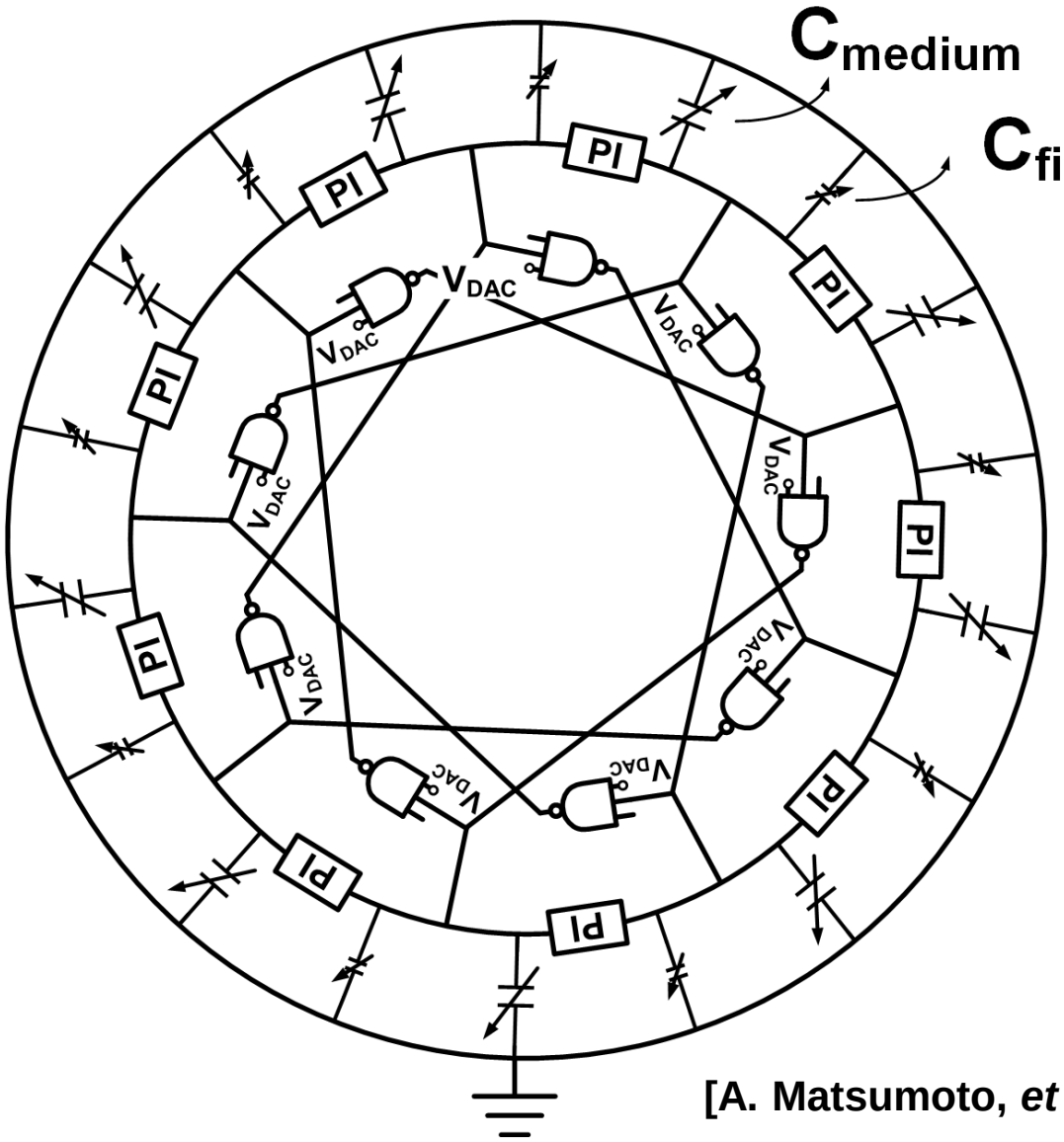
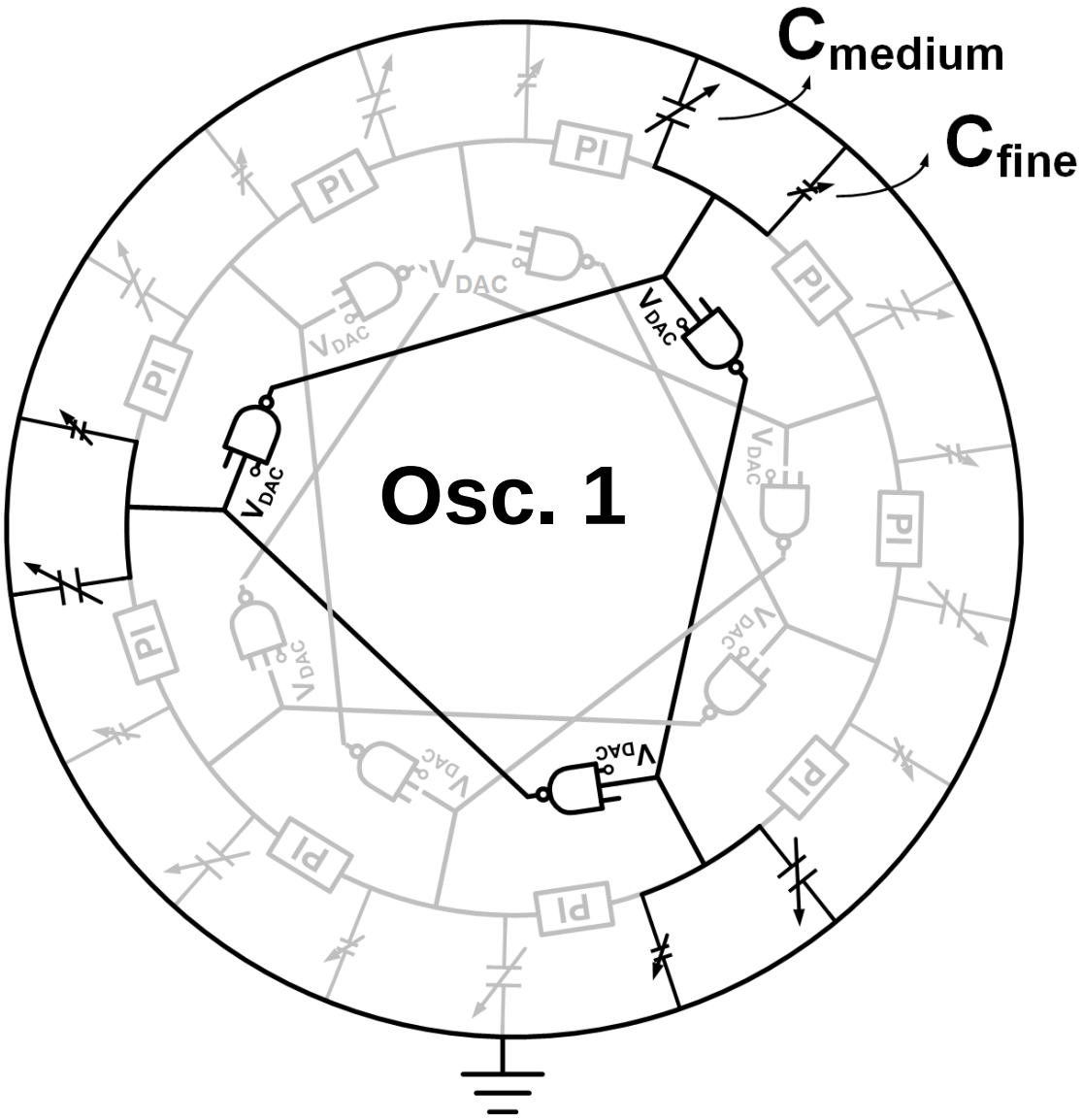
Block Diagram of DCO

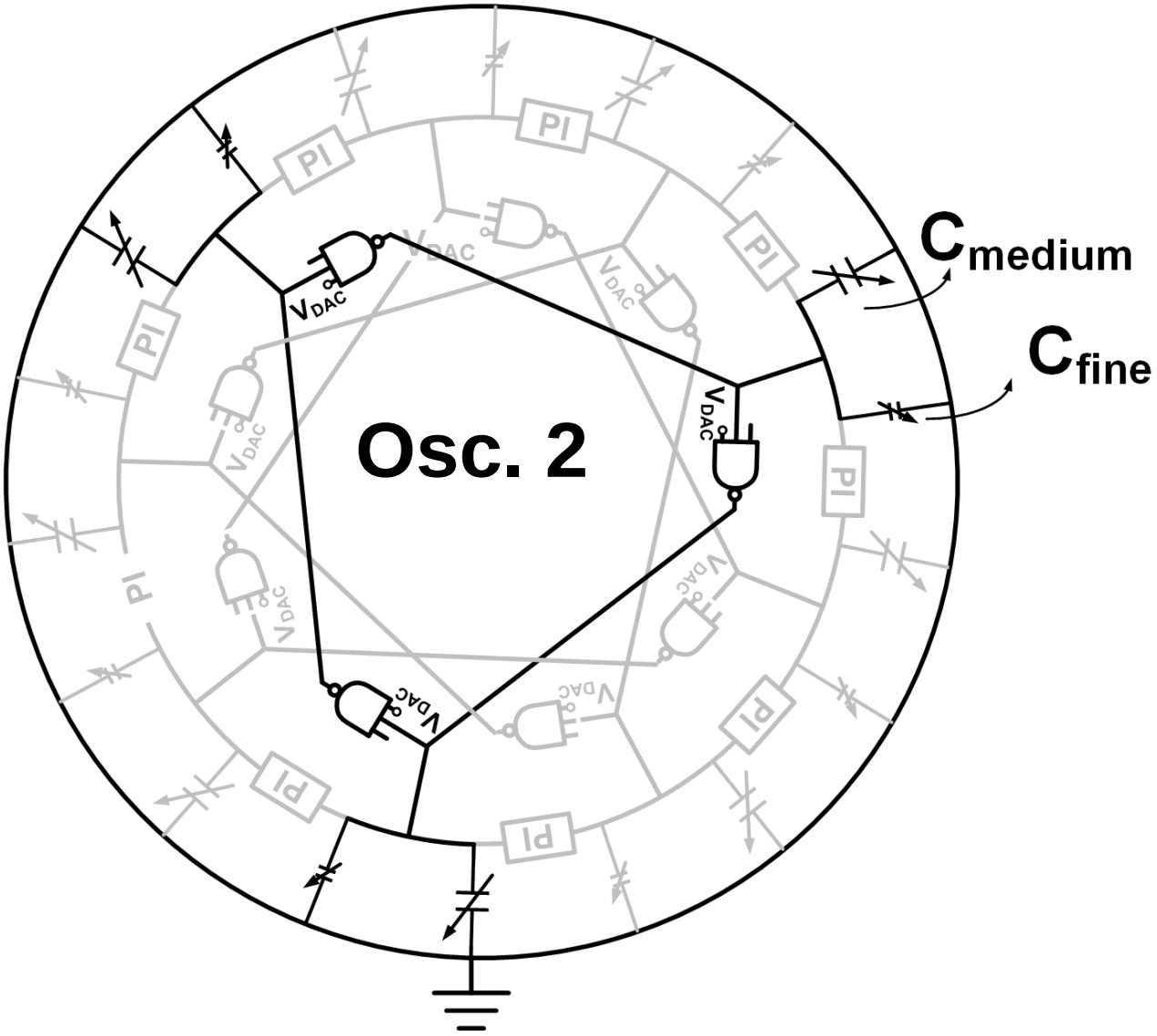


[A. Matsumoto, *et al.*, JSSC 2008]

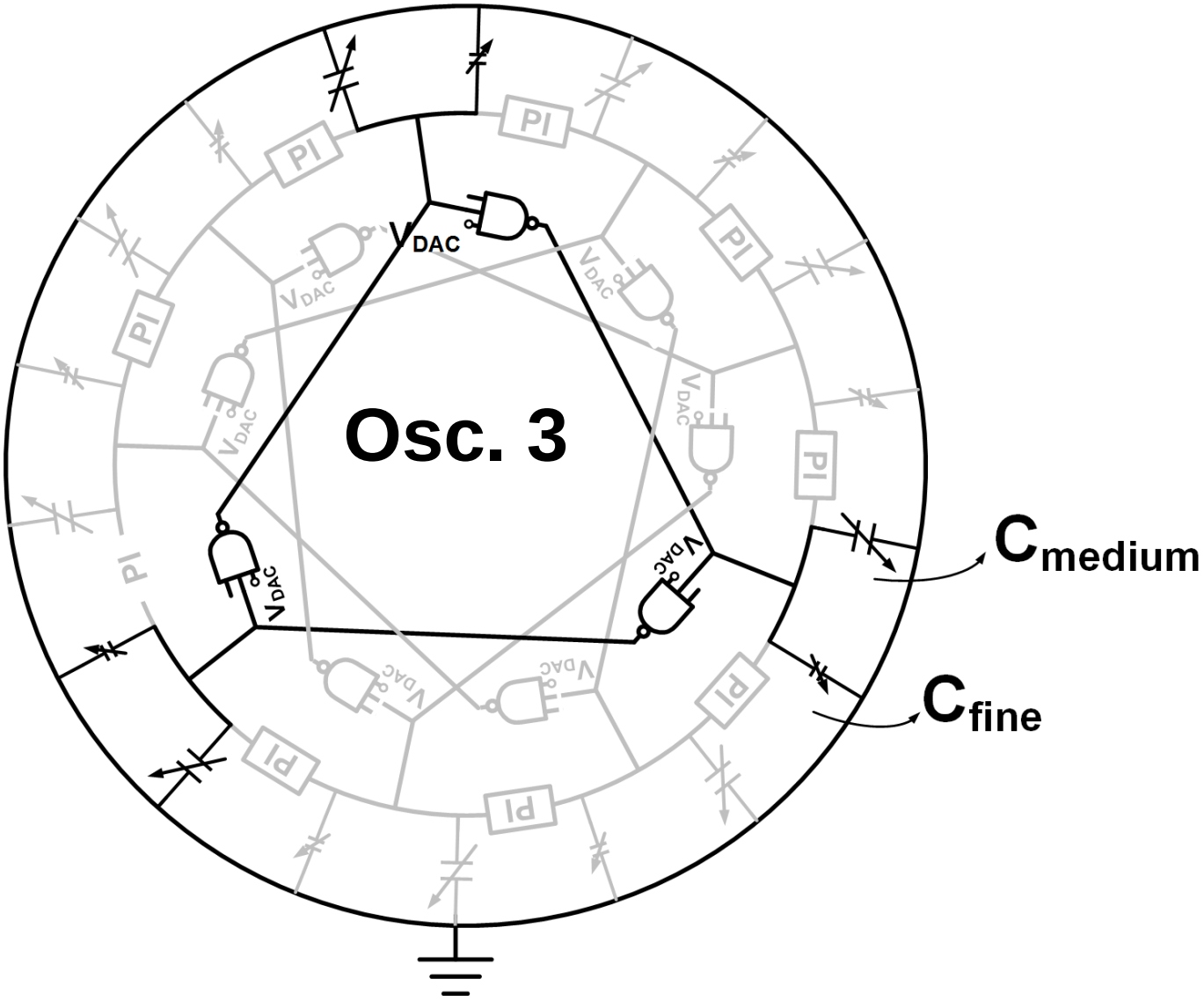
Block Diagram of Oscillator 1



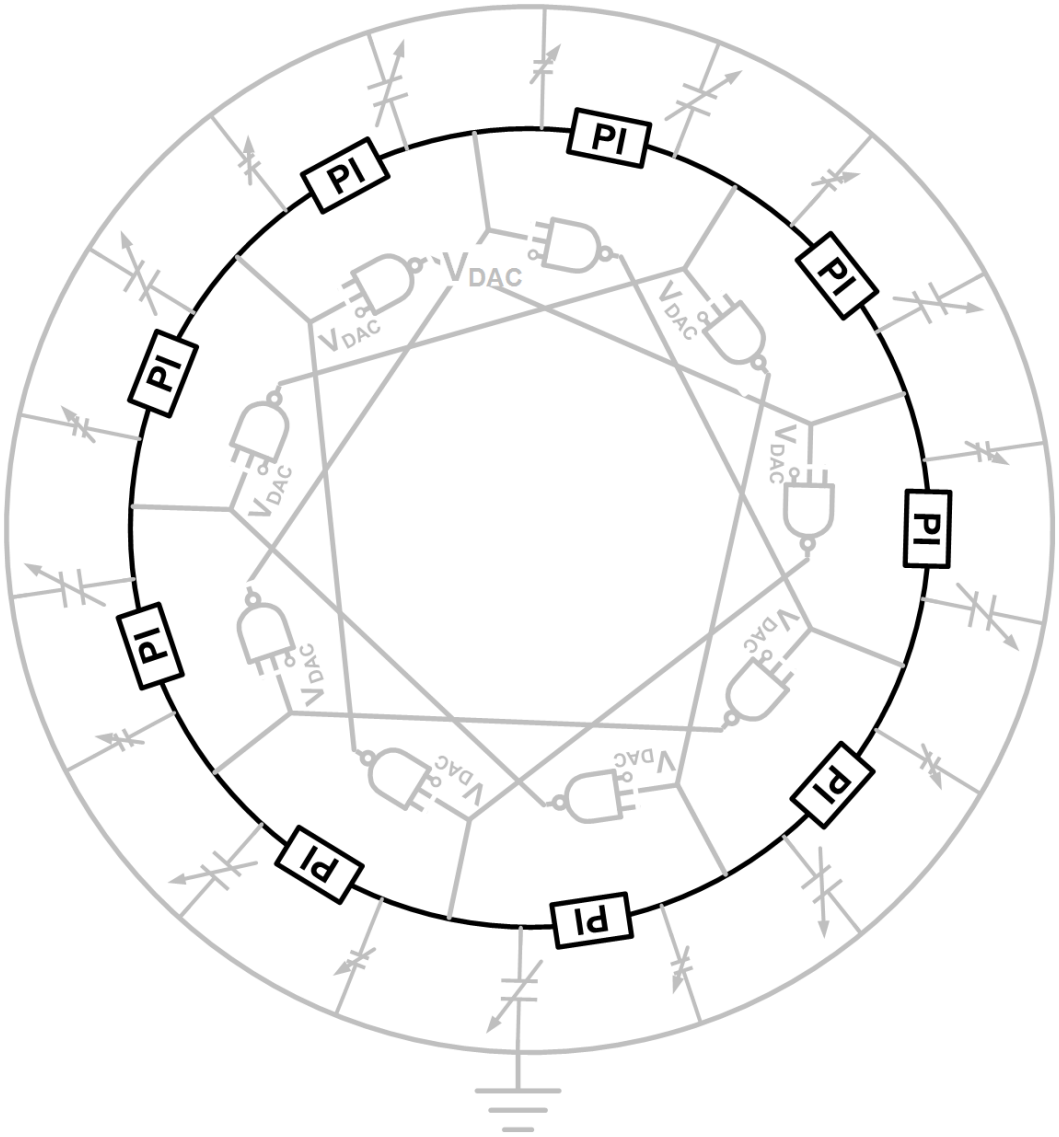
Block Diagram of Oscillator 2



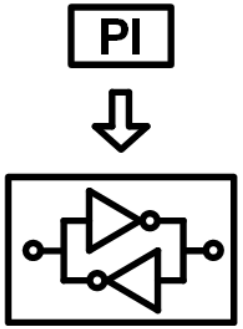
Block Diagram of Oscillator 3



Interpolative Phase-coupled Ring



PI: Phase Interpolator



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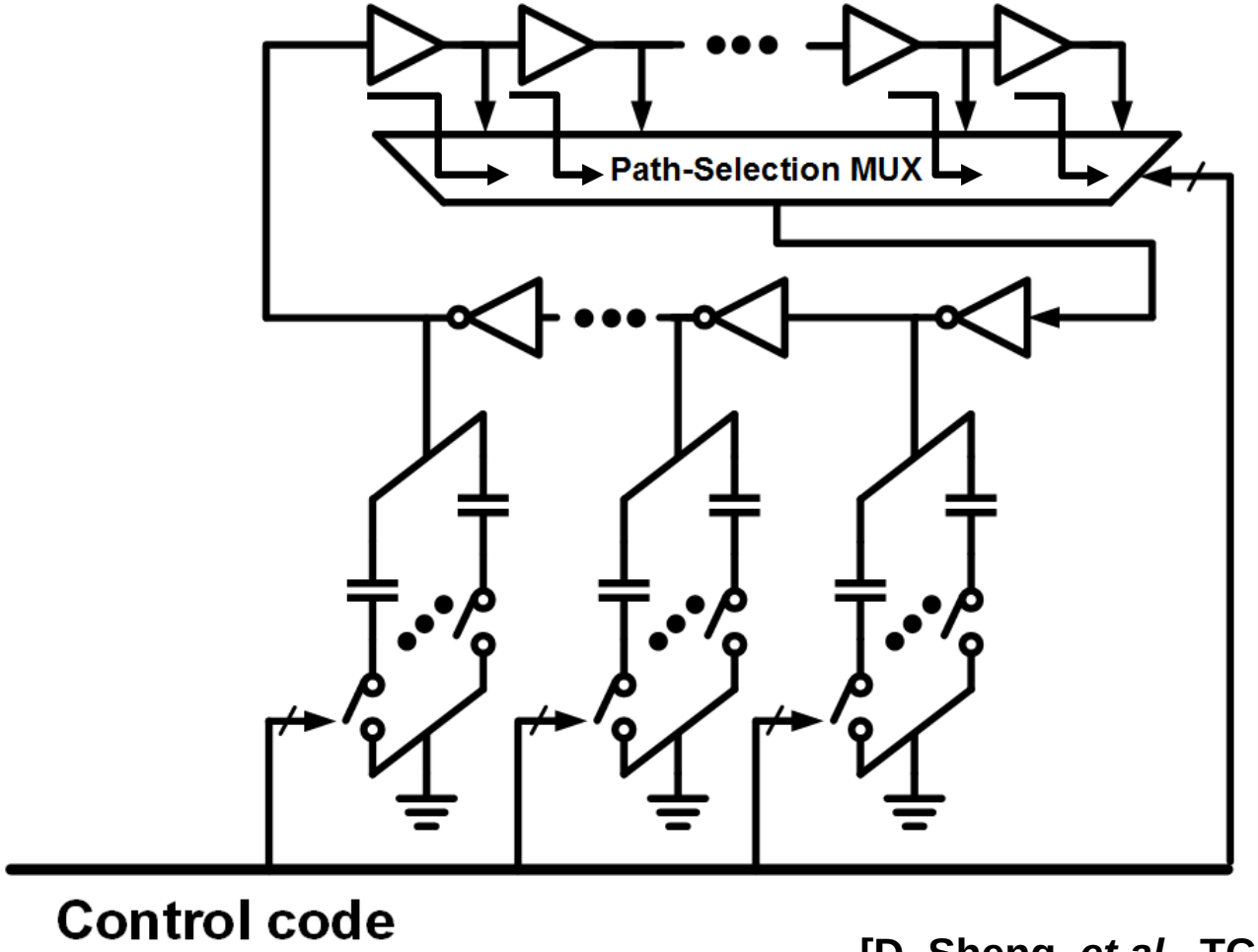
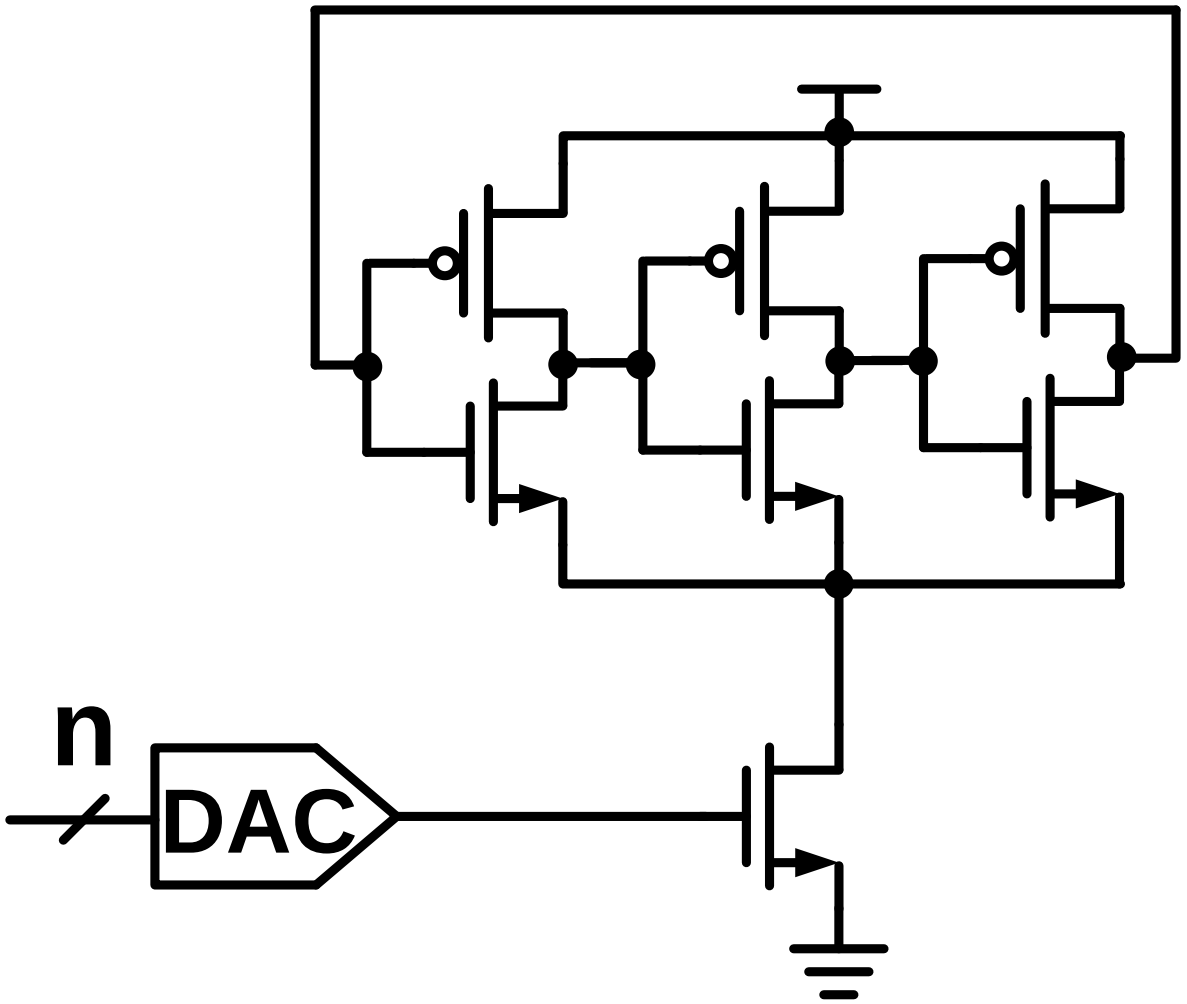
Conventional Coarse Tuning

Unbalanced loading at each stage.

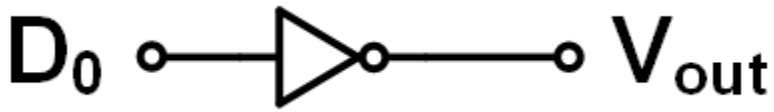


[D. Sheng, *et al.*, TCAS II 2007]

Coarse Tuning using DAC

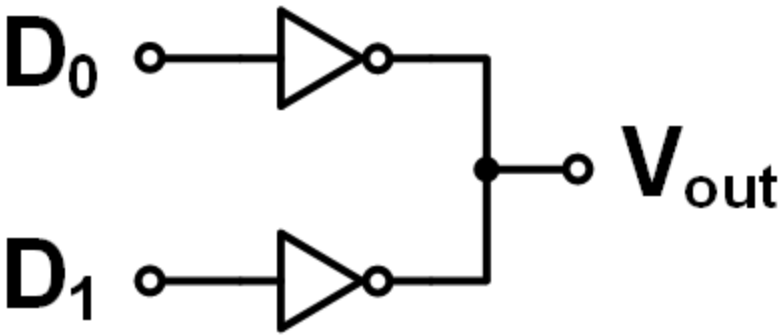


Simple Voltage-output DAC



$D_0 = 0$ $V_{out} = 1V$

$D_0 = 1$ $V_{out} = 0V$



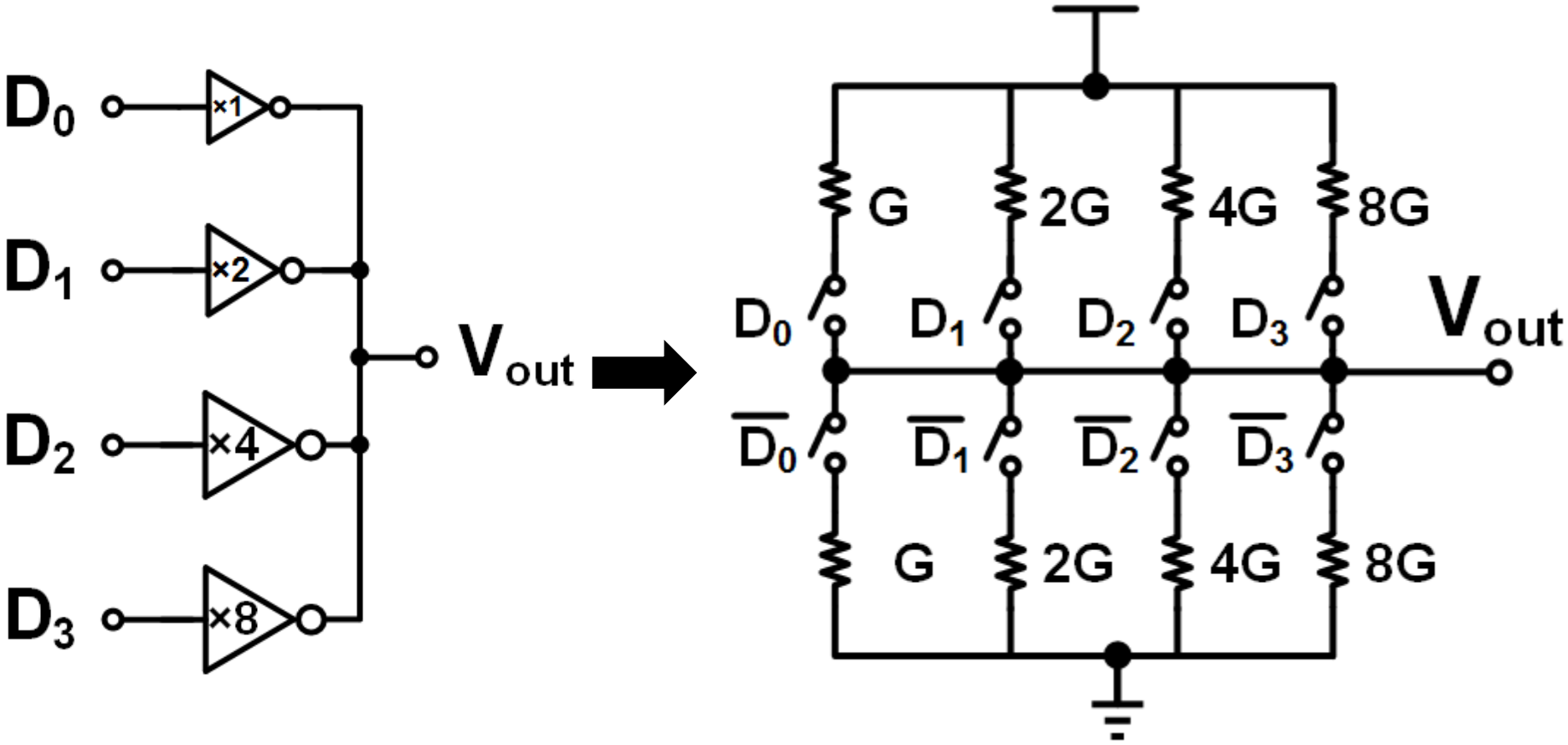
$D_0D_1 = 11$ $V_{out} = 0V$

$D_0D_1 = 10$ $V_{out} = 0.5V$

$D_0D_1 = 01$ $V_{out} = 0.5V$

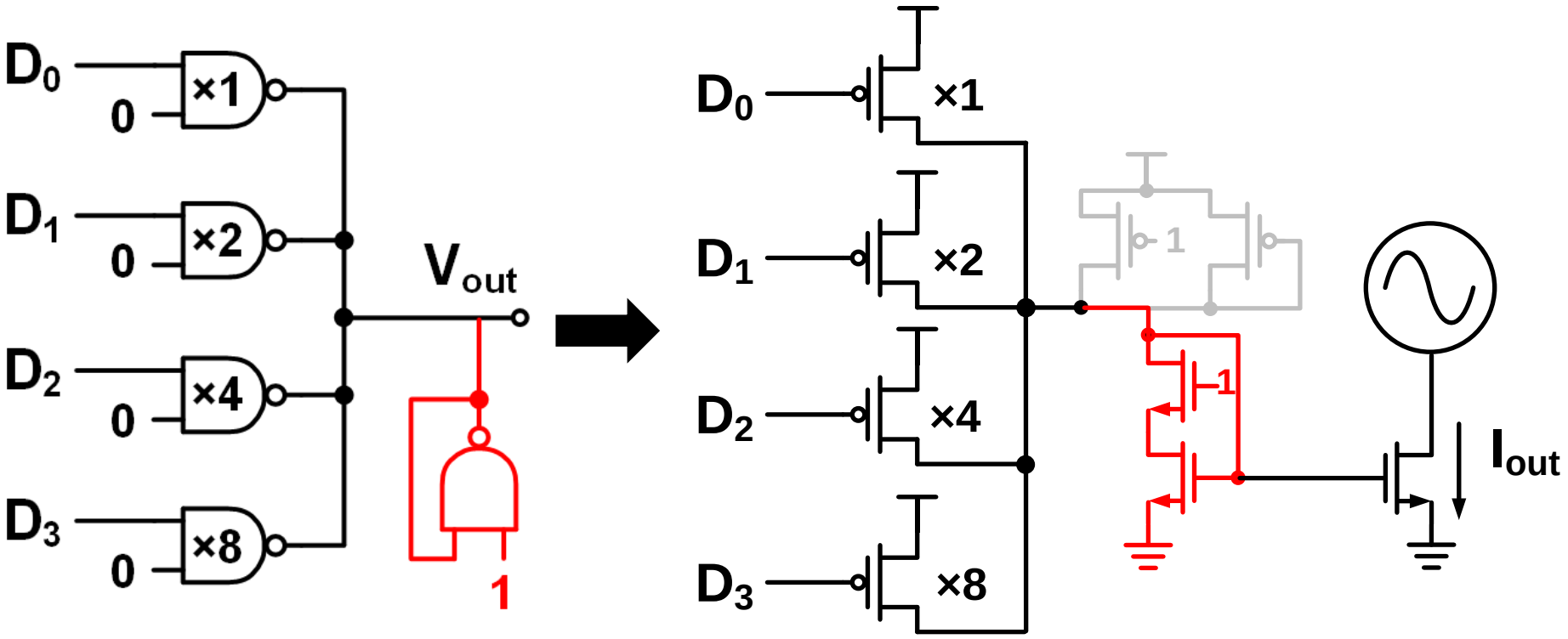
$D_0D_1 = 00$ $V_{out} = 1V$

Model of V-linear DAC



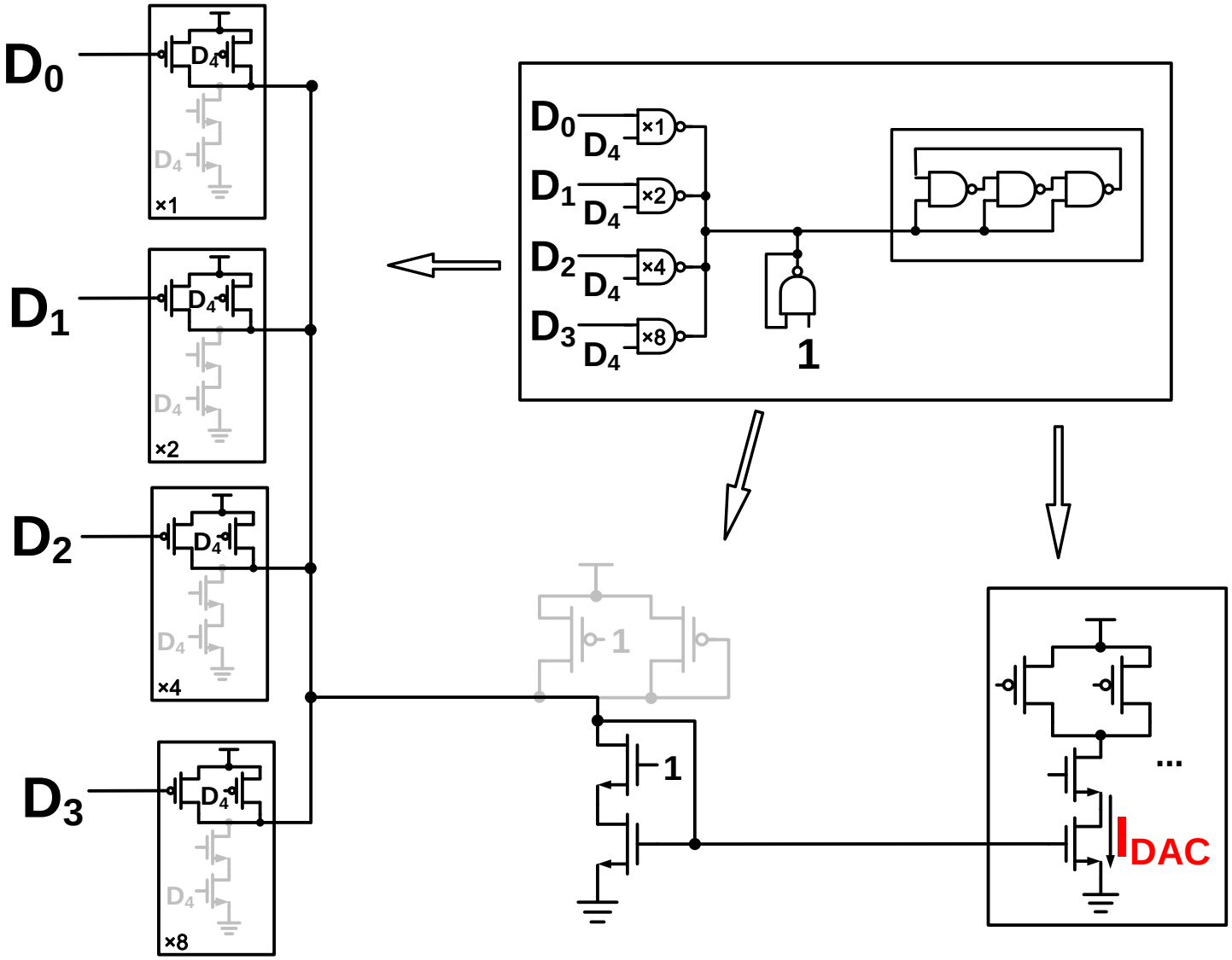
- How to obtain a I-linear DAC?

Proposed I-linear DAC

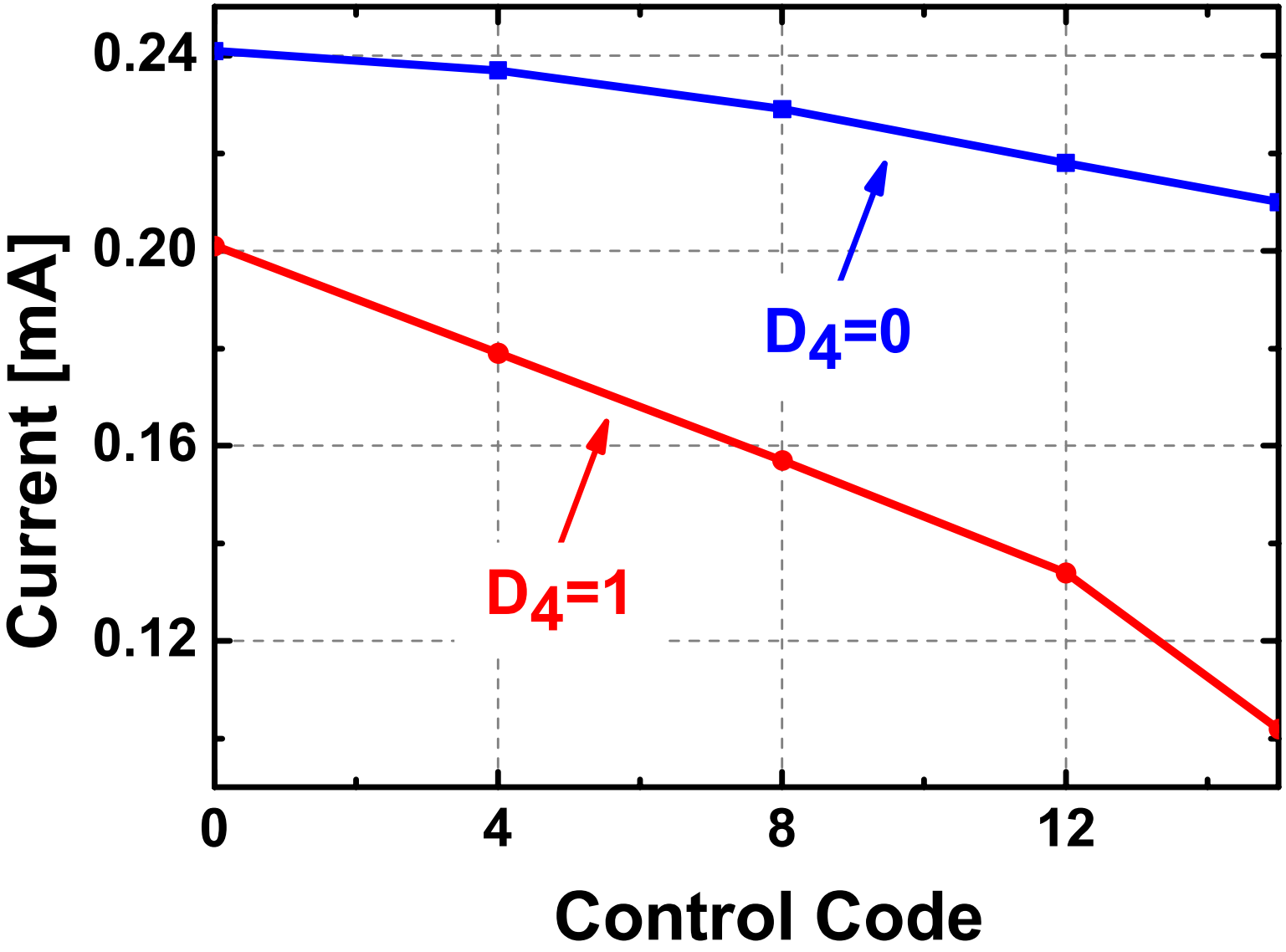


- A **feedback** structure for forming a current mirror.

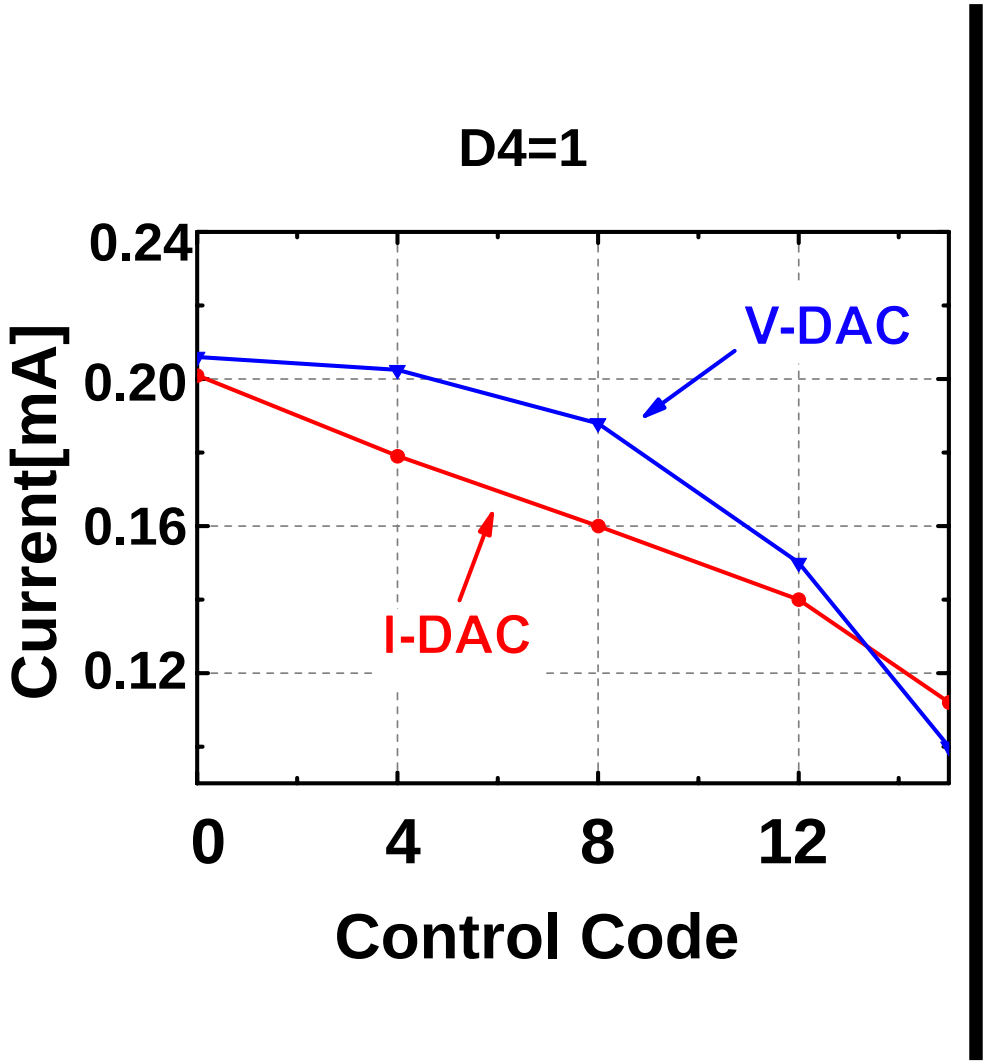
Proposed I-linear DAC (cont.)

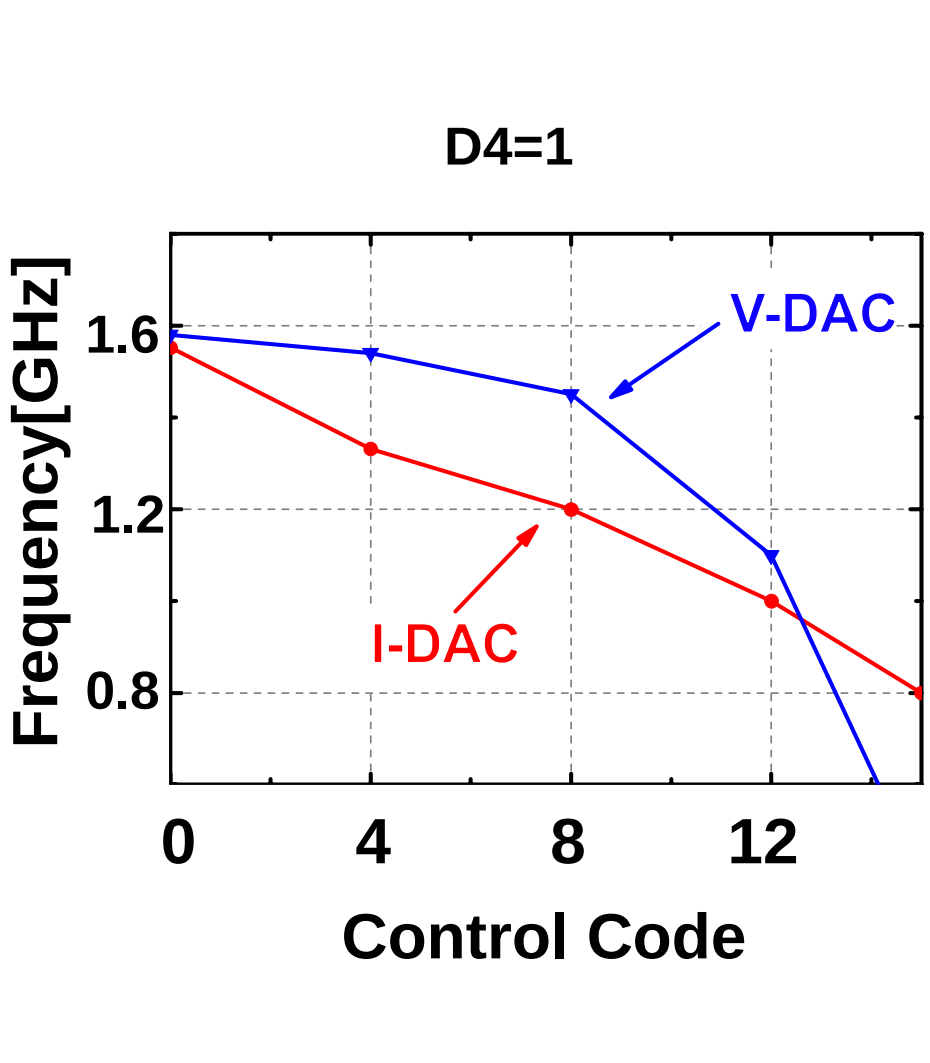


Simulation Result



V-DAC VS I-DAC





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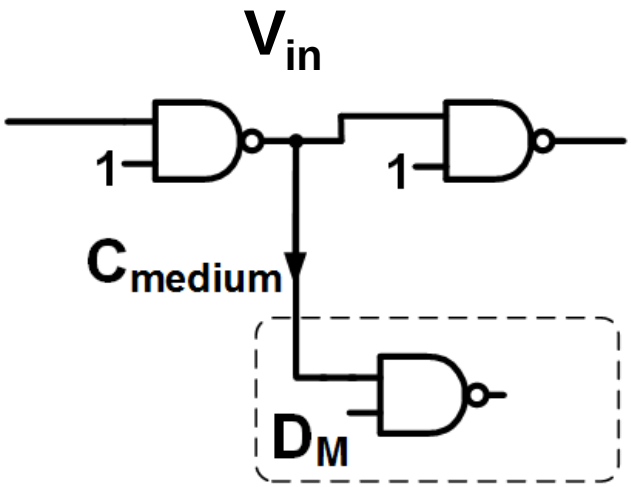
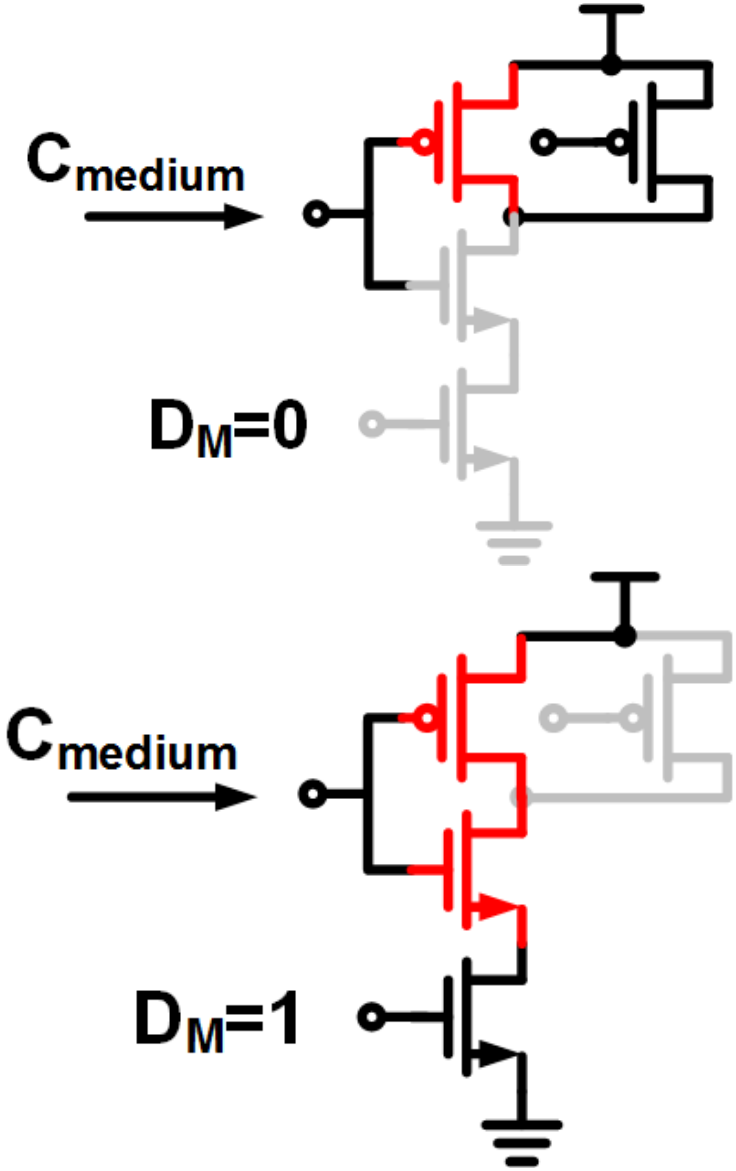
Medium Tuning Capacitor

Conventional:
1.55ps@200MHz

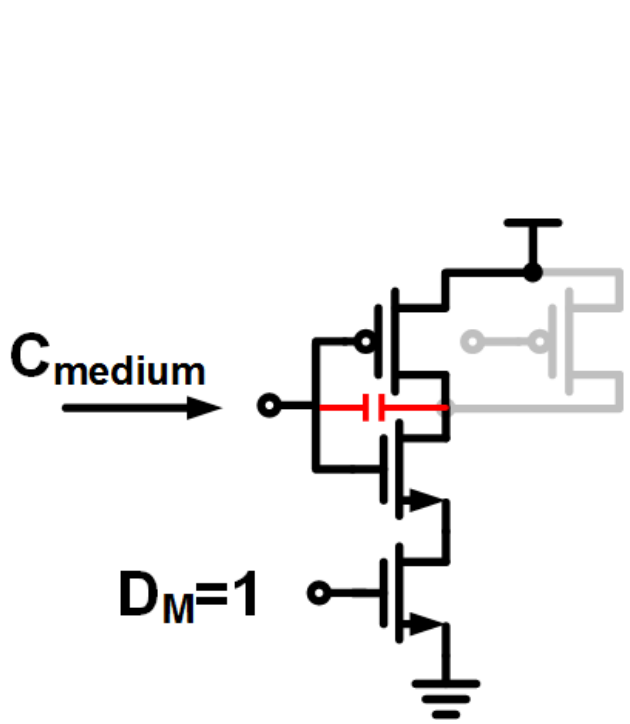


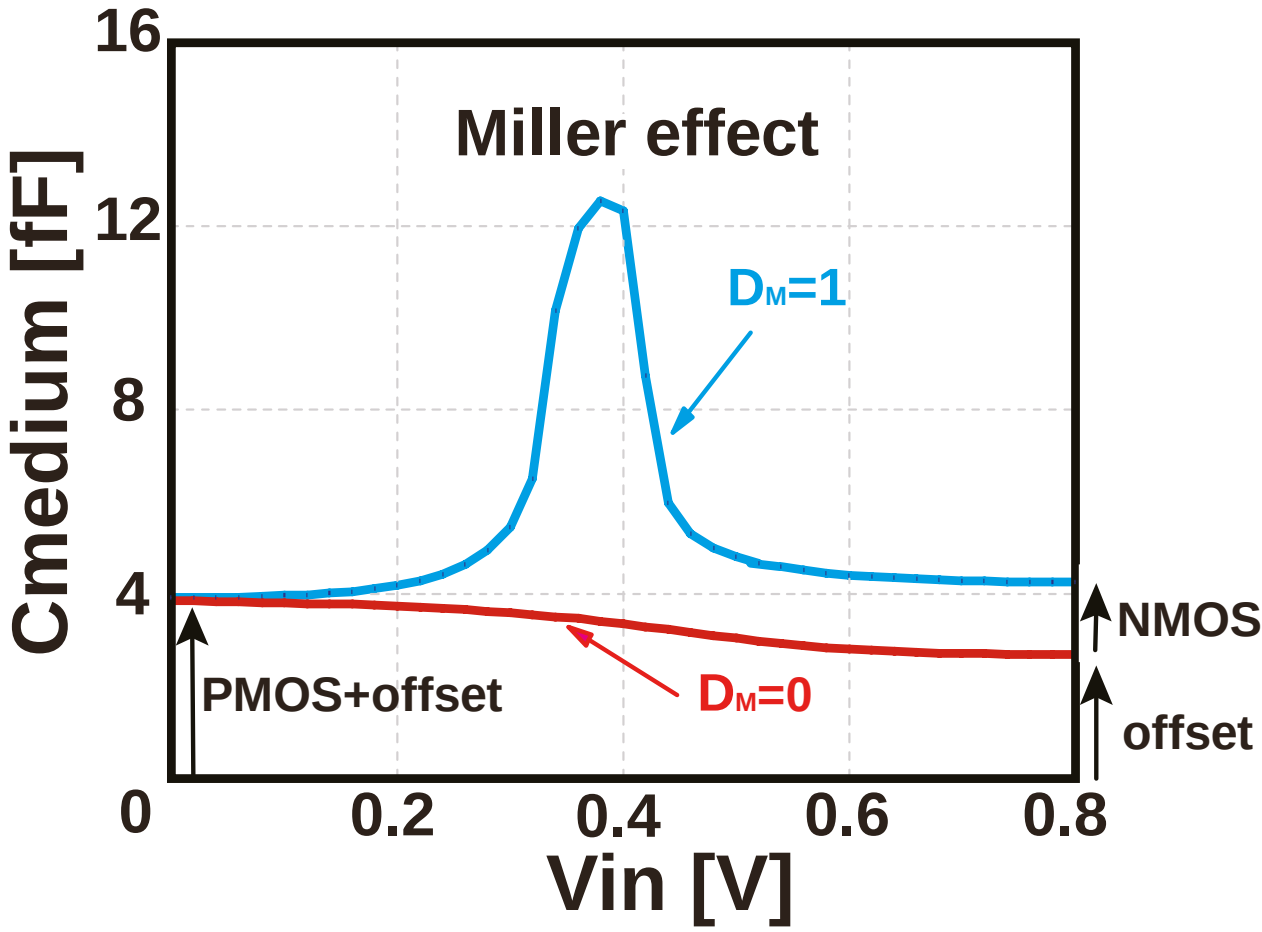
Medium resolution



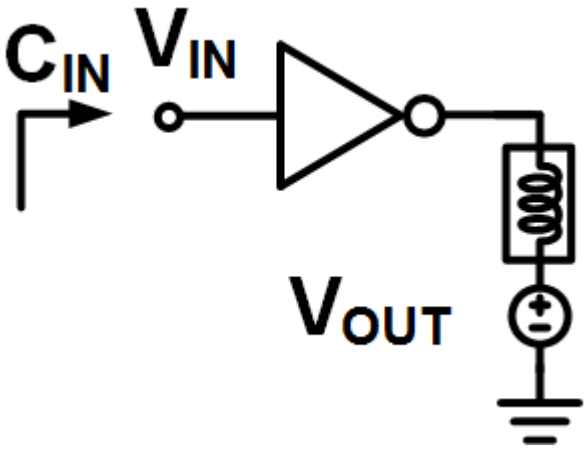
[P.L. Chen, *et al.*, TCAS II 2005]

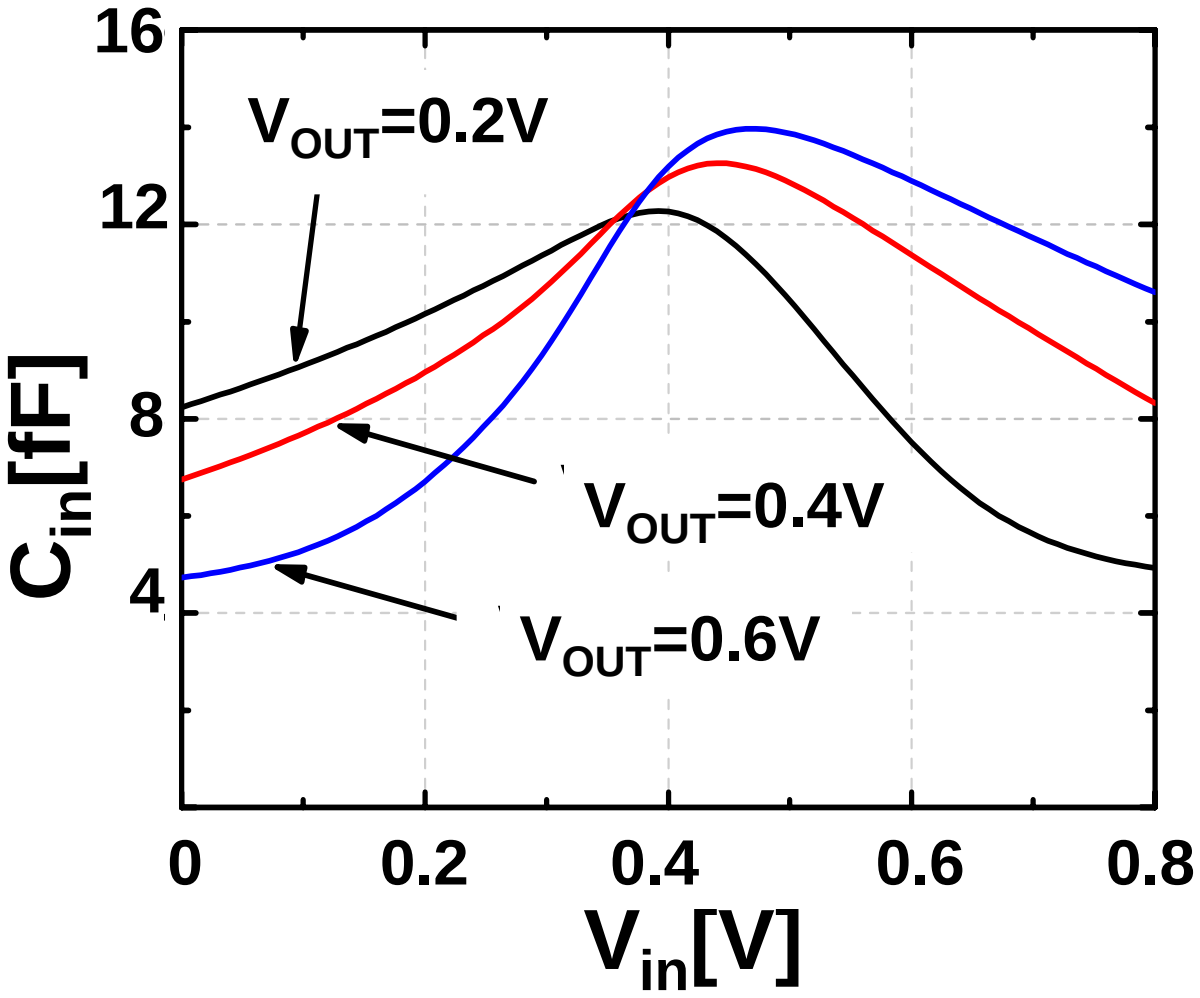
Simulated C_{medium} against V_{in}





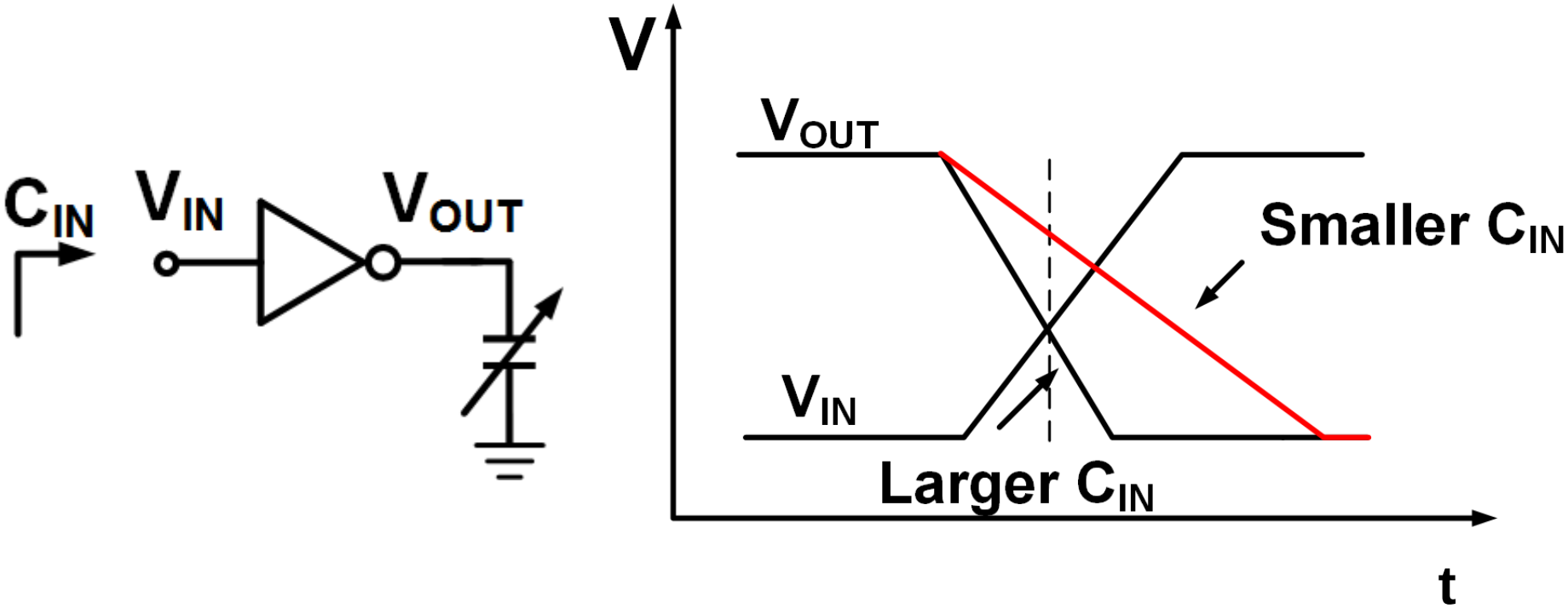
Miller Effect Sensitivity





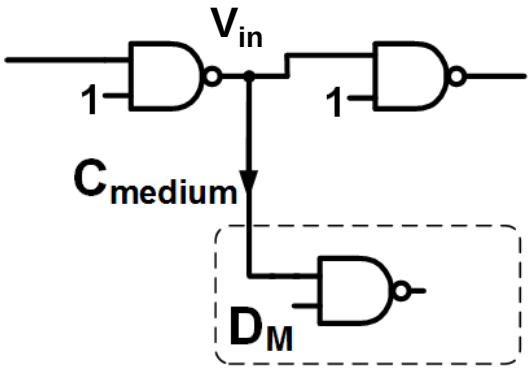
- **Miller effect can be controlled by Vout.**

Miller Effect Sensitivity (Cont.)

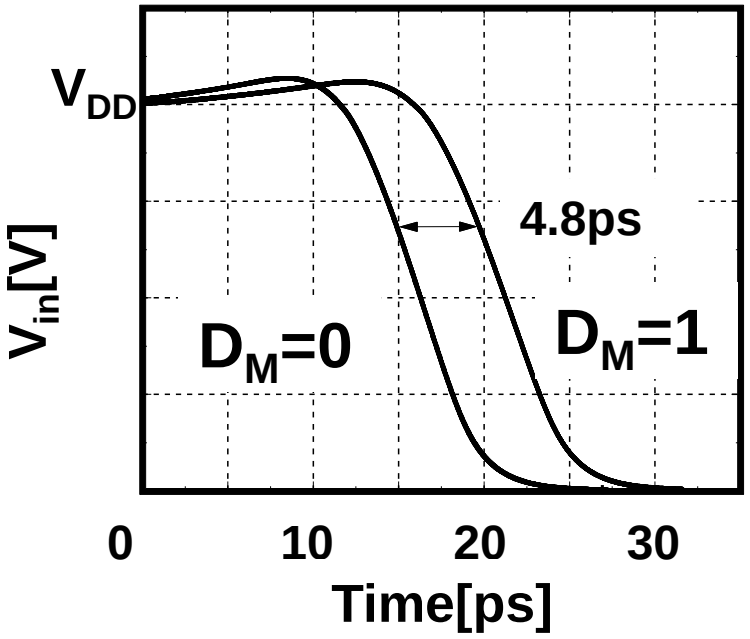


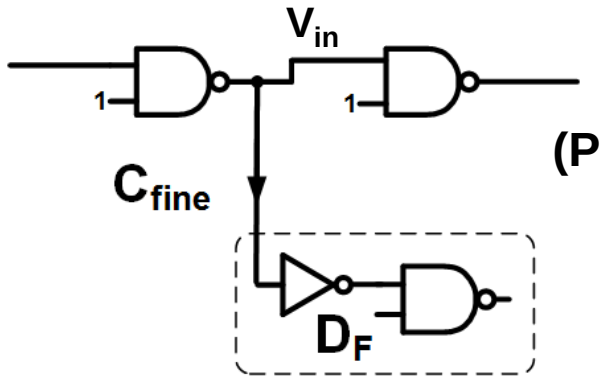
- **A transient variation of V_{OUT} can make a fine capacitance difference in C_{IN}.**

Tuning Capacitors



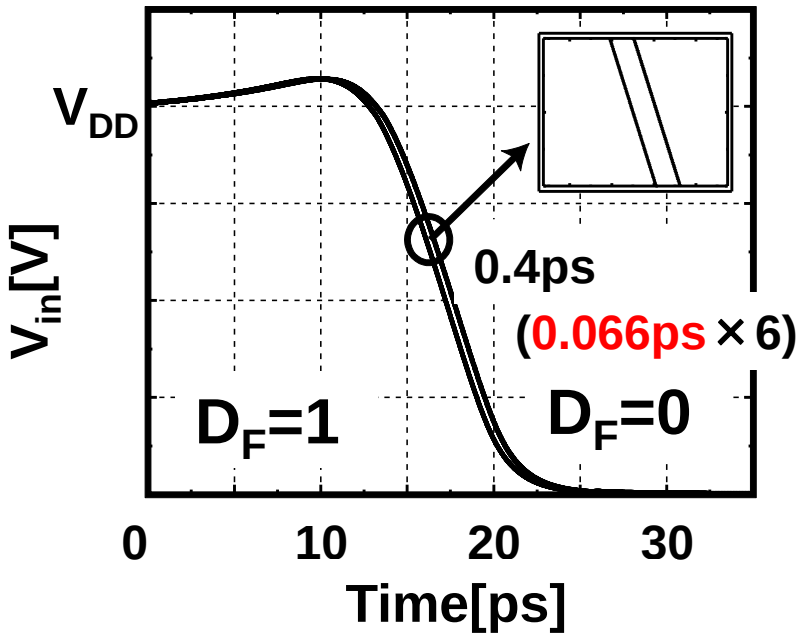
Medium resolution





(Proposed)

Fine resolution



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  - **Edge injection**
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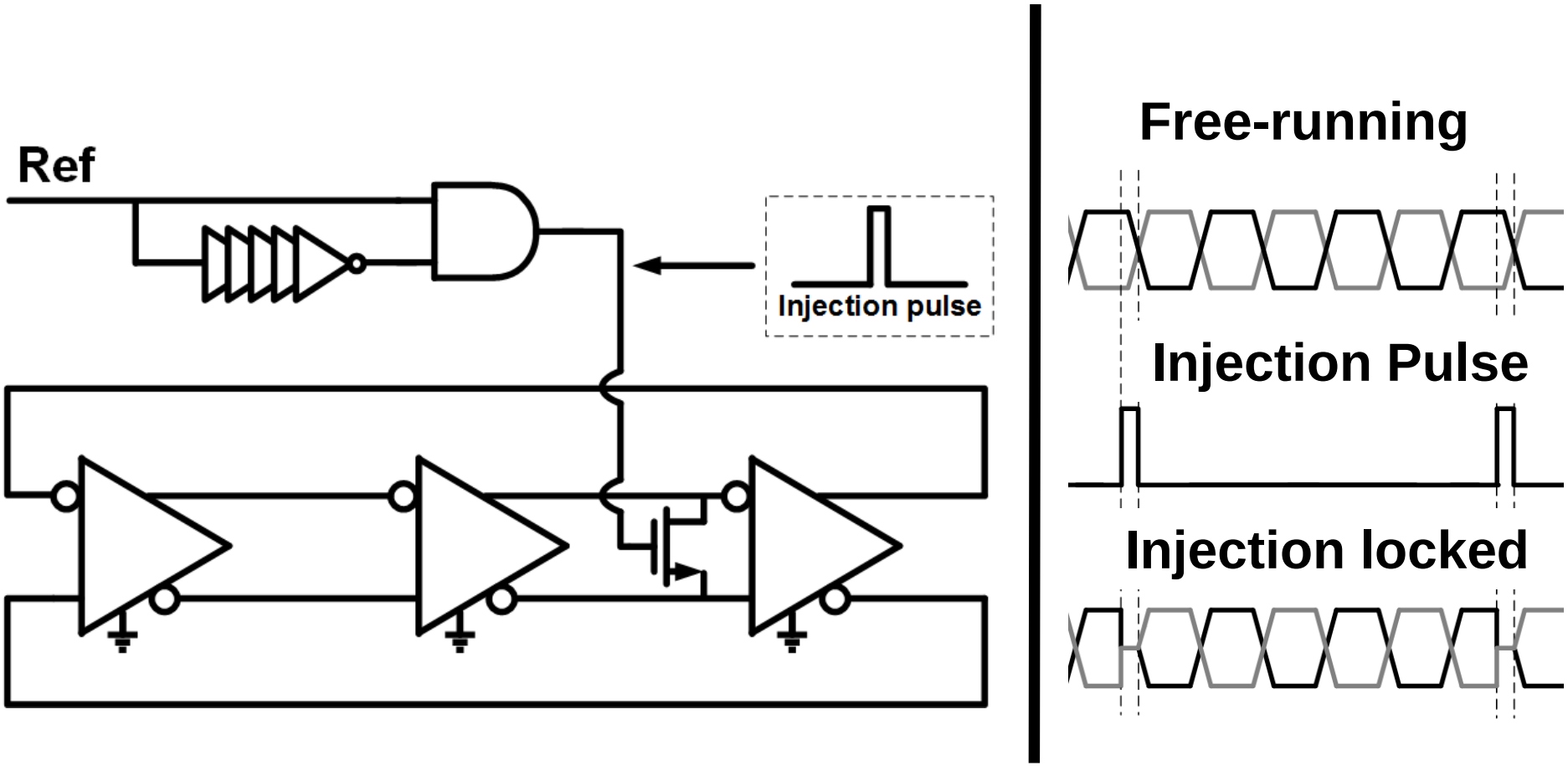
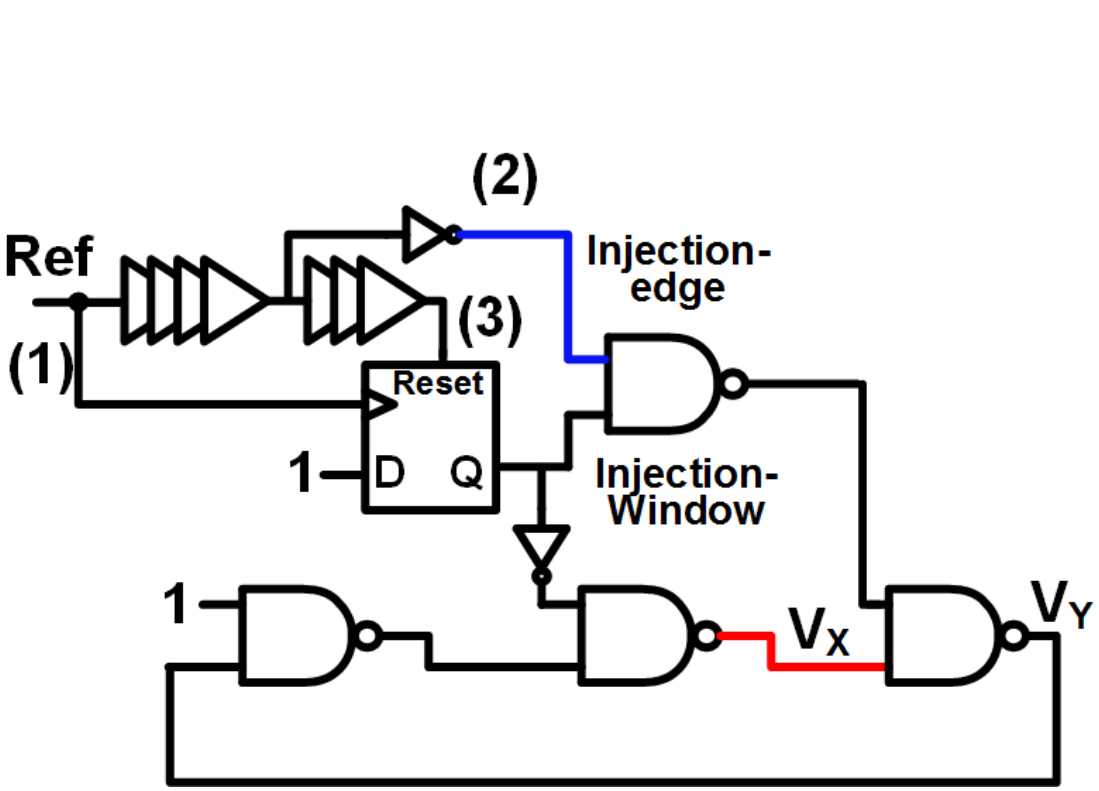
Conventional Pulse Injection

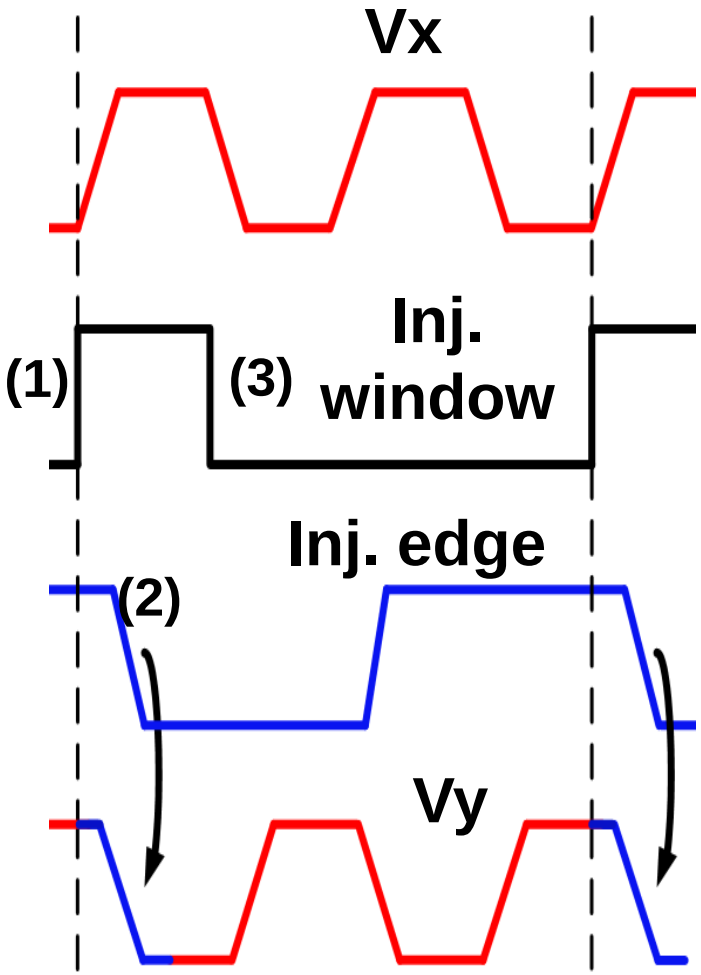


- **Severe timing design** is required on the injection pulse width.

[B. Helal, *et al.*, JSSC 2009]

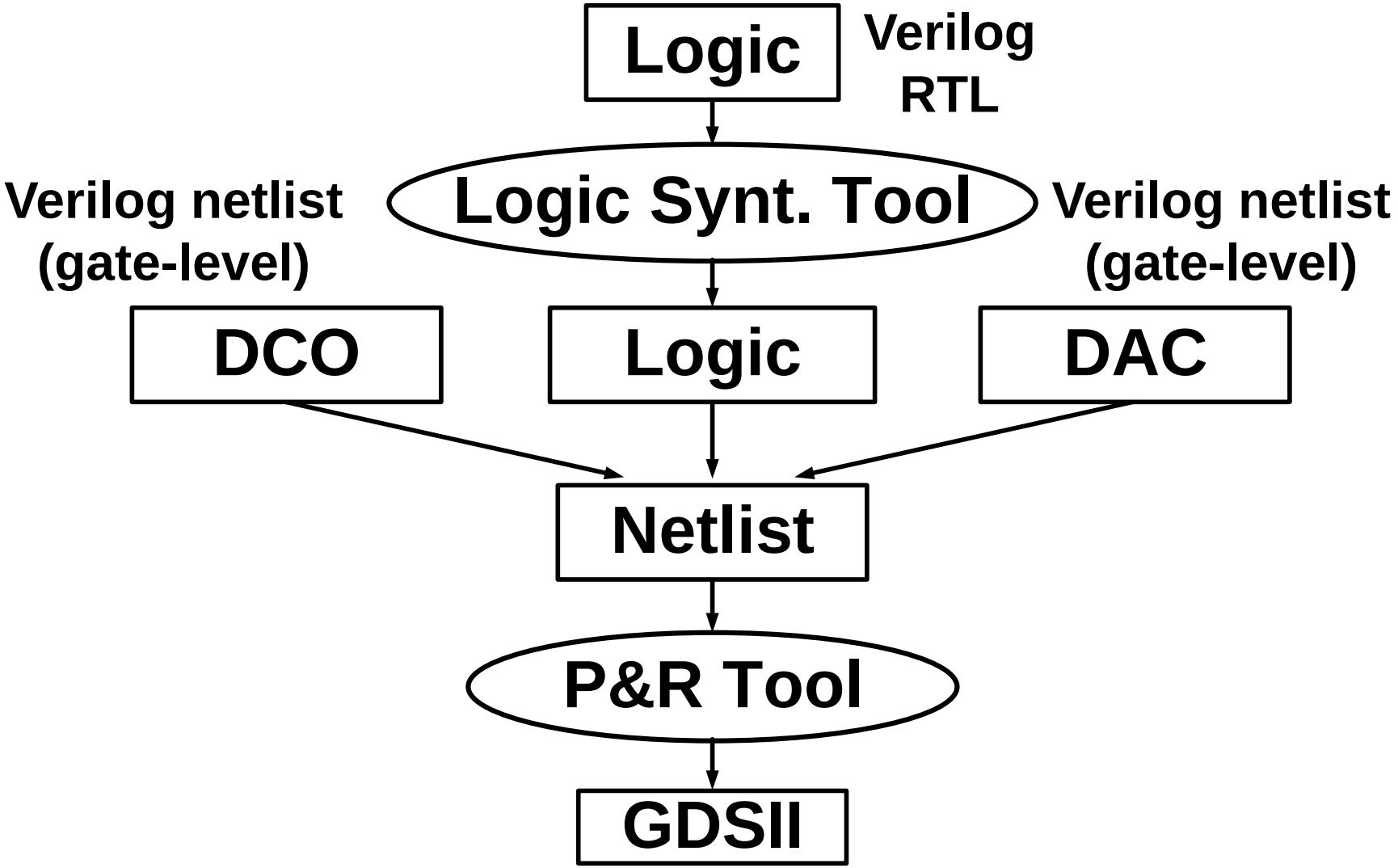
Edge Injection



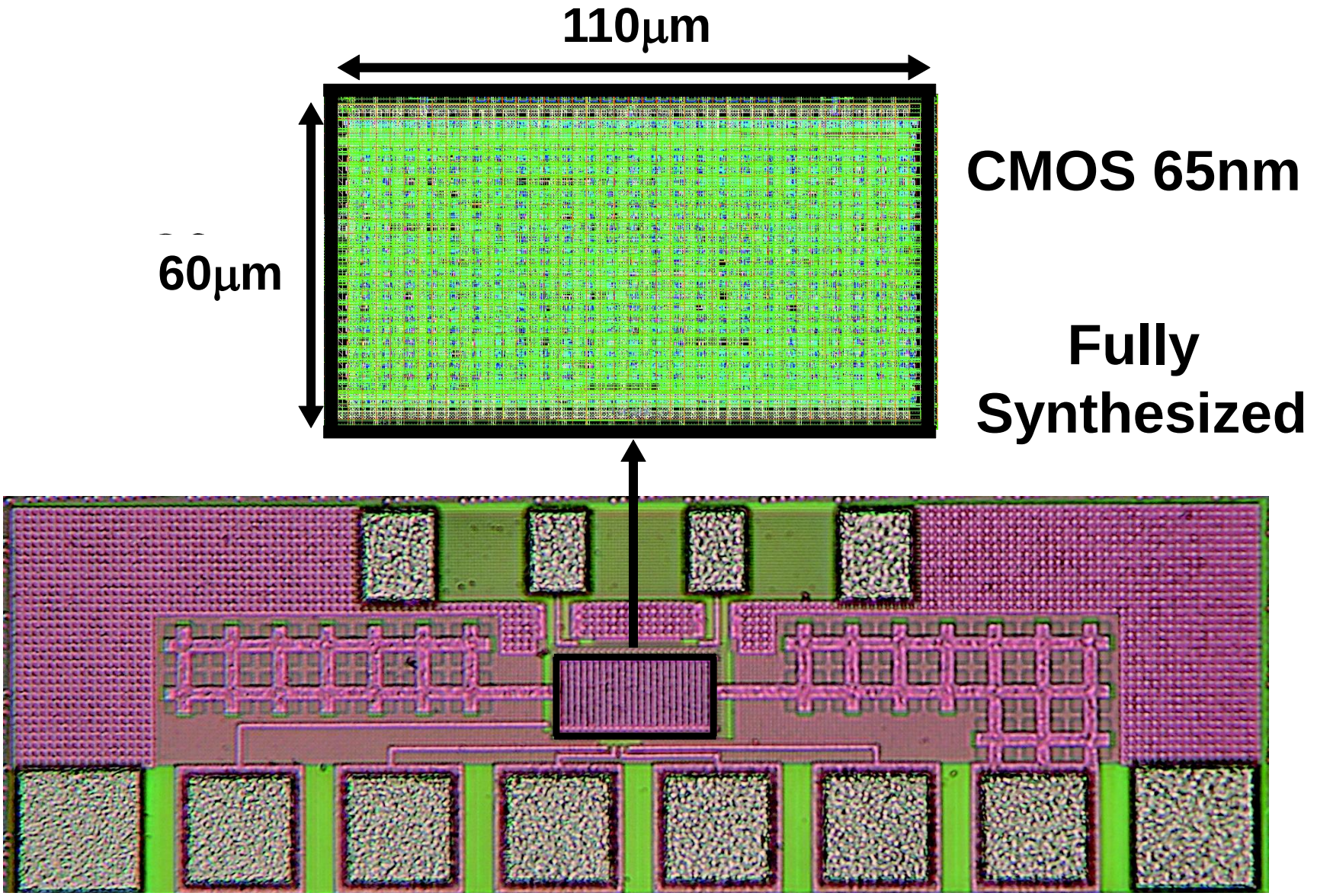


- **Severe timing design is not required.**

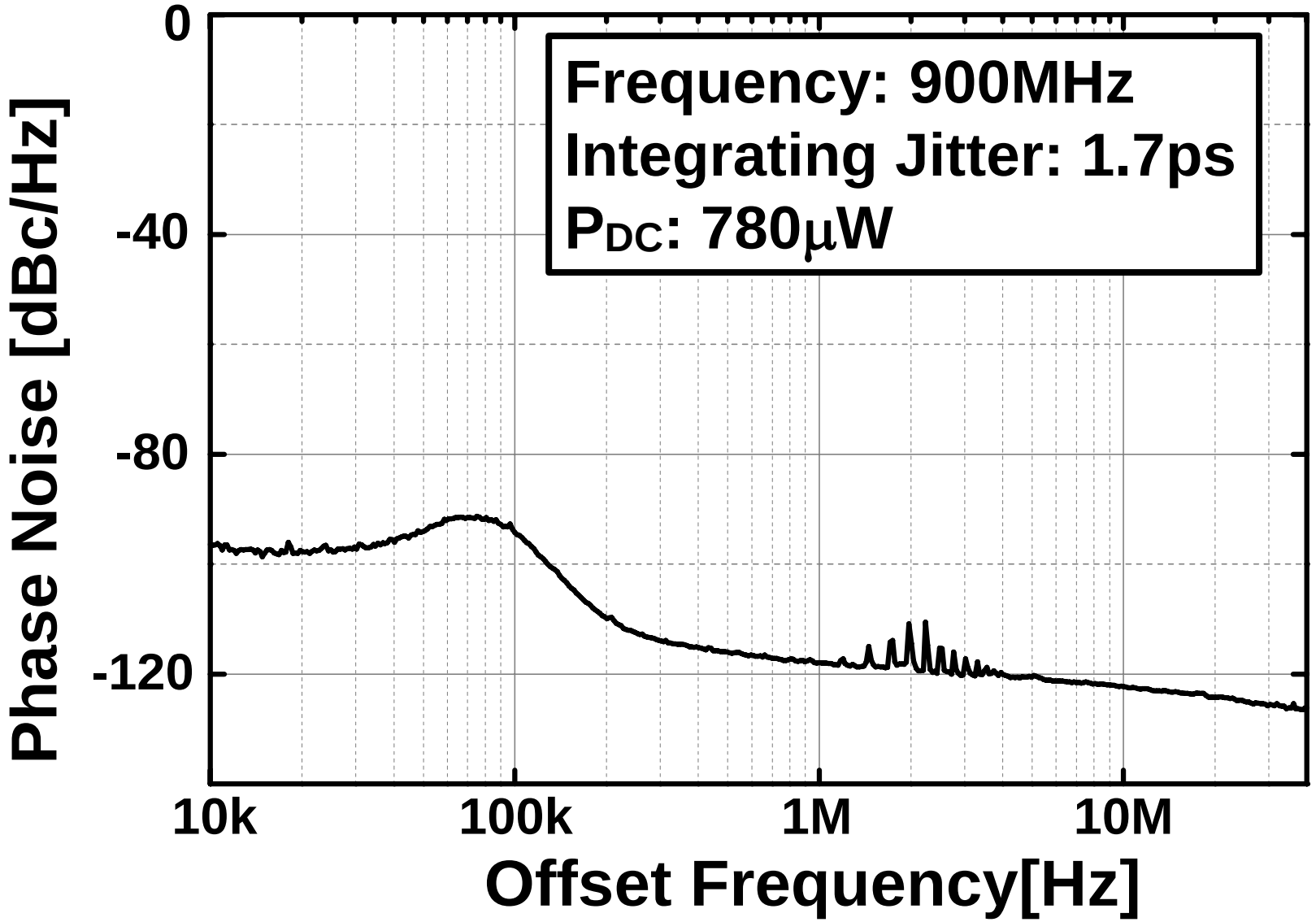
Design Procedure



Chip Microphotograph

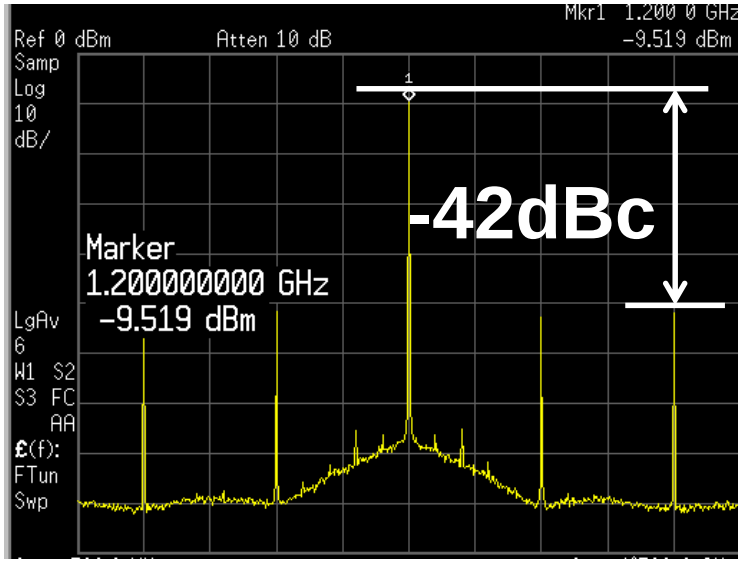


Phase Noise



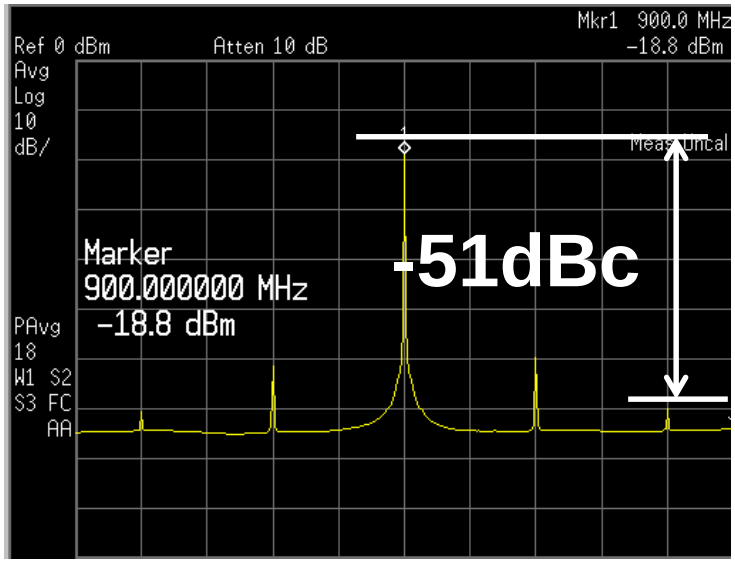
Measured Spur Level

Pulse Injection (Conventional) N=6



1st Spur: -41 dBc
2nd Spur: -42 dBc

Edge Injection (This work) N=6

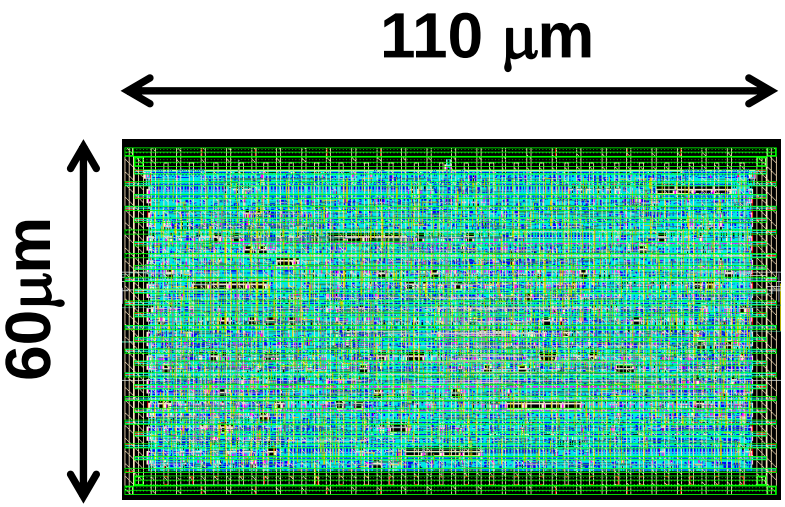


1st Spur: -41 dBc
2nd Spur: -51 dBc

N: Multiplication factor

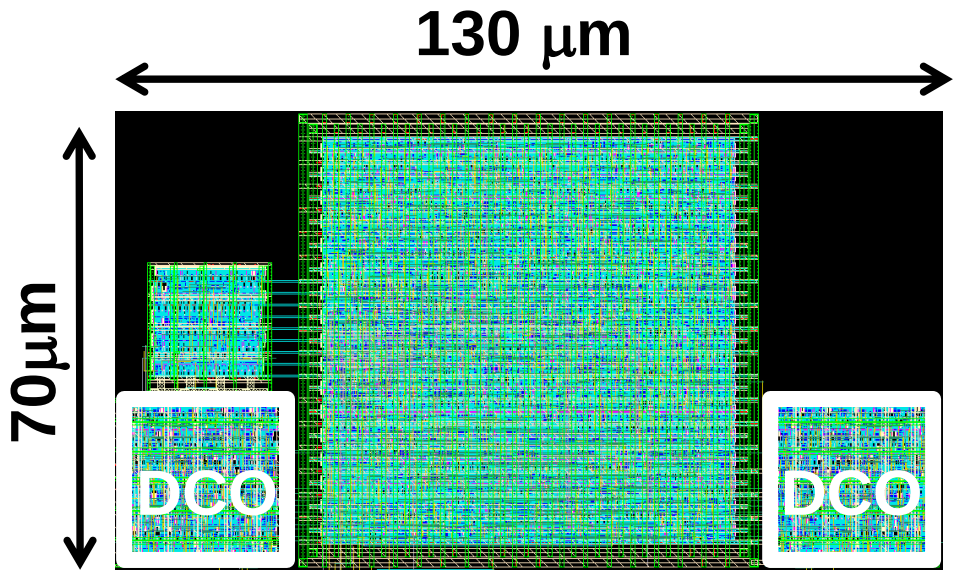
Layout Consideration

Integrating Jitter: 1.7ps
P_{DC}: 780μW
FOM: -236.5 dB



Fully synthesized (proposed)

Integrating Jitter: 2.32ps
P_{DC}: 640μW
FOM: -234.6 dB



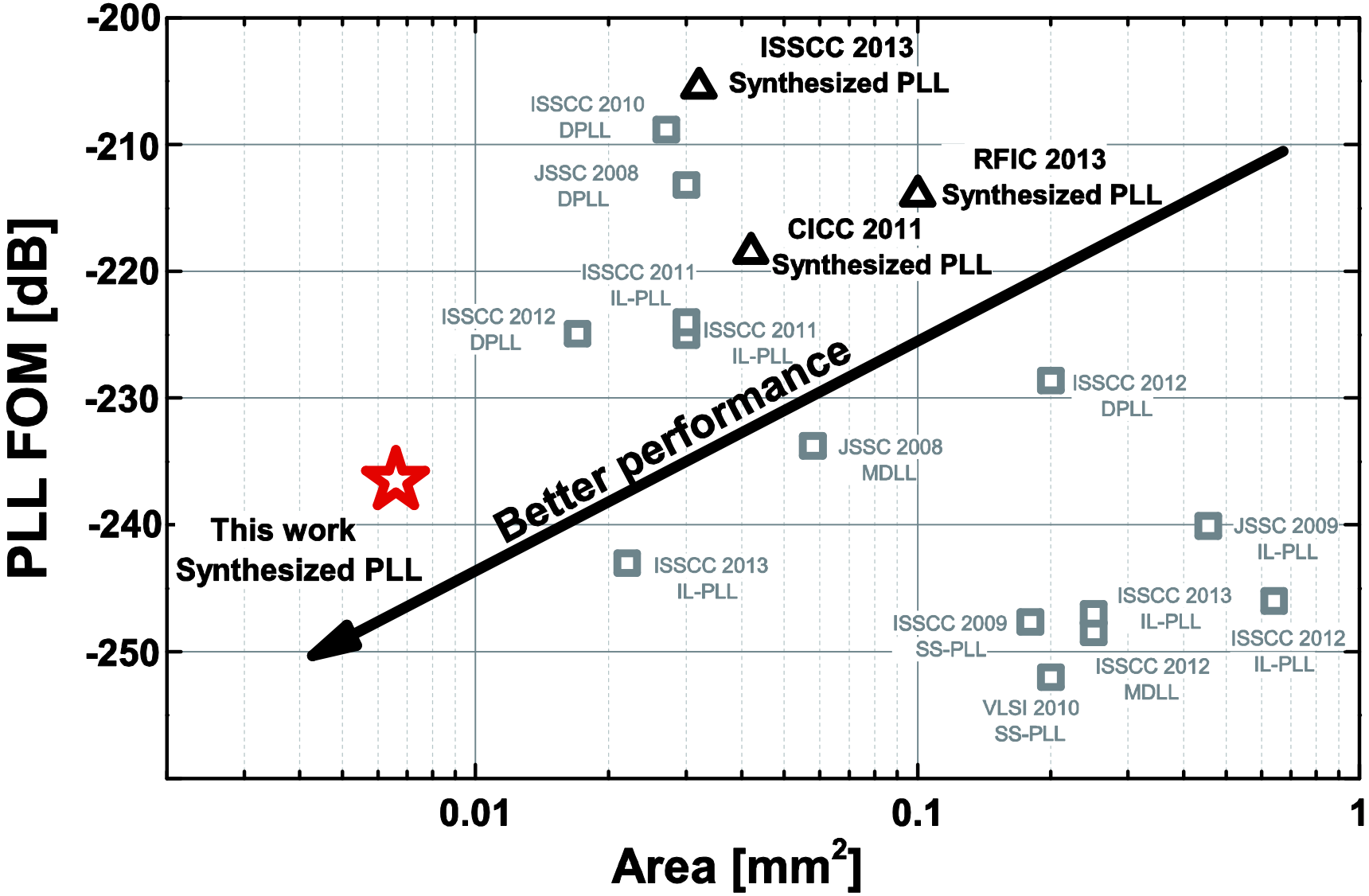
Hierarchical P&R with synthesized DCOs

Compar. of Synthesizable PLLs

	This work 65nm	[1] 28nm	[2] 65nm	[3] 65nm
Power [mW]	0.78 @900MHz	13.7 @2.5GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	0.0066	0.042	0.032	0.1
Integ. Jitter [ps]	1.7	N.A.	30	N.A.
RMS Jitter [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	-236.5	-218.6*	-205.5	-214*
W/ custom cells?	No	No	Yes	Yes
Topology	IL-base	TDC-base	TDC-base	TDC-base

*FOM is calculated based on RMS jitter.

Performance Comparison



Conclusion

- **Synthesizable analog circuit design is proposed.**
  - **By the digital design flow**
  - **Without any manual placement**
  - **Without any custom-designed cells**
- **Fully synthesized PLL**
  - **Dual-loop injection-lock topology**
  - **Current-output DAC**
  - **Ultra-fine frequency resolution**
  - **Interpolative-phase coupled oscillator**

Acknowledgement

This work was partially supported by STARC, SCOPE, MIC, MEXT, Canon Foundation, and VDEC in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.