15.1 A 0.0066mm² 780μW Fully Synthesizable PLL with a Current-Output DAC and an Interpolative Phase-Coupled Oscillator Using Edge-Injection Technique

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Phase-locked loops (PLLs) are widely used for clock generation in modern digital systems. All-digital PLLs have been proposed to address design issues in conventional analog PLLs. However, current all-digital PLLs require custom circuit design, and therefore cannot leverage advanced automated digital design flows. While fully synthesizable PLLs [1, 2, 3] have been reported, they suffer from high power consumption and large area. This arises because each stage of the ring needs to have a large number of parallel tristate buffers/inverters in order to achieve the necessary frequency resolution. Moreover, custom-designed cells are required in prior synthesizable PLLs [2, 3], introducing additional place-and-route (P&R) steps, leading to poor portability, integration, and scalability. To address these issues, this paper proposes a fully synthesizable PLL based solely on a standard digital library, with a current-output digital-to-analog converter (DAC) for maintaining frequency linearity and duty balance, an interpolative phase-coupled oscillator for minimizing the output phase imbalance from automatic P&R, as well as an edge injection technique for avoiding injection-pulse width issues.

A block diagram of the proposed PLL with a DAC and an interpolative phase-coupled oscillator is given in Fig. 15.1.1. All circuits that makeup the PLL, including the DAC and DCO, are implemented using standard cells and an automated design flow. A dual-loop PLL architecture [5] is employed and improved in this design to provide continuous tracking of voltage/temperature variations and to avoid the timing problems associated with conventional injection-locked PLLs. The frequencies of two oscillators are digitized by two counters. A signed adder/subtractor compares the digitized frequencies with a predefined frequency-control word (FCW) and provides a frequency difference to a digital-loop filter consisting of a proportional path and an integral path. The filter output determines whether to increase, decrease, or hold the DCO oscillation frequency. In addition, an edge-injection technique is incorporated into this design.

Figure 15.1.2 illustrates the proposed oscillator architecture that is used in both main and replica VCOs. In order to relieve the oscillator output phase imbalance caused by the automatic P&R, an interpolative phase-coupled oscillator built by three 3-stage oscillators is developed, based on the concept in [6]. Due to its internal feedback and feed-forward control using phase interpolators for the oscillator, the phase difference within the ring and between all adjacent rings will remain fixed in time, leading to balanced output phases. To maintain the control-code resolution and extend the operating frequency range, the oscillator is designed to operate with a coarse, medium, and fine tuning. A standard cell-based DAC controls the coarse tuning of the oscillator. As shown in Fig. 15.1.2, a digitally-controlled varactor using NAND gates is adopted in the medium-tuning circuitry. The fine-tuning circuitry is realized by another type of digitally controlled varactor using inverters and NAND gates. A digitally controlled NAND gate introduces a capacitance difference at the inverter output node, which alters the rising and falling slopes, thereby changing an influence on Miller effect. Thus, the effective capacitance seen from the ring oscillator is also changed. This capacitance difference is adopted for the fine-tuning stage.

Conventionally, a path-selection method is applied for coarse tuning in synthesized oscillators [4], helping to reduce power consumption and chip area. However, this method suffers from unbalanced output phases due to different loading at each stage, degrading injection efficiency. In our design, an analog-equivalent DAC built from standard CMOS NAND gates is used in the coarse-tuning circuitry, reducing power consumption and area, without sacrificing phase balance. Tristate buffers are not used, as they may not be present in some standard cell libraries. To make it easier to understand, Fig. 15.1.3 depicts a diagram of a 4b binary-weighted current-output DAC constructed from five two-input NAND gates. The DAC consists of a PMOS-current-source array and an NMOS current mirror. The PMOS-current-source array is built by connecting the outputs of 4 NAND gates together, and with an input of each NAND gate connected to a digital control bus and the other input connected to D4. The NMOS current mirror is built by connecting one input of a NAND gate to its output and the other input to logic-1. The proposed current-output DAC is combined with a current-starved ring oscillator using NAND gates as its delay cell to form a digitally controlled oscillator, which maintains high current-domain linearity. The simulated DAC power consumption is less than 60μW.

Injecting a stream of narrow pulses into the oscillator is a widely used approach to improve its jitter performance by resetting the oscillator at every reference cycle. However, the injection pulse width requires additional calibration to guarantee robust operation over environmental variations, since an excessively narrow pulse width causes a failure to lock or an over-designed pulse width causes a strong periodic disturbance to oscillator phase and amplitude-degrading deterministic jitter. As shown in Fig. 15.1.4, an edge-injection technique is applied to avoid the injection pulse width issue [7]. Assuming that the oscillator frequency is *N* times higher than the reference frequency, an inverted injection-window signal forces the oscillator to stop oscillating at the rising edge of the injection-window signal. Then, an injection signal with clean edge is forwarded to the oscillator and replaces the noisy edge V_y to prevent jitter accumulation for several cycles. Finally, at the falling edge of the injection-window signal, the oscillator starts to oscillate again with its phase aligned to the phase of injection signal. Compared to conventional pulse injection, which requires a carefully timed injection-pulse width, the proposed edge injection style does not imply strict timing on the injection-window width. Phase replacement and alignment can be done in one reference cycle.

The fully synthesizable PLL is fabricated in a 65nm digital CMOS process. The PLL occupies 110×60μm². The phase noise is evaluated by using a signal-source analyzer (Agilent E5052B) and the spectrum is measured using a spectrum analyzer (Agilent E4407B). The measured frequency-tuning range of the PLL is 0.39GHz to 1.41GHz. At 0.9GHz output, the power consumption is 780μW excluding output buffers from a 0.8V power supply. Fig. 15.1.5 shows the measured phase noise and output spectrum at 0.9GHz output using a 150MHz reference clock. The phase noise corresponds to a 1.7ps jitter when integrated from 10kHz to 40MHz.

Figure 15.1.6 shows a performance comparison table between this work and previously published synthesizable PLLs. The current PLL achieves the best performance in terms of power, jitter, and area. The figure of merit (FOM) is -236.5dB at 0.9GHz output frequency, where the FOM is defined as $10\log[(\sigma_t/1s)^2 \cdot (P_{DC}/1mW)]$, where σ_t is the integrated jitter, and P_{DC} is the DC power consumption. The chip micrograph is shown in Fig. 15.1.7.

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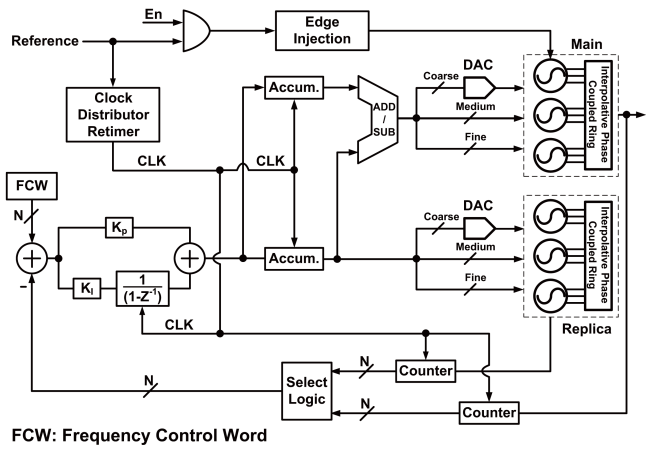

Figure 15.1.1: Block diagram of the proposed fully synthesizable PLL with a DAC and an interpolative phase-coupled oscillator.

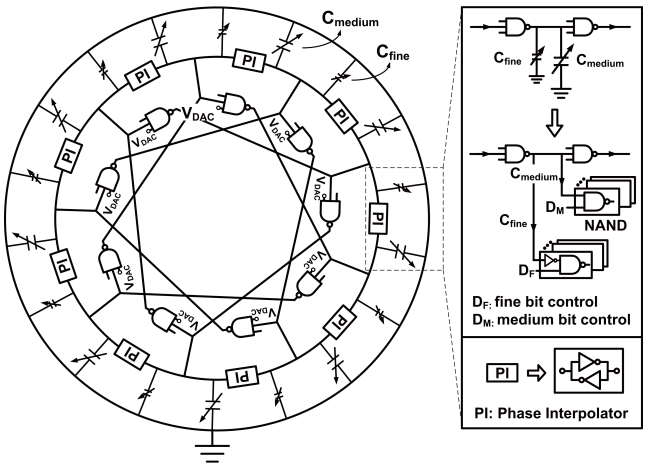

Figure 15.1.2: Block diagram of the interpolative phase-coupled oscillator.

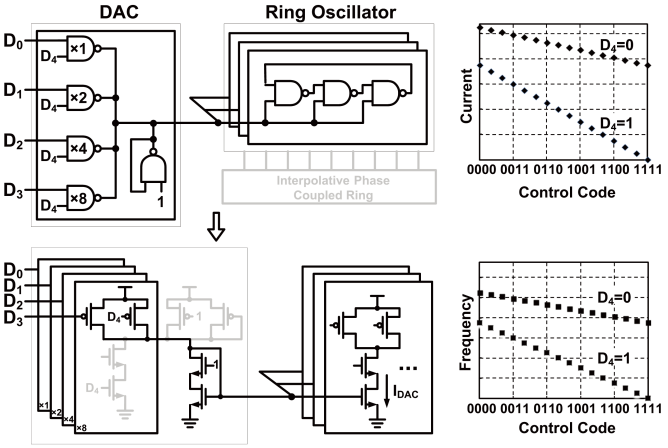

Figure 15.1.3: Conceptual diagram of the synthesizable DAC with a current-linear output.

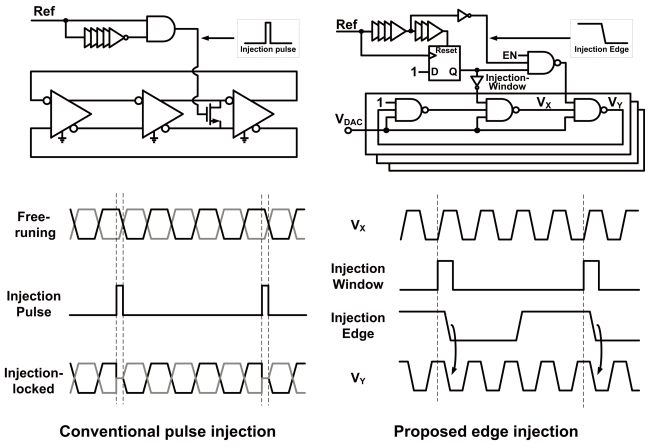

Figure 15.1.4: Block diagram and locking transient of the conventional pulse-injection locking and the proposed edge-injection method.

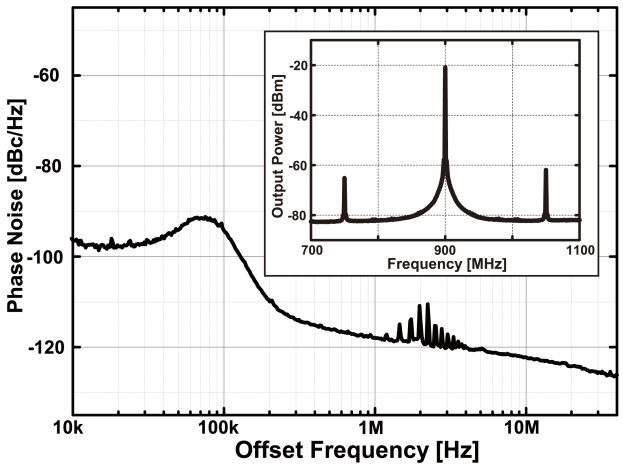

Figure 15.1.5: Measured phase noise and spectrum characteristics at a carrier of 0.9GHz.

	This work	[1]	[2]	[3]
Freq. [GHz]	0.39-1.41	1.5-2.7	0.25-1.65	0.4-0.46
Ref. [MHz]	40-350	10	25	40.3
Power [mW]	0.78 @900 MHz	13.7 @2.5 GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	**0.0066**	0.042	0.032	0.1
Normalized Area	1	6.36	4.84	15.15
Integ. Jitter [ps]	1.7	N.A.	30	N.A.
Jitter RMS [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	**-236.5**	-218.6*	-205.5	-214*
CMOS Technology	65nm	65nm	28nm	65nm
W/ custom cells?	No	No	Yes	Yes
Coarse Frequency Control	DAC	None	None	None

*FOM is calculated based on RMS jitter.

Figure 15.1.6: Performance summary and comparison with state-of-the-art synthesized PLLs.

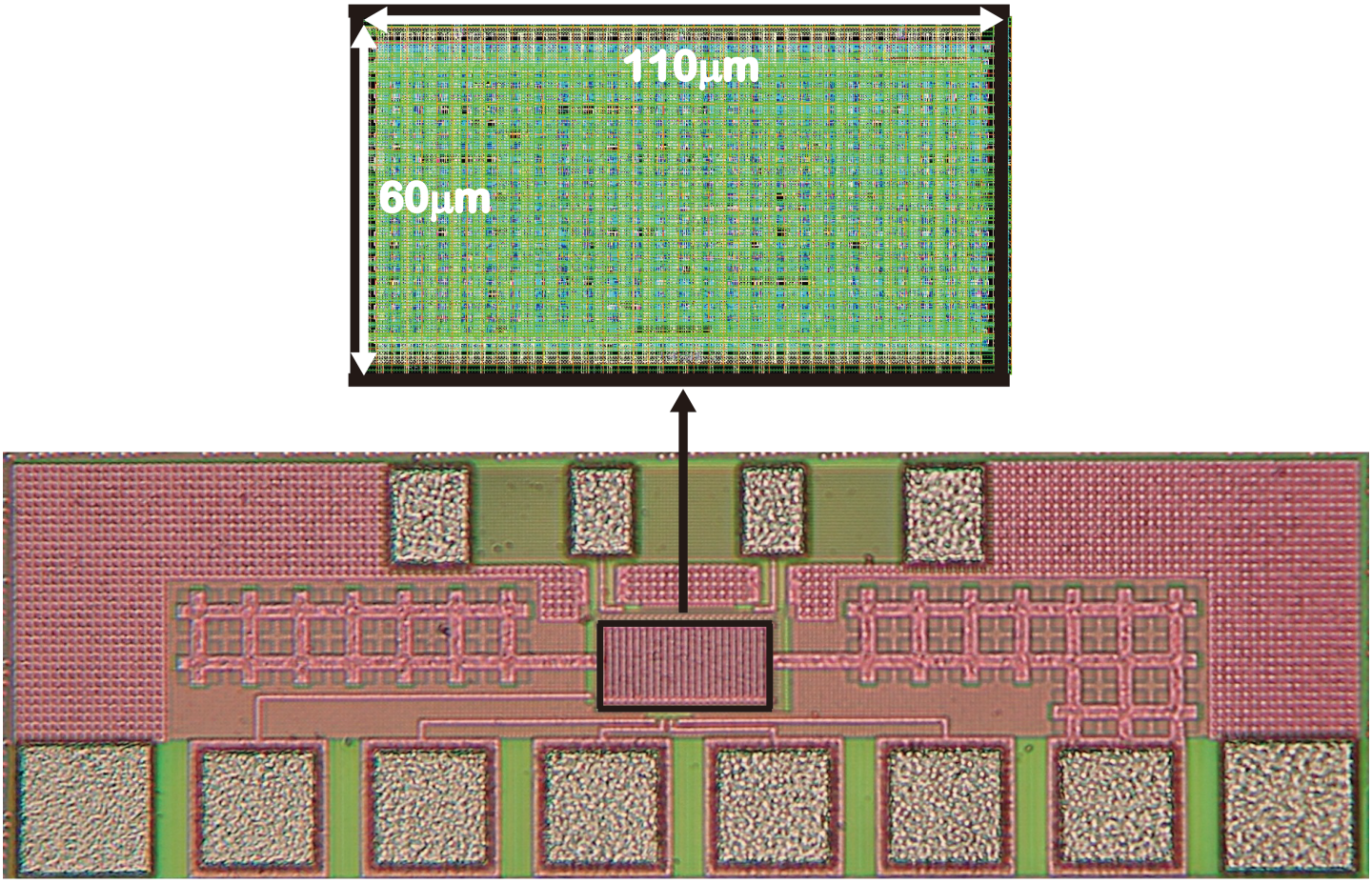

Figure 15.1.7: Die micrograph.