A Characterization Method of On-Chip Tee-Junction for Millimeter-Wave CMOS Circuit Design

Korkut Kaan Tokgoz, Nurul Fajri, Yuuki Seo, Seitarou Kawai, Kenichi Okada and Akira Matsuzawa
Tokyo Institute of Technology, Department of Physical Electronics
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo, 152-8552, Japan, E-mail: korkut@ssc.pe.titech.ac.jp

1. Introduction

The unlicensed band at 60 GHz attracts applications for high-data-rate communications. Moreover, CMOS offers the advantages of cost, and monolithic implementation for high-data-rate transceiver (TRX) systems [1]. In order to successfully implement these systems, one has to have accurate device models, beforehand. The characterization approaches for devices having two-ports, or more number of ports differ. These phases are relatively easy for two-port measurements compared to more number of port measurements, e.g. four-port, and hence device characterizations are much more accurate [2]. Considering these issues, a characterization approach for tee-junction, terminating the unmeasured port with a short circuited transmission line (TL) is developed and presented in this work.

2. Structures and Method

The illustration of tee-junction is given in Fig. 1. The structure used for tee-junction characterization is presented in Fig. 2(a). The assumed tee-junction model is represented in Fig. 2(b). Extra TLs are de-embedded so that the remaining part of the tee-junction can be assumed as lumped constant. Z_{11}-Z_{12} directly gives "Z_1" model parameter in Fig. 2(b). The port 3 of Tee-junction (Fig. 1) is terminated with 2.5 µm short-circuited TL, as shown in Fig. 2(a). Z_{12} is equal to series connection of model parameter "Z_2" and impedance of 8 µm short-circuited TL named as Z_{short} in Fig. 2(b). This extra 5.5 µm TL is considered in Z_{short} for "Z_2" to be assumed as lumped constant. Hence, "Z_2" can be calculated as Z_{12}-Z_{short}. Moreover, the extra lengths used for de-embedding and short circuited TL are determined using the results of verification structure given in Fig. 2(c).

3. Results

The structures of Fig. 2(a) and (c), are fabricated using 65 nm CMOS process. Using model and TL models, structure is reconstructed (Fig. 2(a)) and compared with measurement results from 1 to 110 GHz. Fig. 3(a) represents the input return losses (RL), and Fig. 3(b) represents the insertion losses (IL) for model and measurement results. They coincide perfectly. In Fig. 3(c) and (d) RL and IL results comparison for verification structure Fig. 2(c) are presented. The models are well matched in the entire frequency band.

4. Conclusion

In this work, an approach to characterize tee-junction is presented. The model and measurement results are well-matched from 1 to 110 GHz.

Acknowledgements

This work was partially supported by MIC, SCOPE, MEXT, STARC, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1] K. Okada, *et al.*, *ISSCC*, 2014 pp. 346-347.
[2] K. K. Tokgoz, *et al.*, *SSDM*, 2013, pp. 900-901.

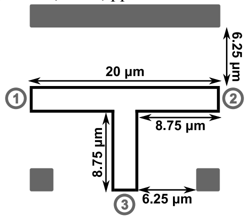

Fig. 1. Geometrical specifications and port assignment for Tee-junction (gray areas represent ground planes).

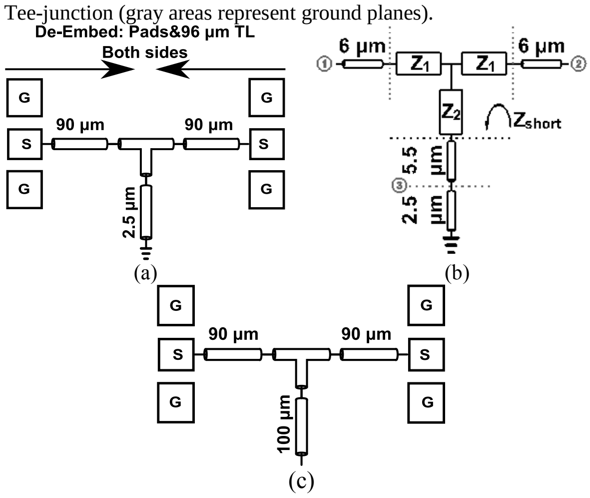

Fig. 2. Illustration of (a) structure for characterization, (b) characterization model, and (c) structure for verification.

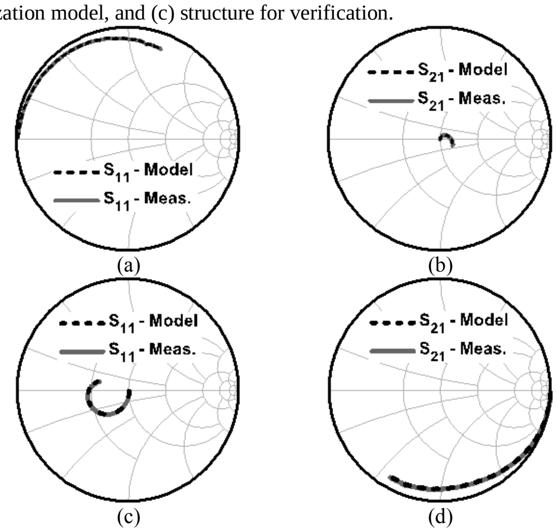

Fig. 3. S-parameter comparison between measurements (gray lines) and models (black dotted lines); (a) RL for Fig. 2(a), (b) IL for Fig. 2(a), (c) RL for Fig. 2(c), and (d) IL for Fig. 2(c) (all results are from 1 to 110 GHz).