

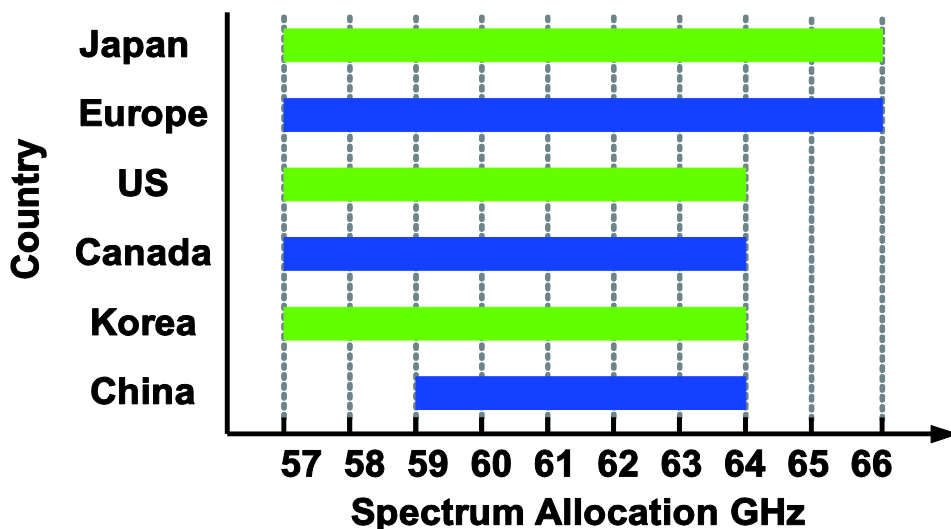
A Dual-Step-Mixing ILFD using a Direct Injection Technique for High-Order Division Ratios in 60GHz Applications

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- **Motivation**
- **Conventional ILFDs**
- **Proposed Dual-Step-Mixing ILFD
using a Direct Injection Technique**
- **Performance Comparison**
- **Frequency Drift over PVT variations**
- **Integration with 20GHz PLL**
- **Conclusion**

- 9-GHz unlicensed bandwidth at 60 GHz
- Several Gbps wireless communication



IEEE 802.11ad/WiGig



IEEE 802.15.3c



Wireless HD

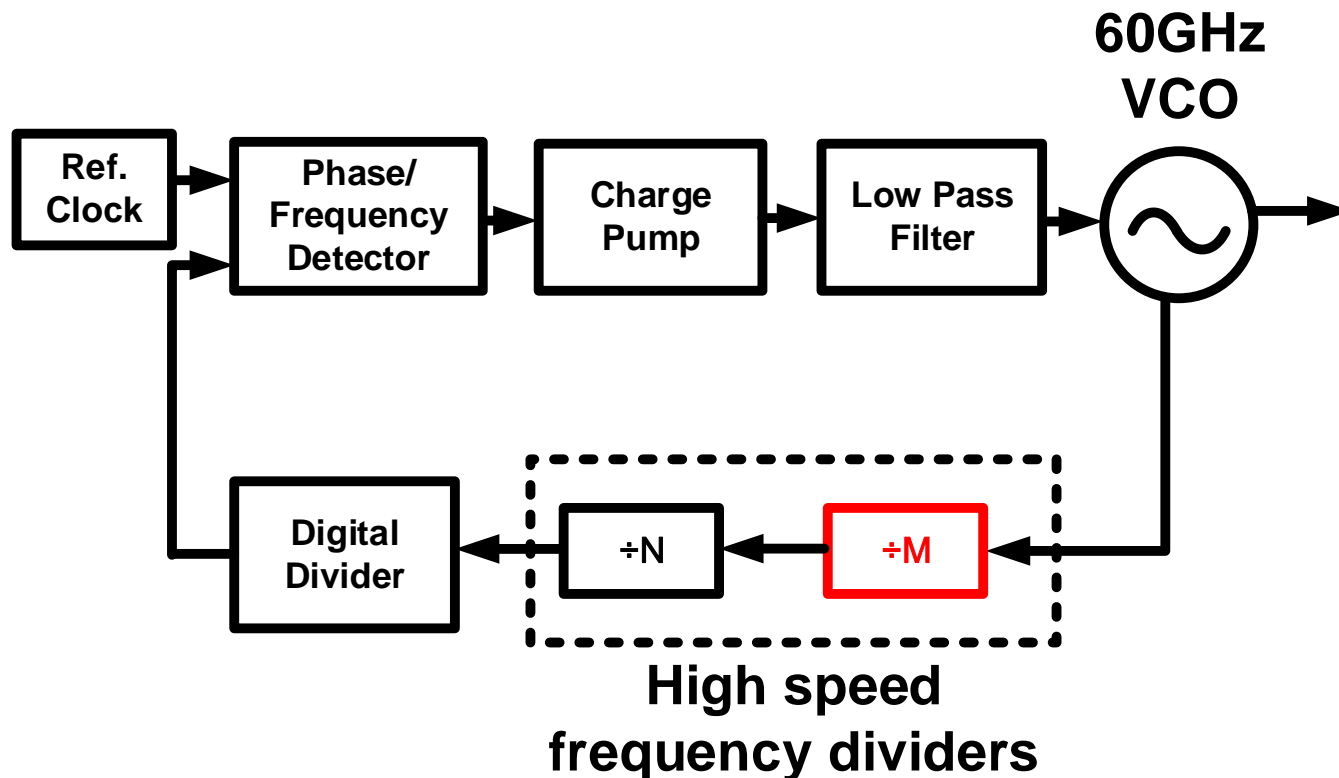


ECMA-387



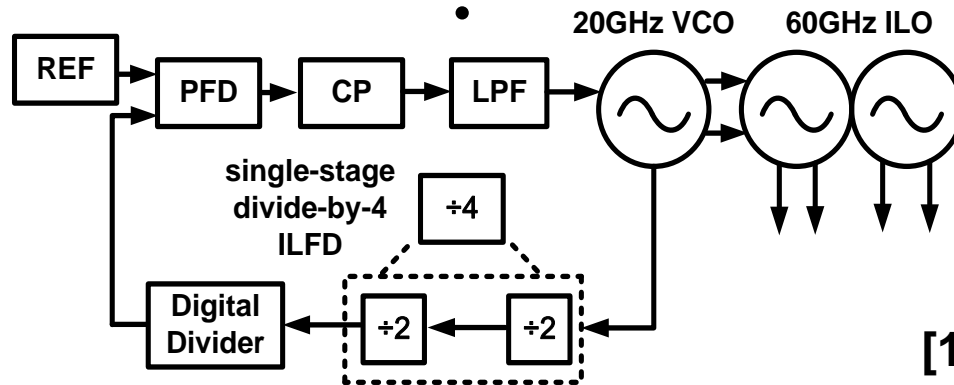
ISO/IEC13156

[1] <http://www.tele.soumu.go.jp>



- Direct 60GHz VCO suffers from inferior phase noise due to Q of tank at 60GHz
- Power-hungry frequency divider is required

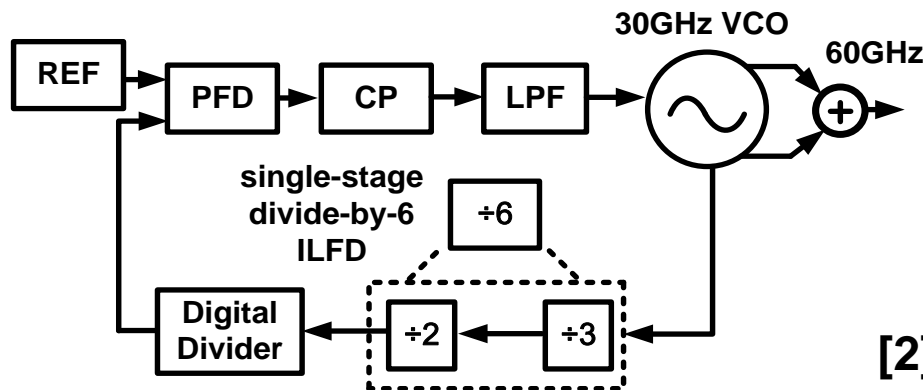
■ Sub-harmonic injection



- 2 divide-by-2 CML divider consumes 15mW (40% of PLL)

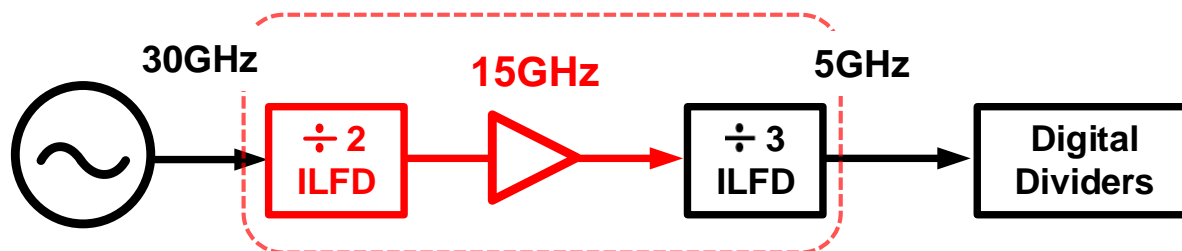
[1] A. Musa, *et al.*, JSSC 2011

■ 60GHz push-push VCO

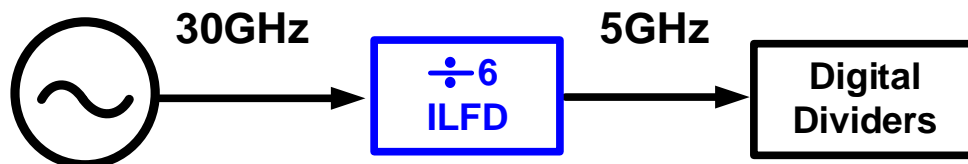


- Divide-by-3 ILFD + divider chain consumes more than 50% of PLL

[2] T. Tsukizawa, *et al.*, ISSCC 2013



- Large power
- Locking range mismatch

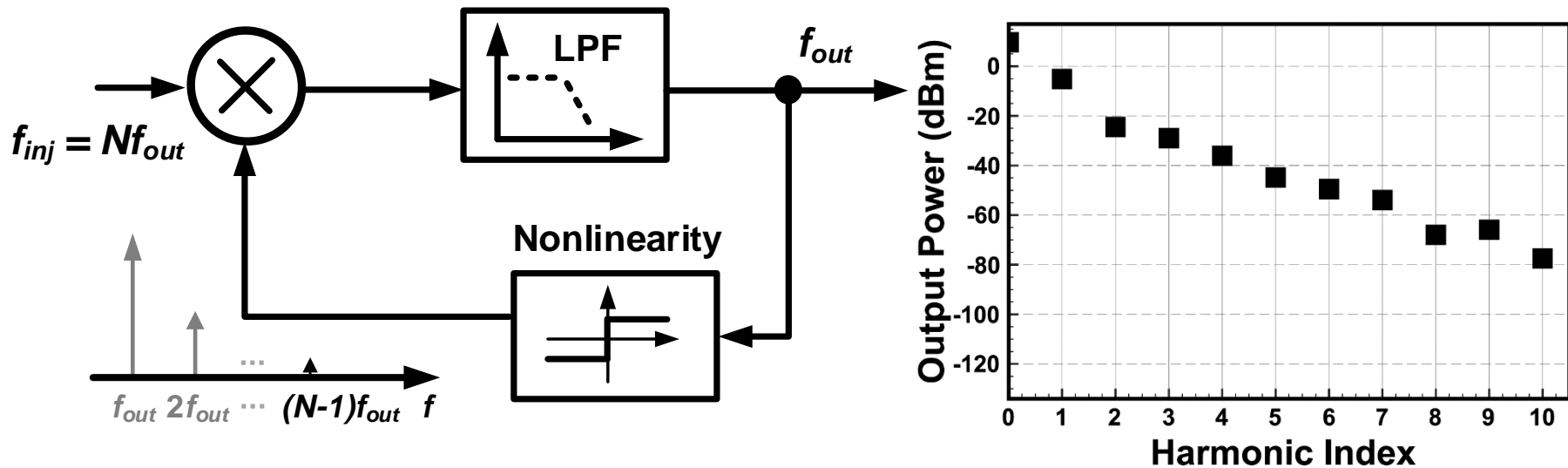


- Narrow locking range

20-GHz PLL needs a divide-by-4 ILFD

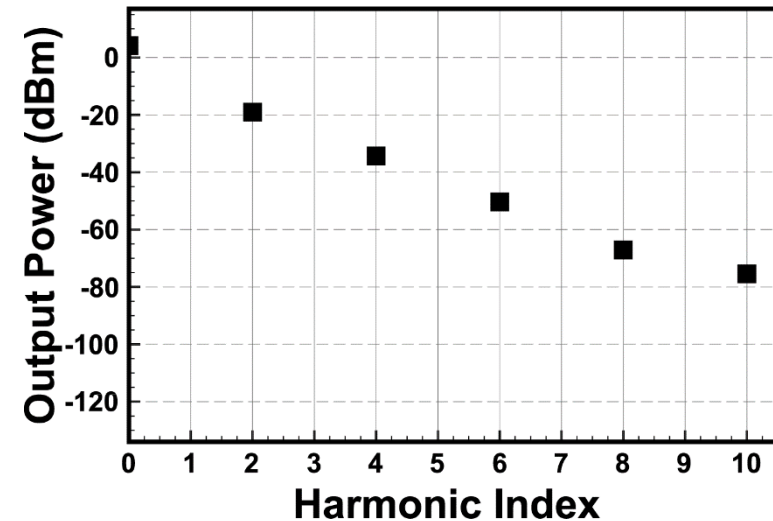
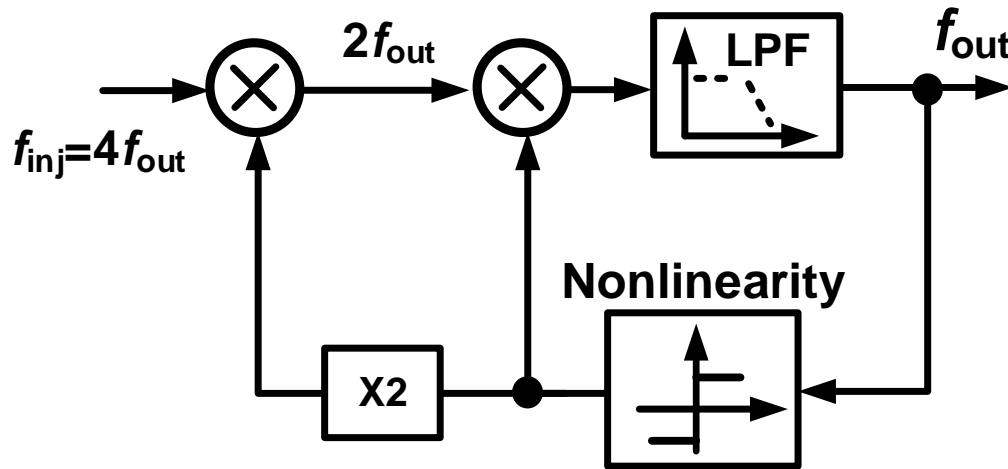
30-GHz PLL needs a divide-by-6 ILFD

- A technique to increase locking range of high-order-division in ILFDs is necessary



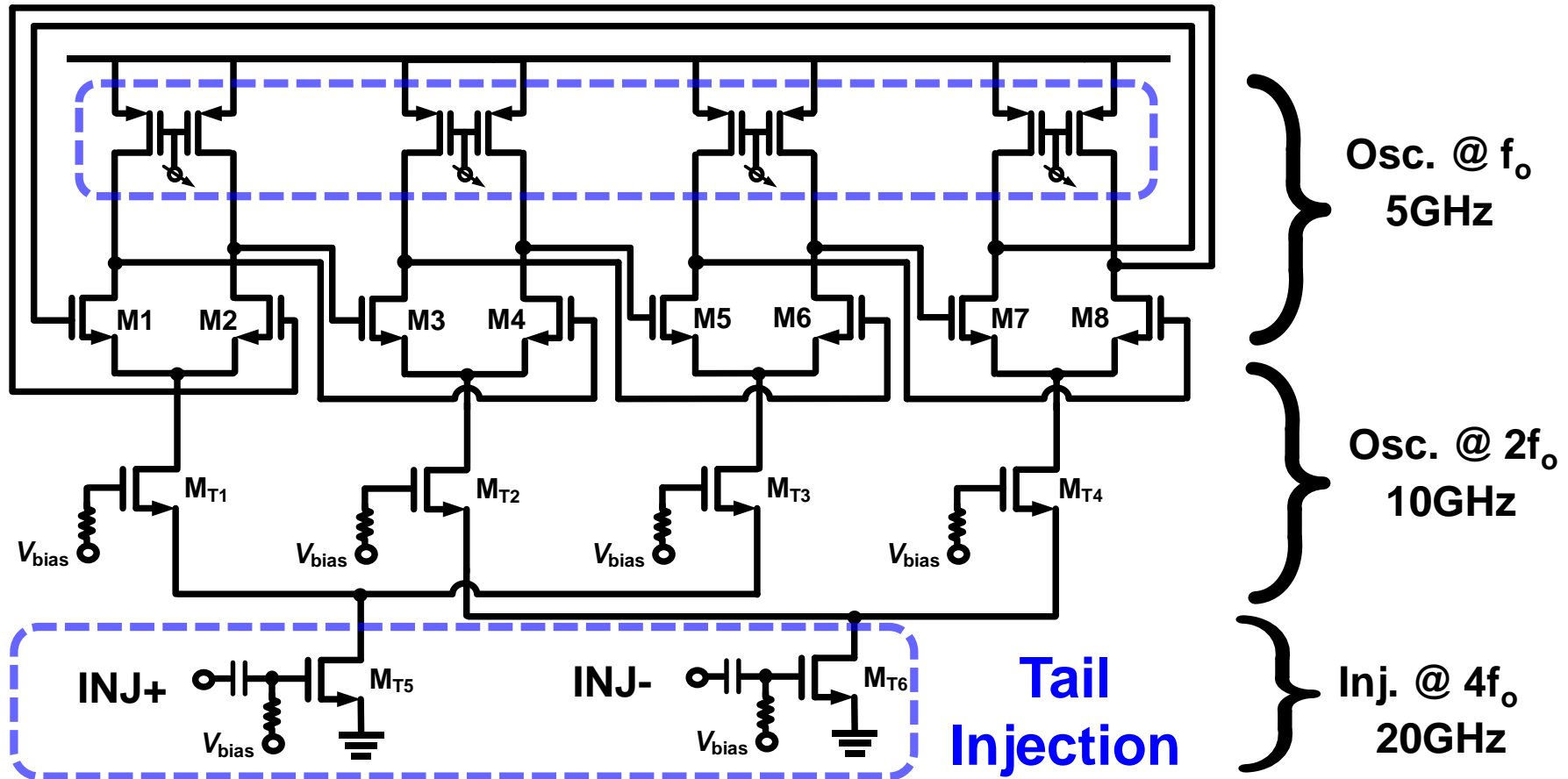
Divide by N directly in one step

- Injection signal is directly divide by N
- Low power consumption
- Narrow Locking range



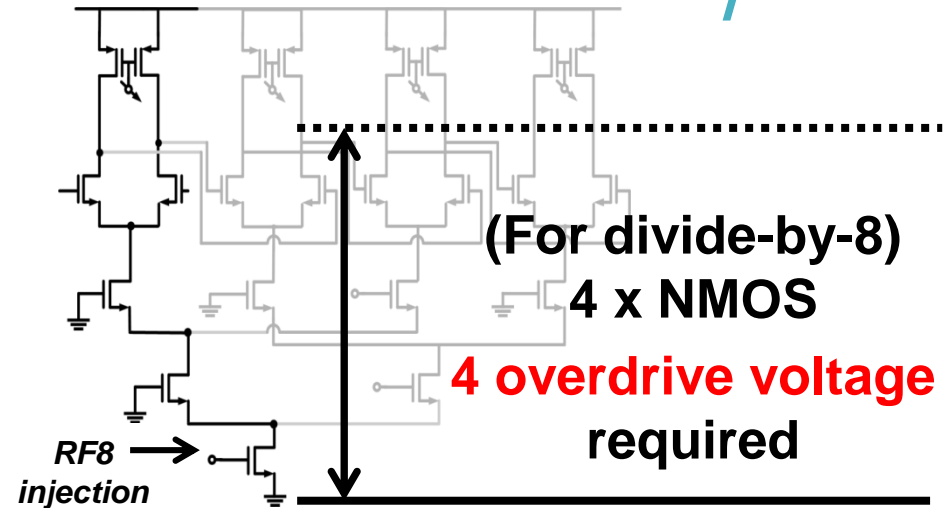
- Multi-step mixing mechanism divide-by- 2^n operation, e.g., 2, and 4
- Locking range is enhanced through the use of stronger harmonics

- High division ratio ILFD by reusing higher harmonic in cascoded configuration



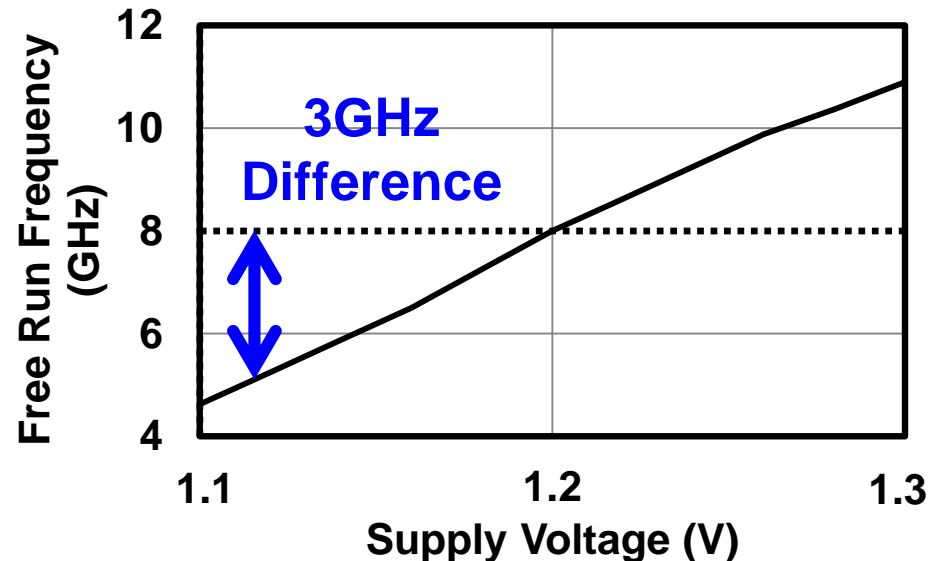
■ Large headroom

- Impractical for low voltage design
- For 1.2 V supply, higher than 8 division is hard to be achieved

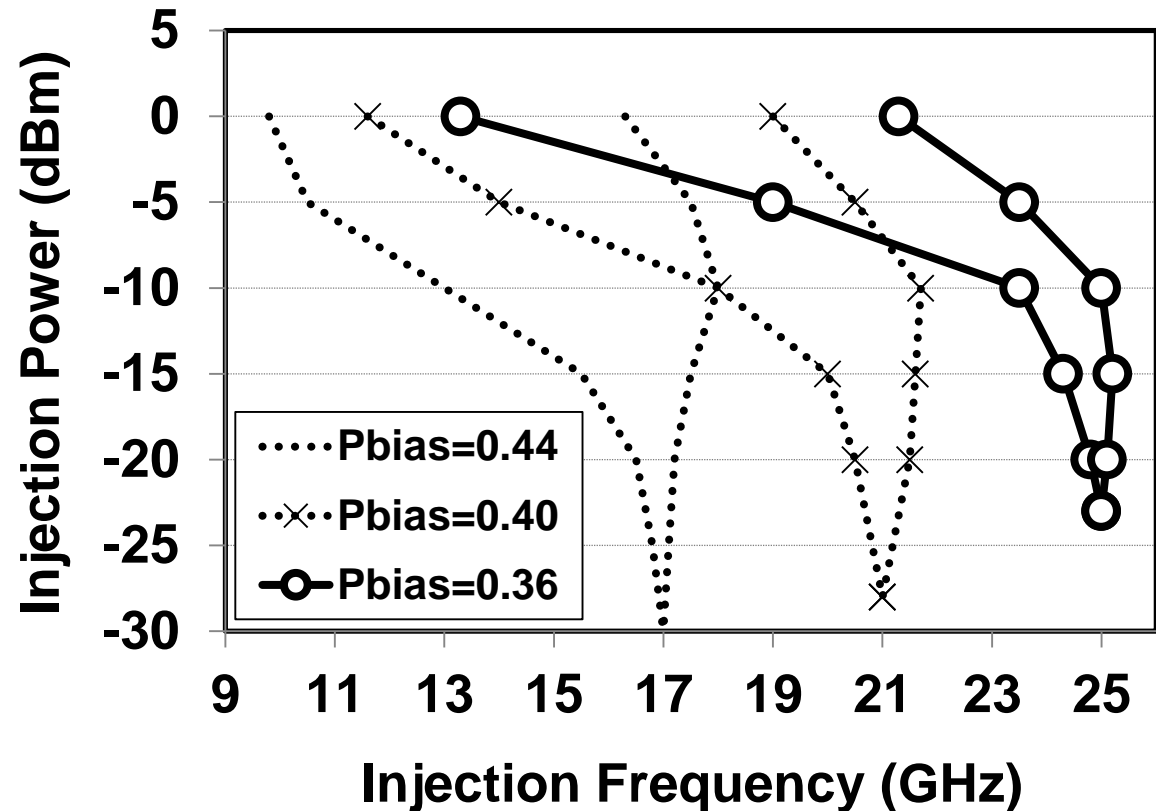
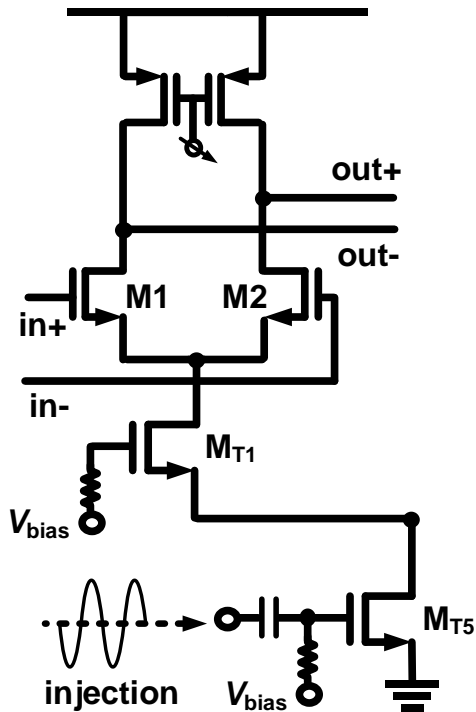


■ Sensitive to PVT due to PMOS tuning

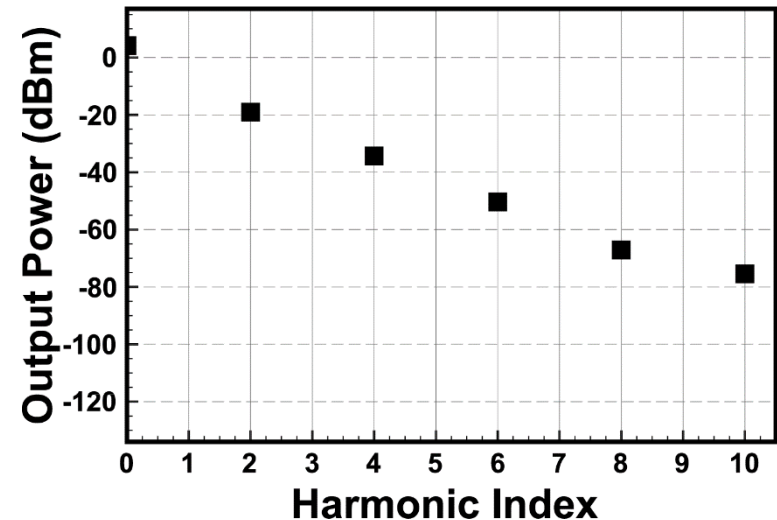
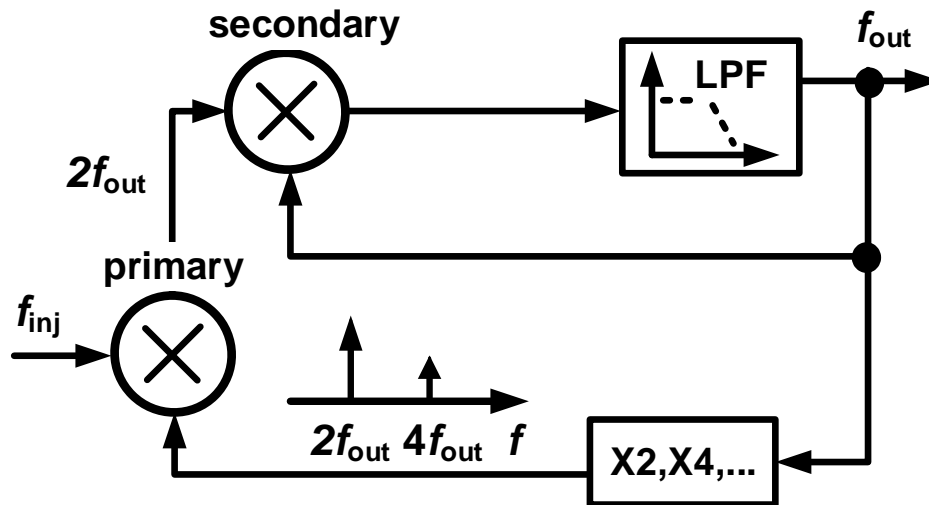
- $\pm 10\%$ supply pushing leads to a drift of free running frequency



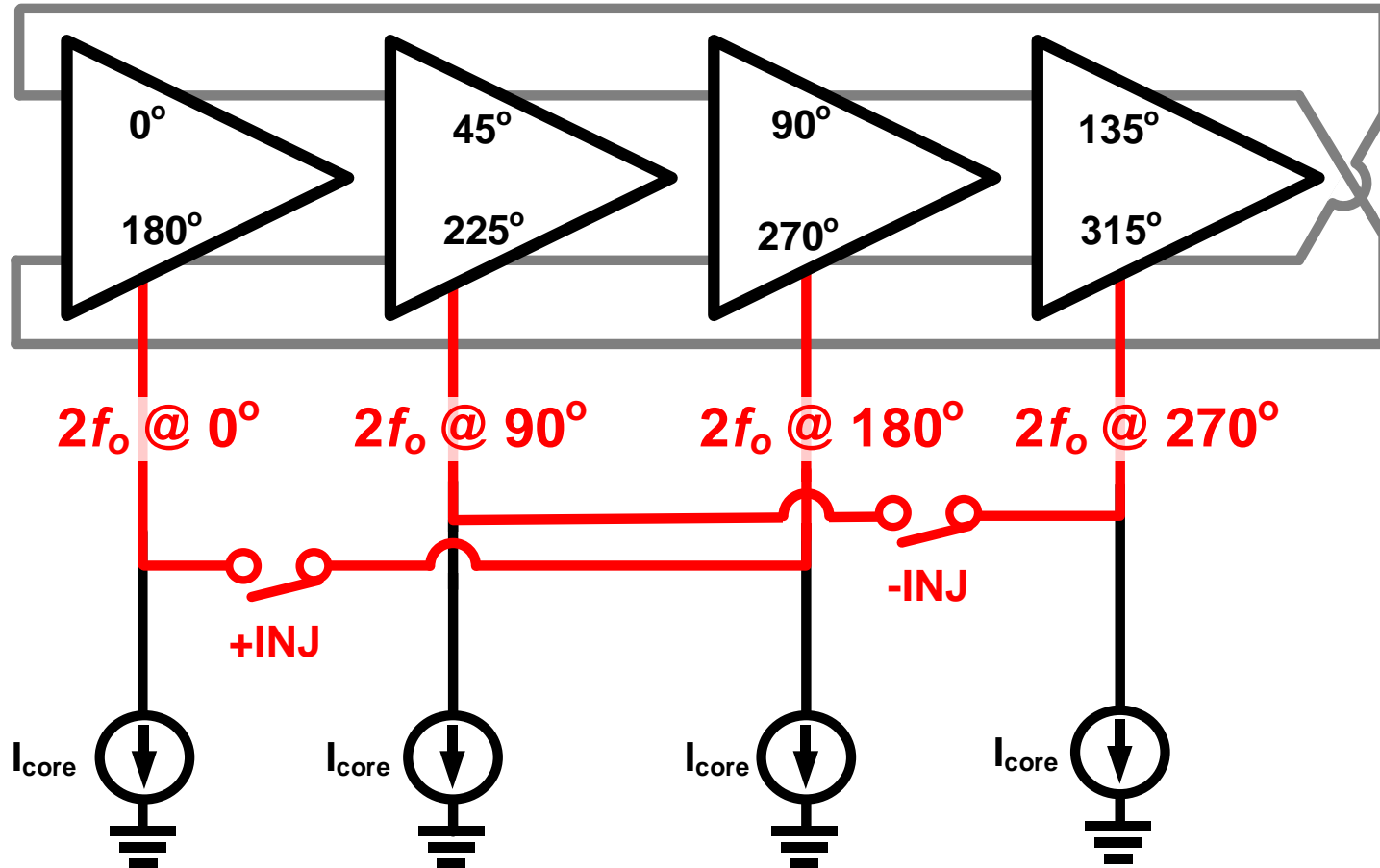
■ Asymmetric Locking Range



Intrinsic free-running frequency of ILFD is
sensitive to large injection signal

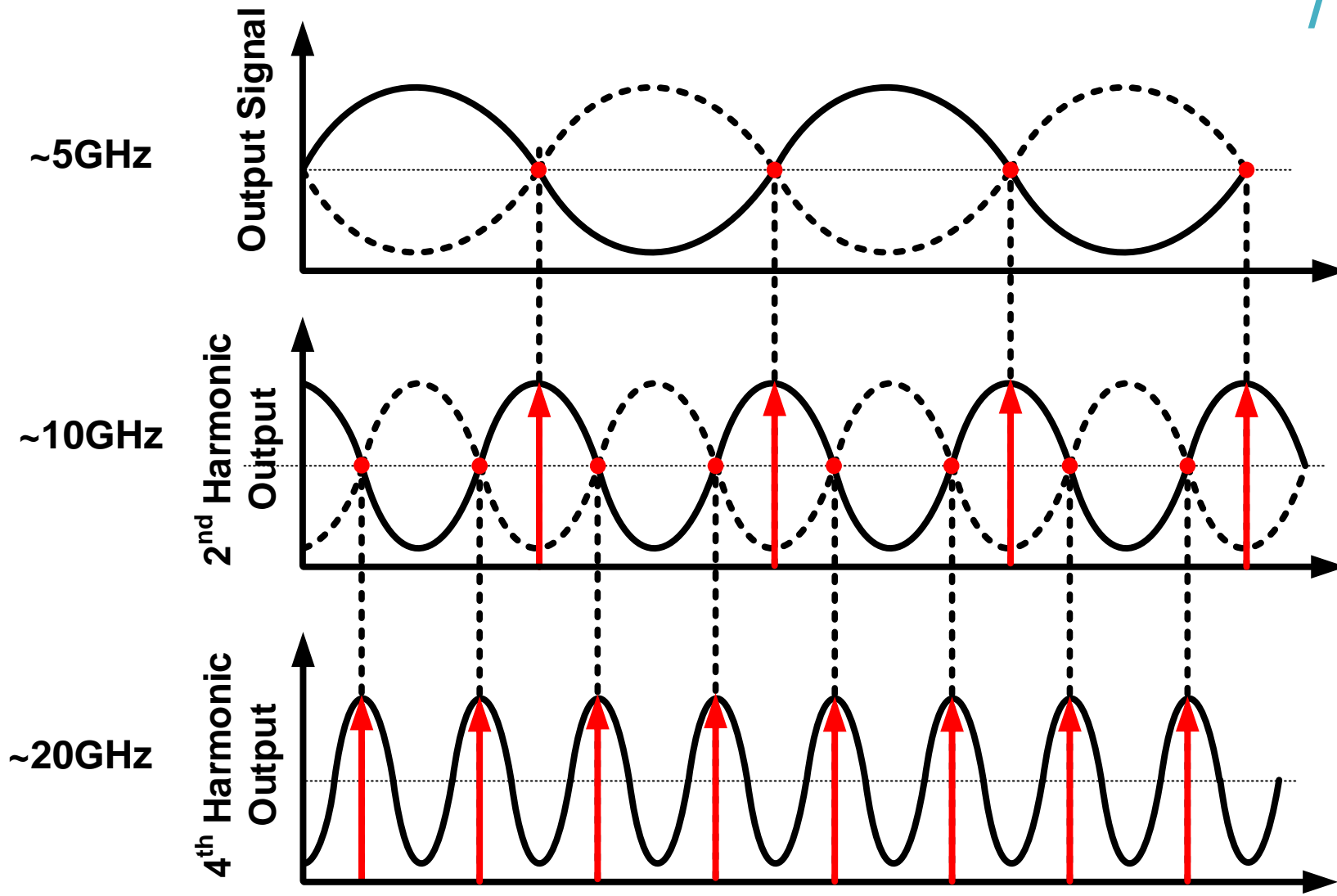


- Dual-step mixing mechanism for divide-by-4 and divide-by-6 operation



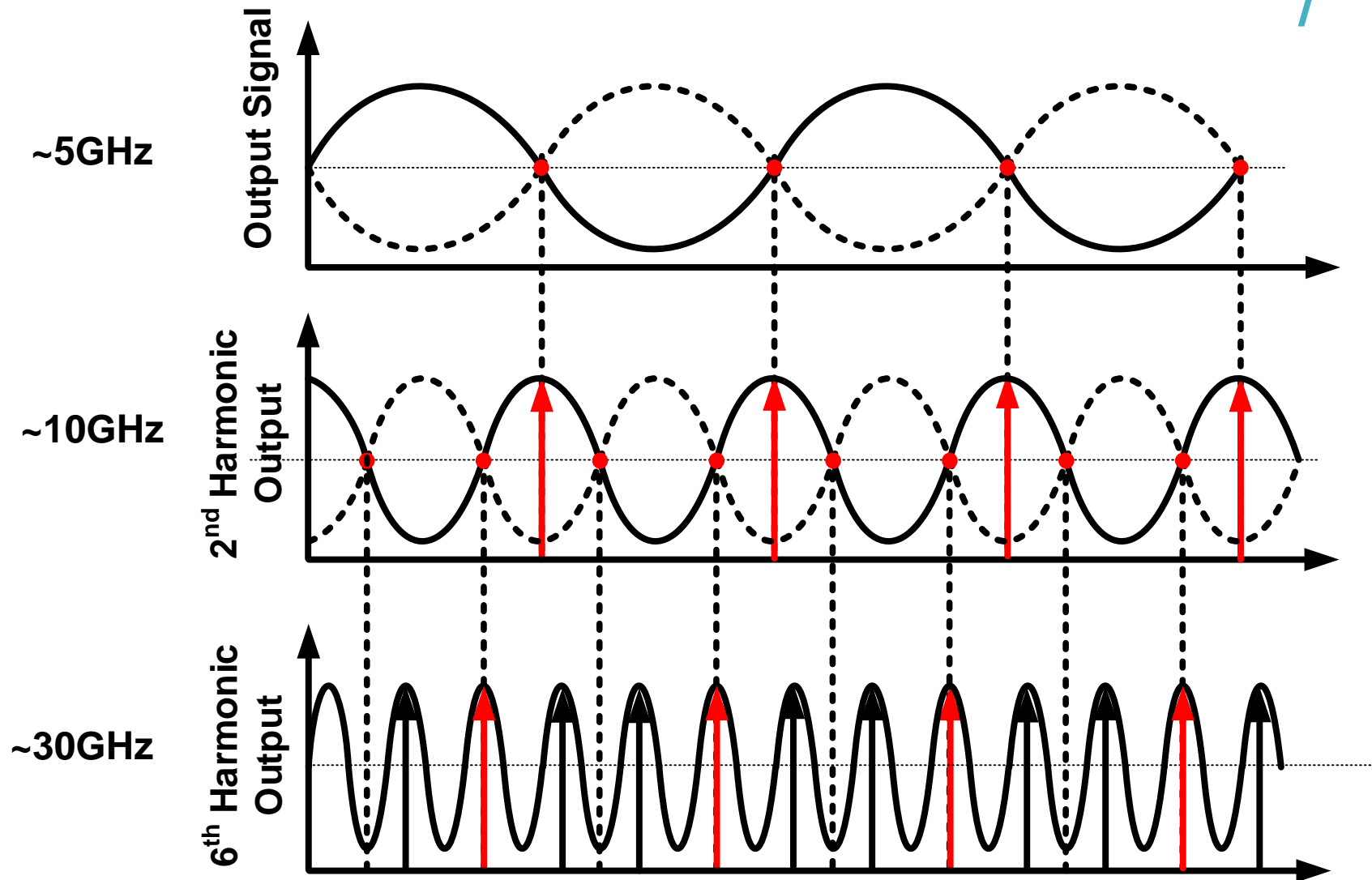
Dual-Step Mixing with Second Harmonic Direct Injection

Divide-by-4 Operation

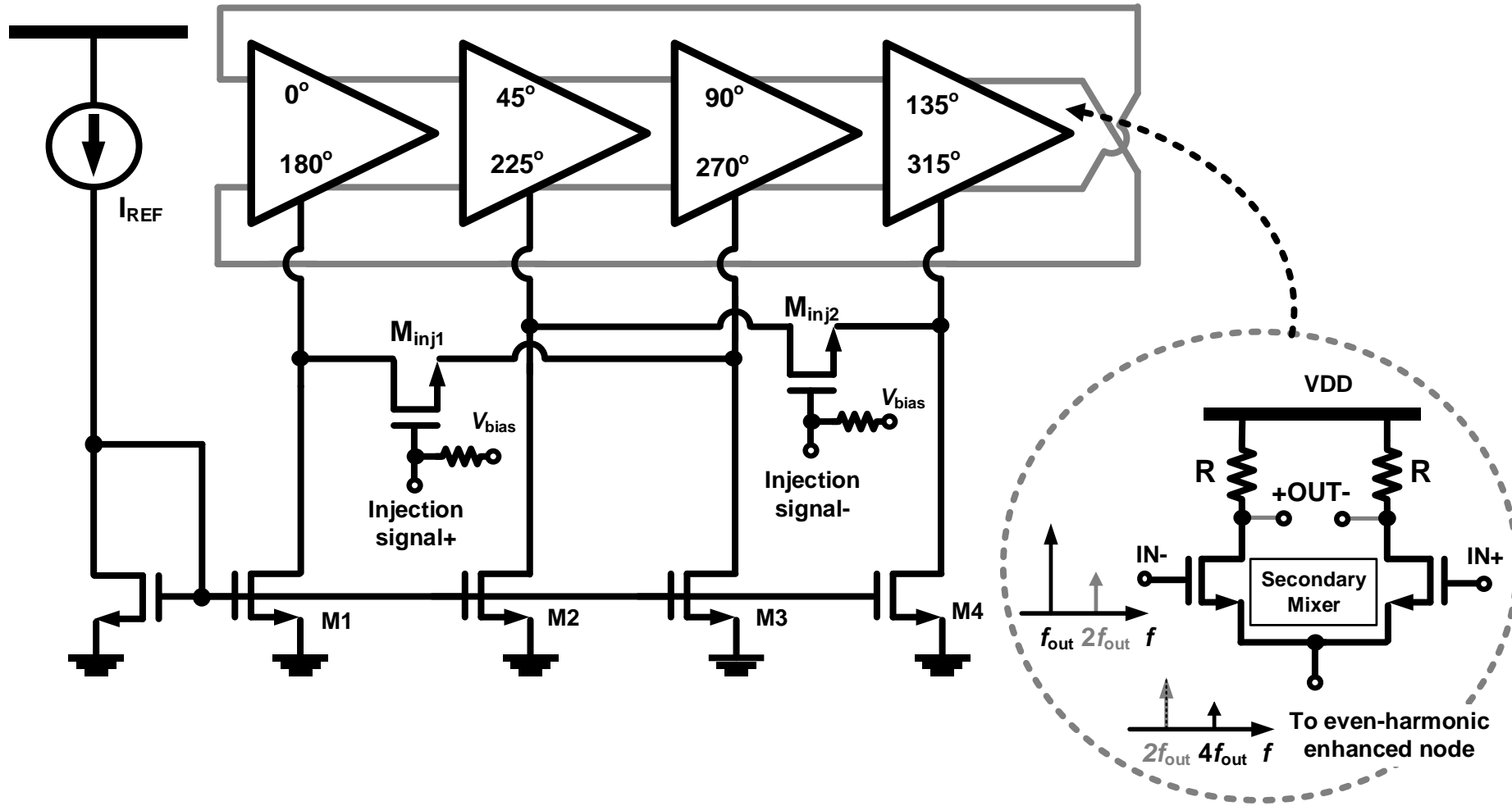


Locked State of Divide-by-4 operation

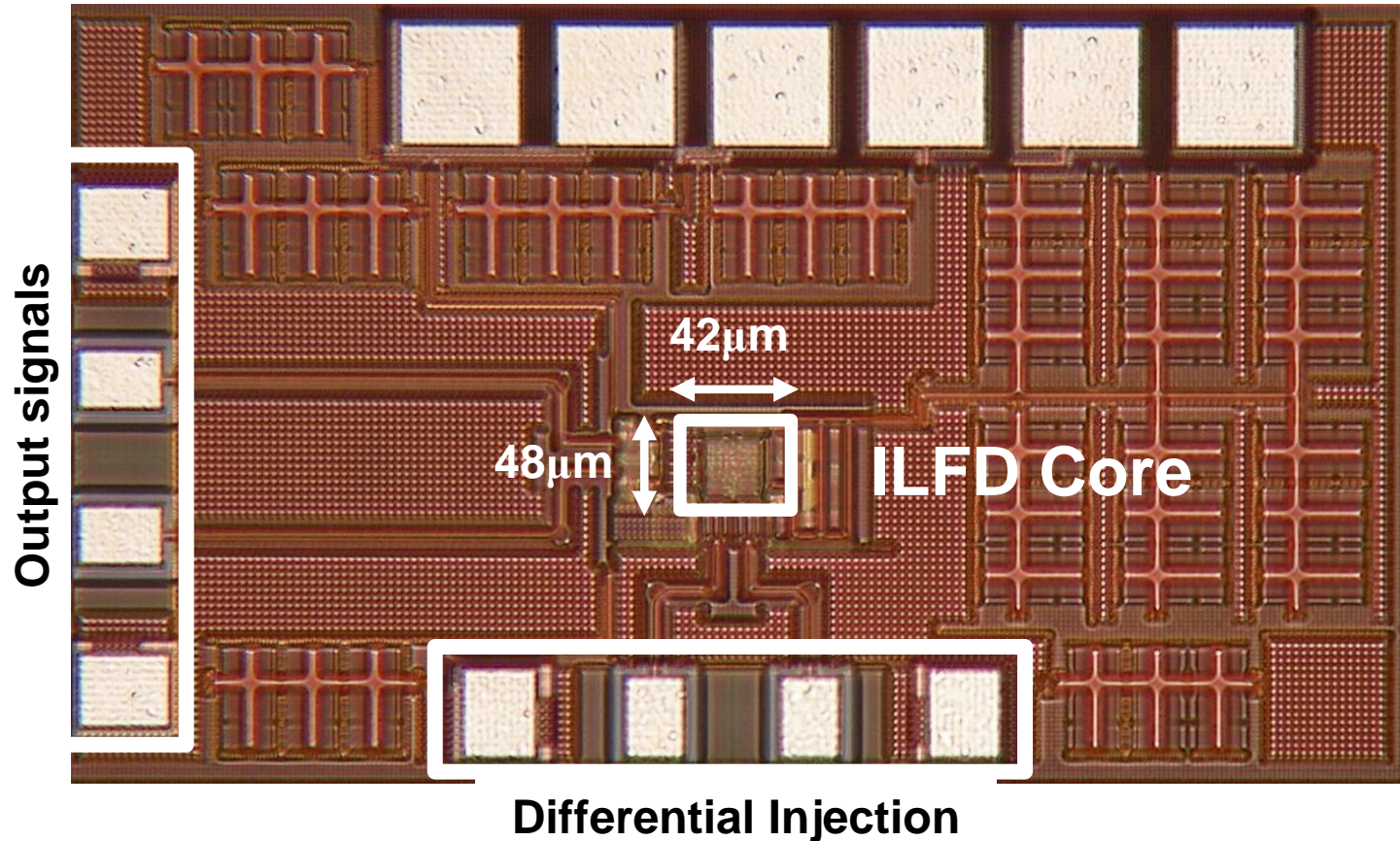
Divide-by-6 Operation



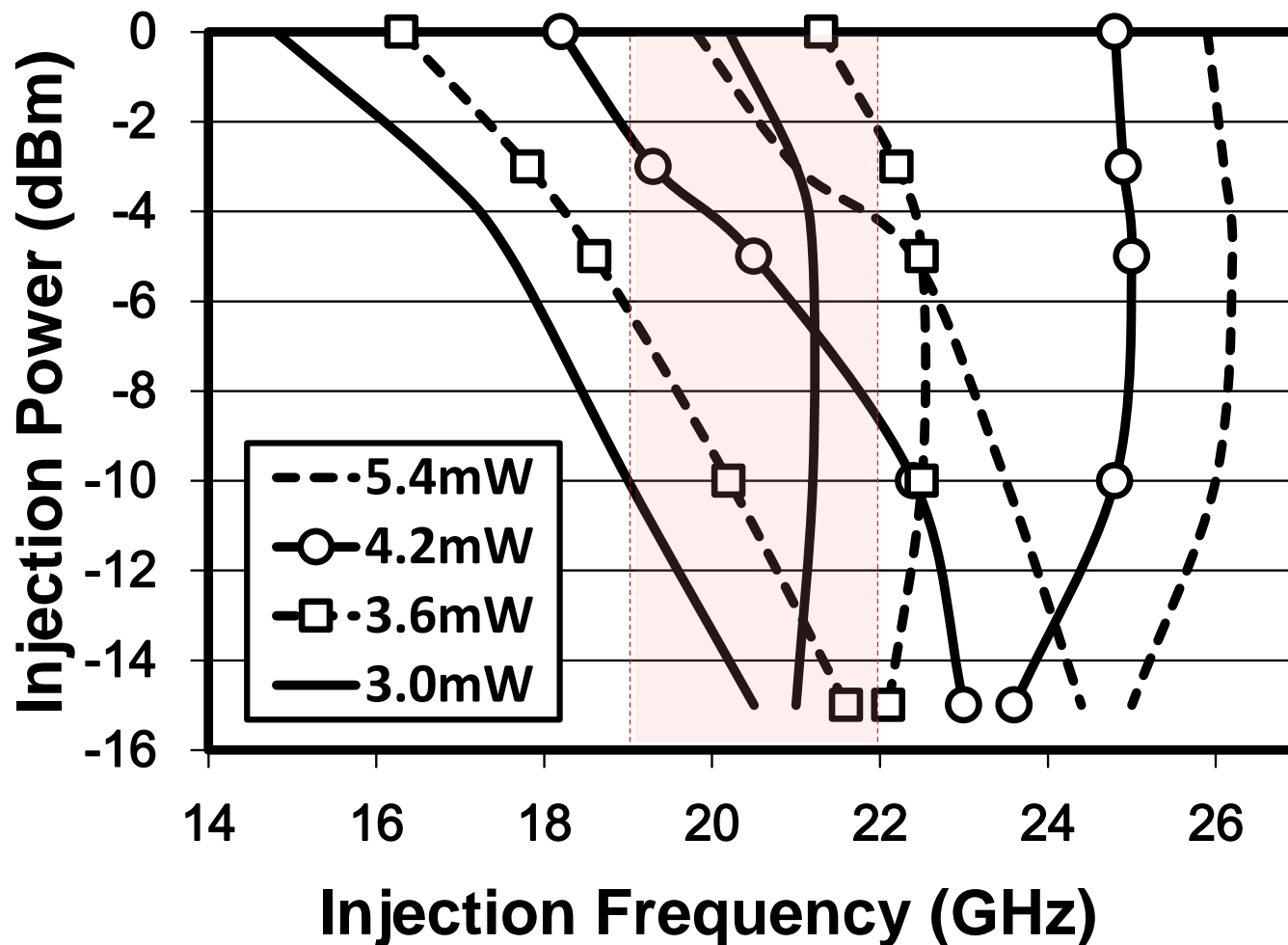
Locked State of Divide-by-6 operation



Schematic of the Proposed Dual-Step-Mixing ILFD using Even-Harmonic Direct Injection Technique



Technology	65nm CMOS
Core area	0.002mm²



Required frequency range for the 60-GHz wireless standards

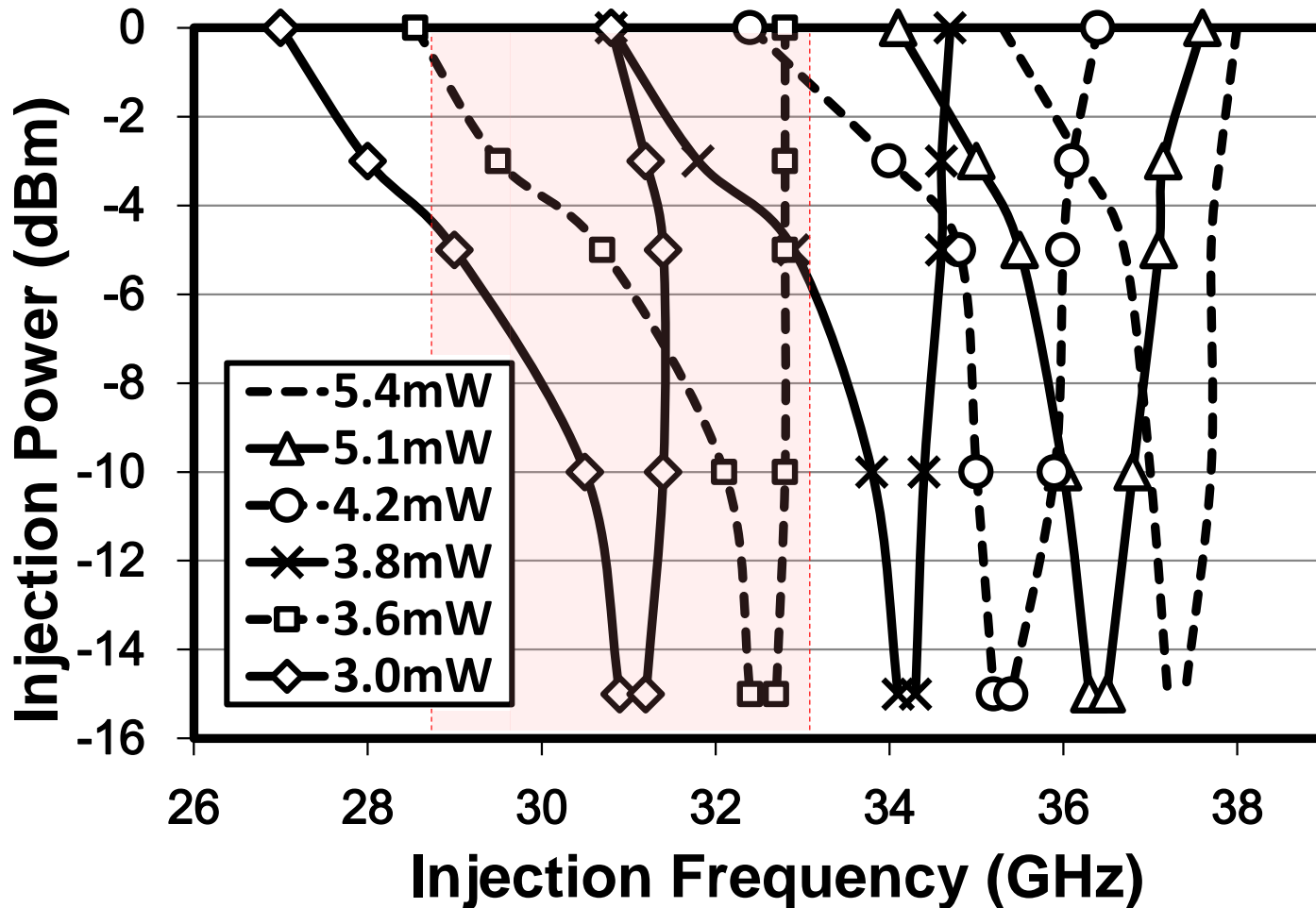
Divide-by-4 Performance Comparison 18

	Features	Div. Ratio	Locking Range* (GHz)	Locking Range* (%)	Power (mW)	FoM (%/mW)	Area (mm ²)
[4]	Direct mixing	4	22.6-28	21	8.3	3.5	0.140
[5]	Direct mixing	4	6.0-7.6	22	6.8	3.24	0.007
[6]	Direct mixing	4	31.0-41.0	27	3.3	8.18	0.002
[7]	LC Direct mixing	4	58.5-72.9	21.9	2.2	9.95	0.032
[8]	CML + LC ILFD	4	13.5-30.5	77.3	7.3	10.6	0.33
[9]*	Progressive mixing	4	13.4-21.3	31	3.9	7.95	0.003
This	Even-harmonic-enhanced	4	15.2-20.4	24.25	3.1	7.82	0.002

FoM=(%Lock Range)/(mW Power)

[4] A-SSCC'07 [5] RFIC'04 [6] ISSCC'06 [7] CICC'12

[8] MTT'11 [9] A-SSCC'11



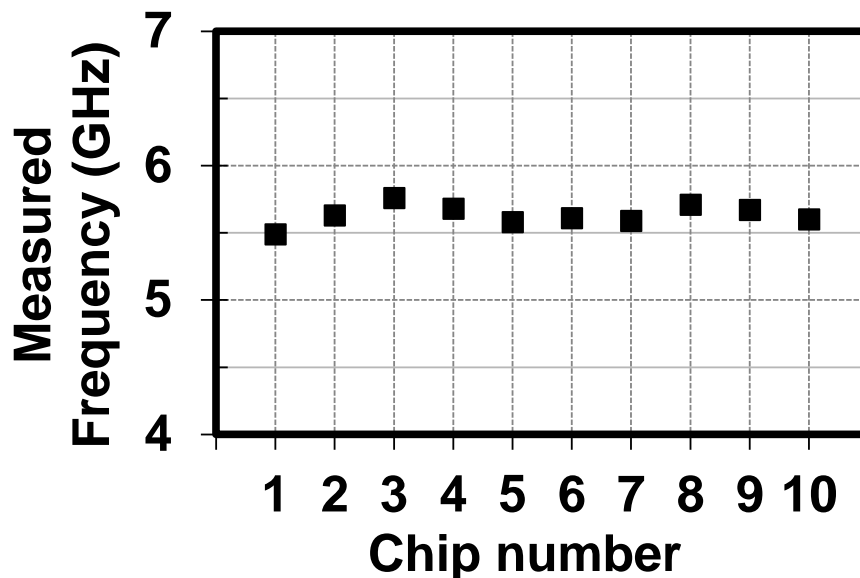
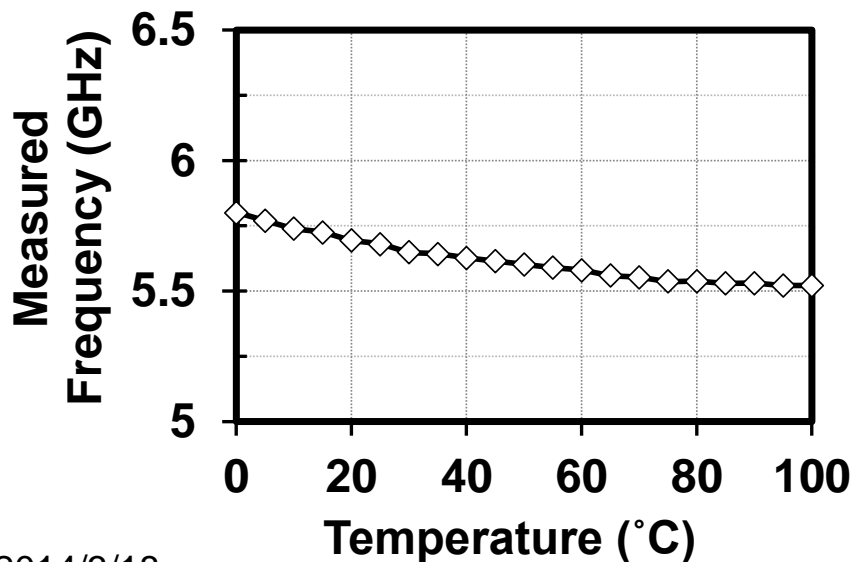
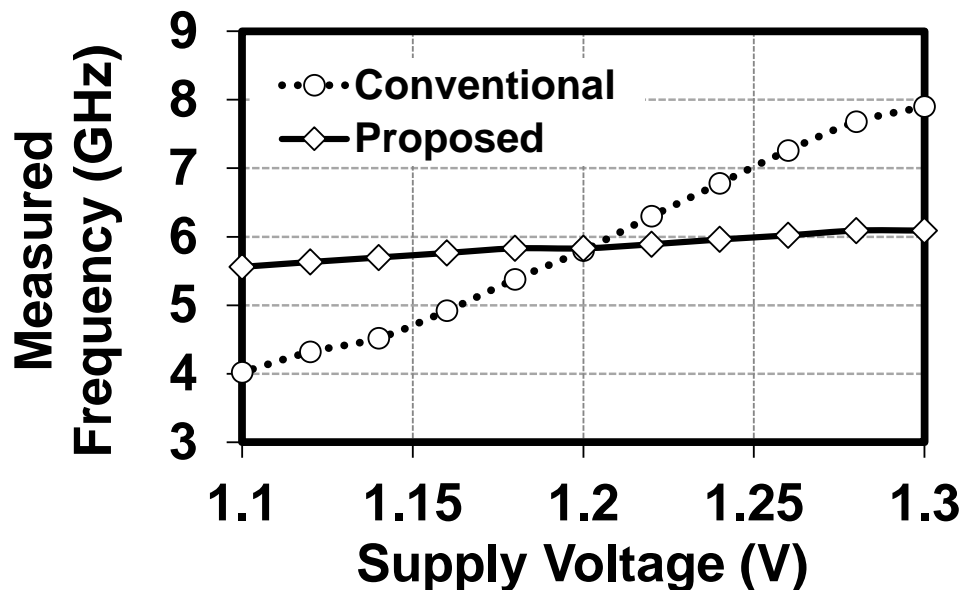
Required frequency range for the 60-GHz wireless standards

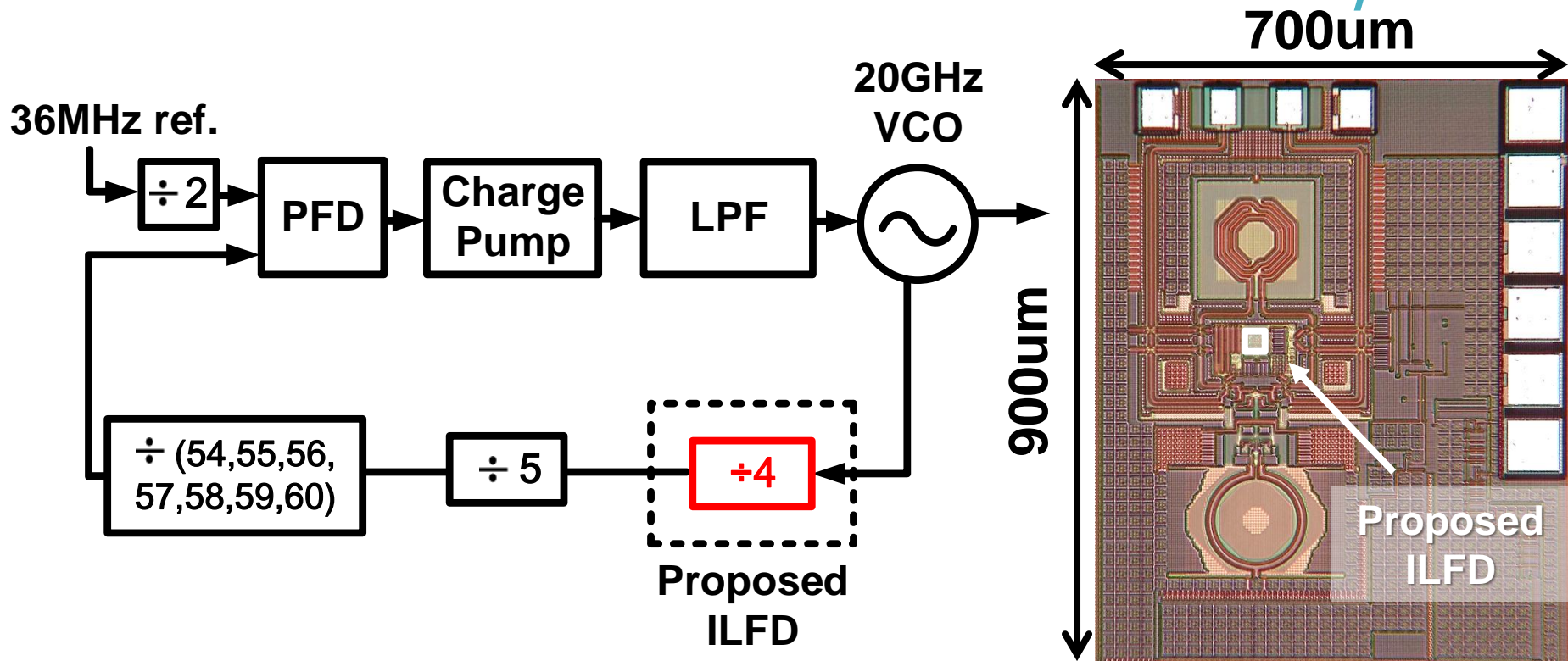
Divide-by-6 Performance Comparison 20

	Features	Div. Ratio	Locking Range* (GHz)	Locking Range* (%)	Power (mW)	FoM (%/mW)	Area (mm ²)
[4]	Direct mixing	3	21.7-24.9	13.7	8.3	1.7	0.140
[5]	Direct mixing	3	53.9-57.8	7.0	4.6	1.5	0.800
[6]	Direct mixing	6	141.0-144.3	2.7	14.0	0.2	1.160
[7]	Direct mixing	6	10.2-11.3	11.0	6.8	1.6	0.007
[8]	Direct mixing	6	14.6-15.4	5.0	12.5	0.4	0.300
[9]	Current reused ILFD	6	121.0-124.8	3.5	4.5	0.8	0.140
This	Even-harmonic-enhanced	6	27.7-32.0	13.2	3.1	4.0	0.002

FoM = (%Lock Range)/(mW Power)

[4] MTT'12 [5] ISSCC'09 [6] A-SSCC'11 [7] RFIC'04
[8] RFIC'05 [9] MTT'13

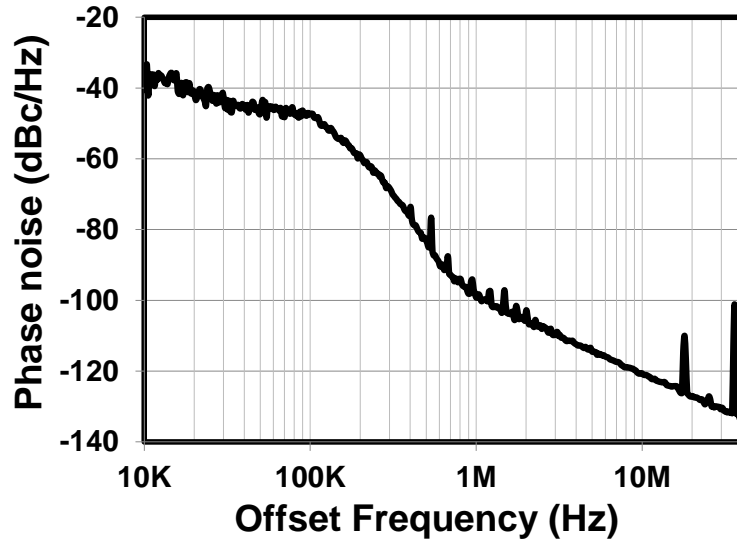




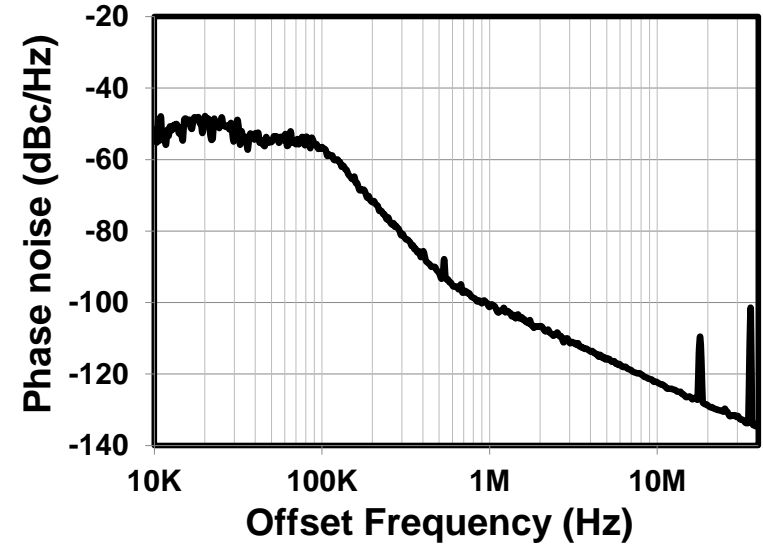
- Proposed ILFD consumes only 4.2mW
(Two cascading CML dividers consumes 14mW [1])

[1] K. Okada, et al., JSSC 2011

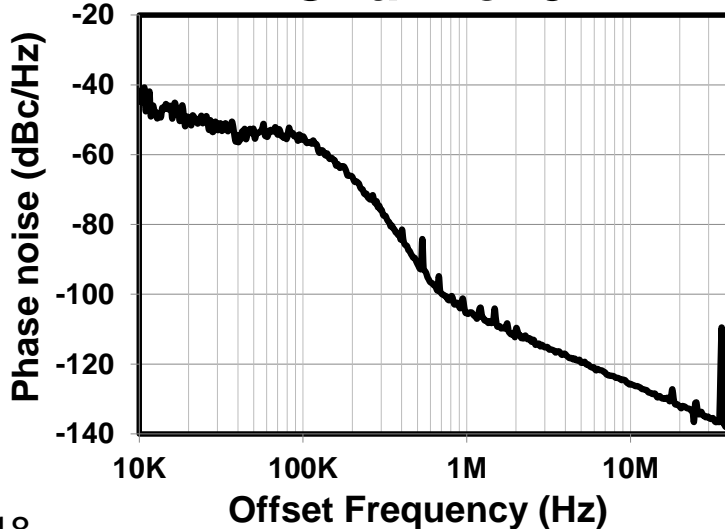
Channel 1



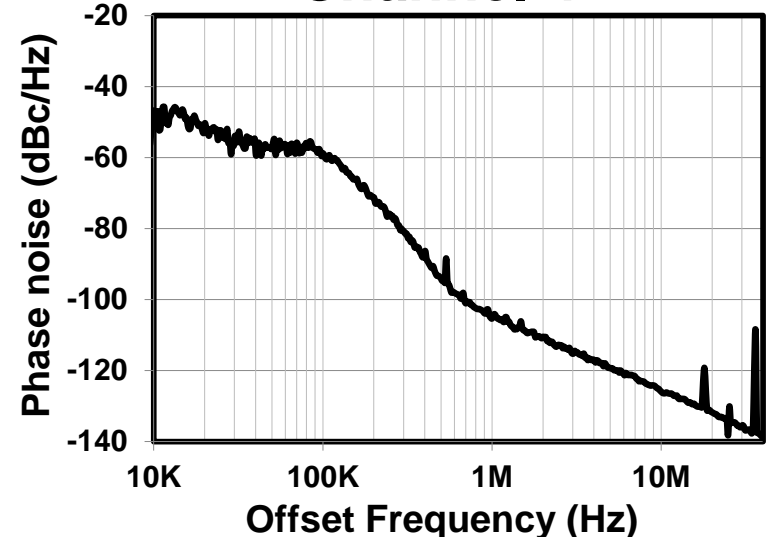
Channel 2



Channel 3



Channel 4

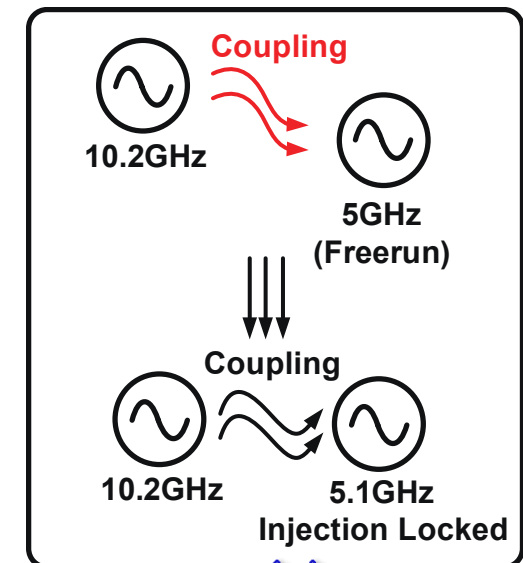
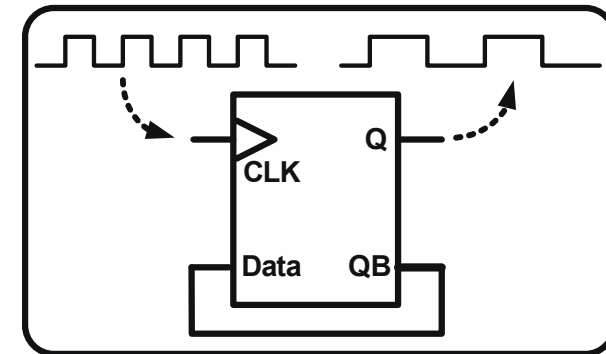


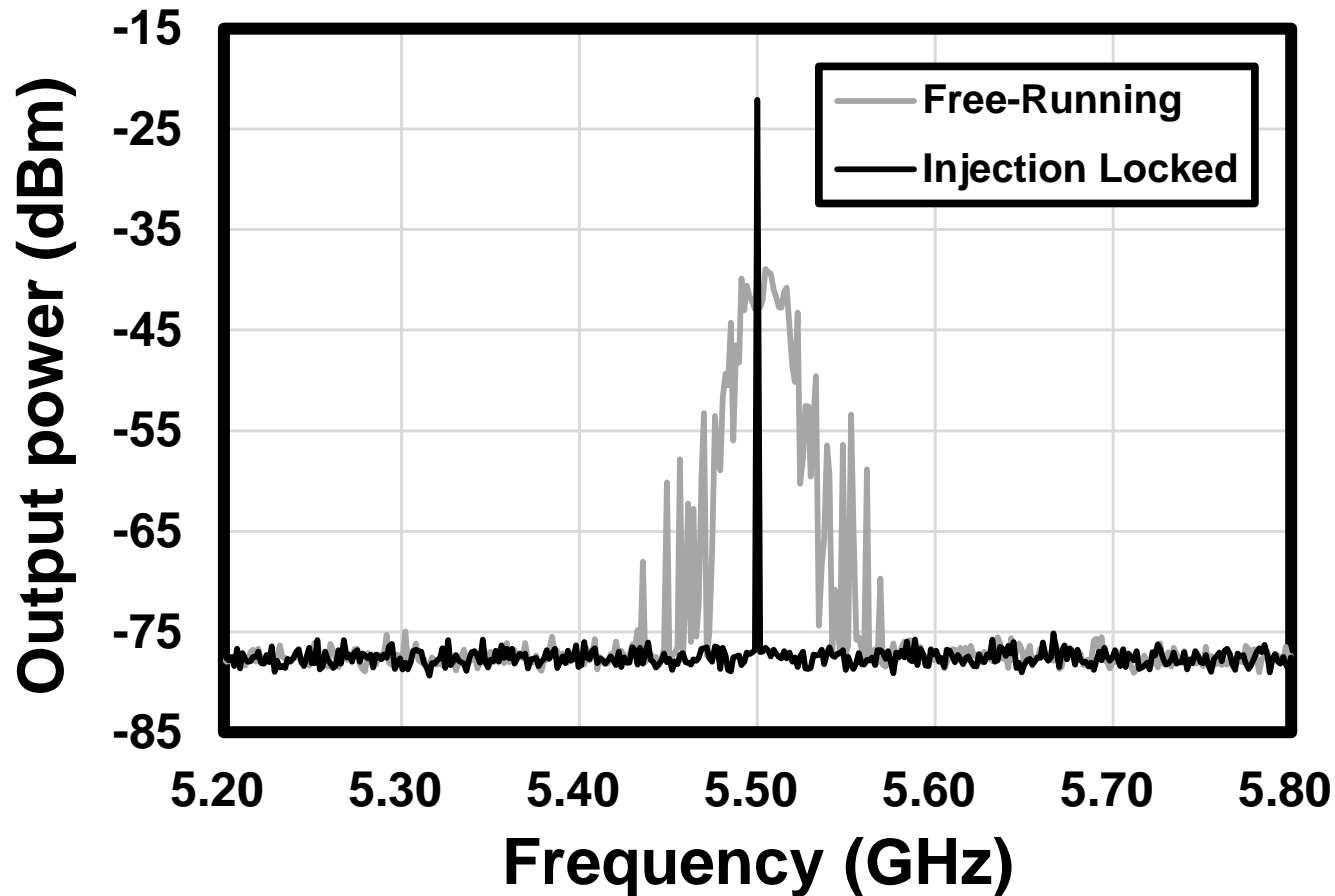
- An Dual-Step-Mixing ILFD using a **Even-Harmonic Direct Injection Technique** is proposed for an enhanced locking range of divide-by-6 and divide-by-4 operations
- It achieves the **widest locking range reported for divide-by-6 operation** and comparable performance with the state-of-the-art divide-by-4 ILFDs
- This work is suitable to be integrated in push-push or sub-harmonic injection-locked 60GHz PLLs

Thank you for your interest

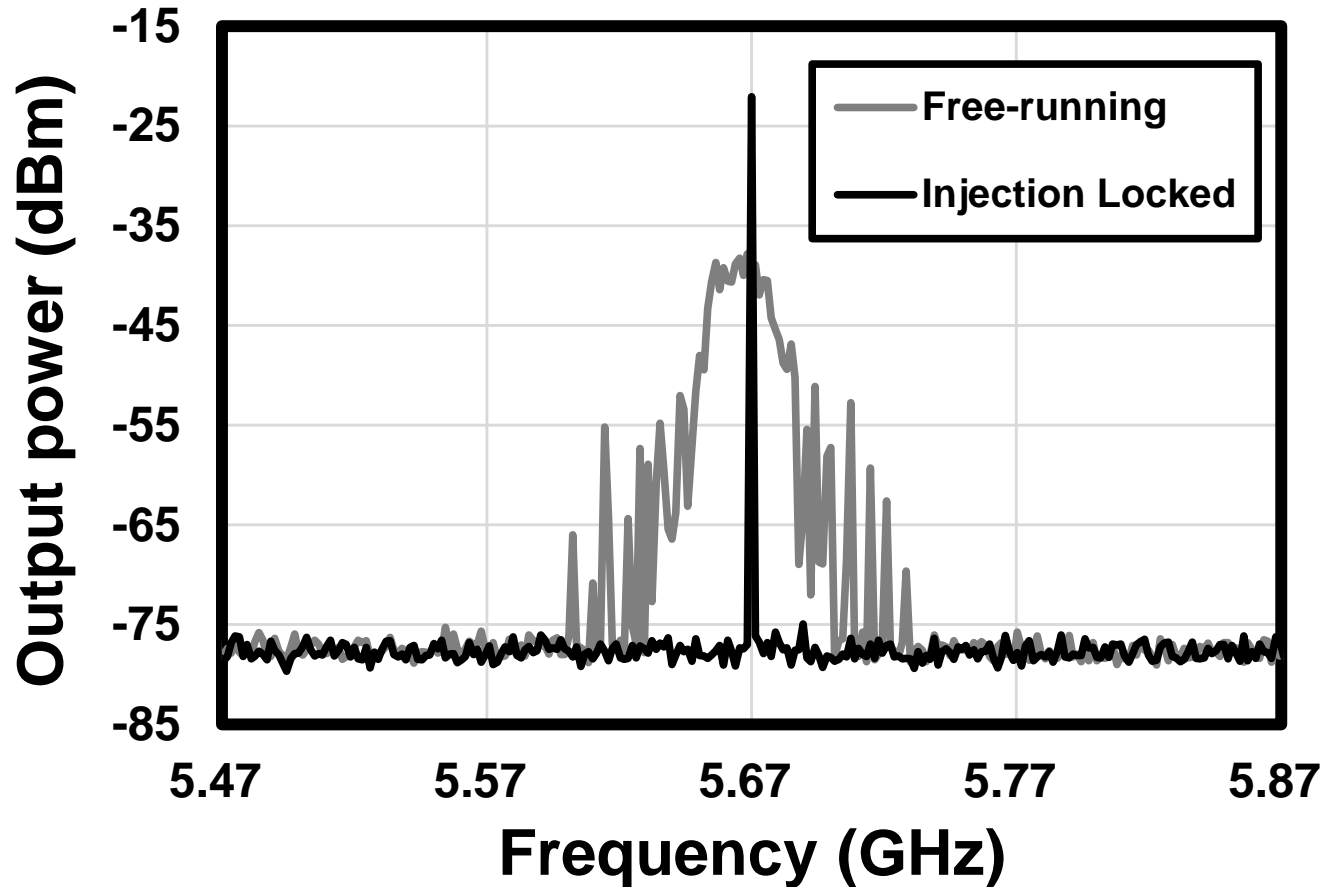
This work was partially supported by MIC, SCOPE, MEXT, STARC, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

- High speed frequency dividers and VCO are the most power hungry parts of modern high frequency PLLs.
- Static Frequency Dividers:
 - Wide locking range
 - Consume considerable power
 - Conventionally only divides by 2
- Injection Locked Frequency Dividers (ILFDs)
 - Limited locking range
 - Low power consumption
 - Can divide by higher than 2

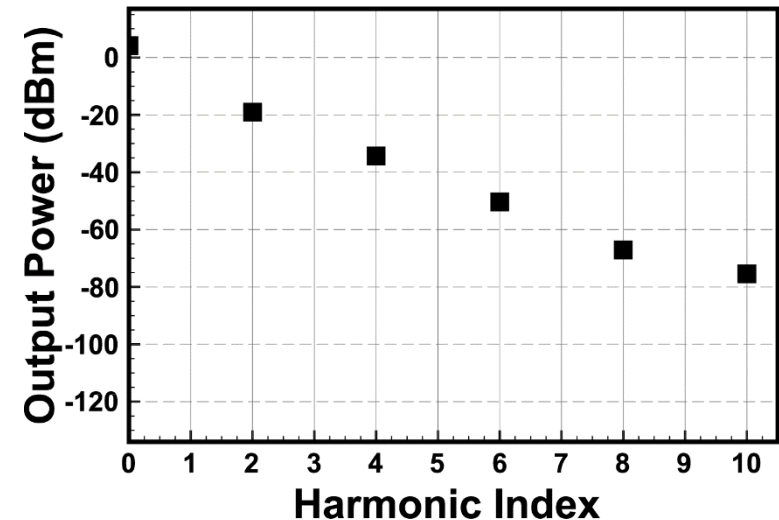
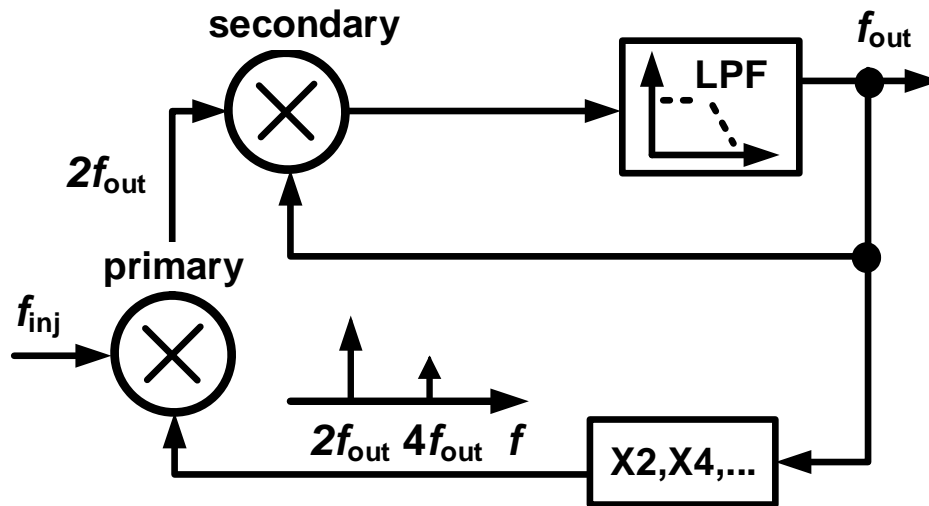




- Injection frequency of 22GHz is applied



- Injection frequency of 34GHz is applied



- Dual-step mixing mechanism for divide-by-4 and divide-by-6 operation