A 0.4ps/bit Digitally-controlled Varactor for a Fully Synthesizable DCO

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1. Introduction

Recently, all-digital PLLs synthesized from standard cells have shown the advantages compared with traditional analog PLL in terms of portability and scalability [1, 2]. A DCO with high resolution is inevitably required in synthesizable PLLs. Conventionally, tri-state and NAND gates are used to change the DCO resolution but the result is not good [1]. This paper proposes a 0.4ps/bit digitally-controlled varactor for a fully synthesizable DCO using Miller effect to achieve a finer capacitance.

2. Circuit Design and Simulation

As depicted in Fig.1, medium resolution is achieved by NAND gate with one port (D_M) as control bit and the other port connecting to DCO ring. From the simulation result, there is a capacitor peak when D_M is equal to 1 and input voltage is almost equal to 0.4V. Miller effect can be used to illustrate this peak. The NAND gate can be considered as analog amplifier when the input is around half of VDD. Thus its DC gain will affect the input capacitance by Miller effect. For the medium capacitor, the simulated time delay is 4.8ps when D_M varies from 0 to 1. To achieve a finer resolution, one INV is used to reduce the Miller effect. As shown in the simulation result, the capacitance difference is finer than medium one and the time delay difference is only 0.4ps.

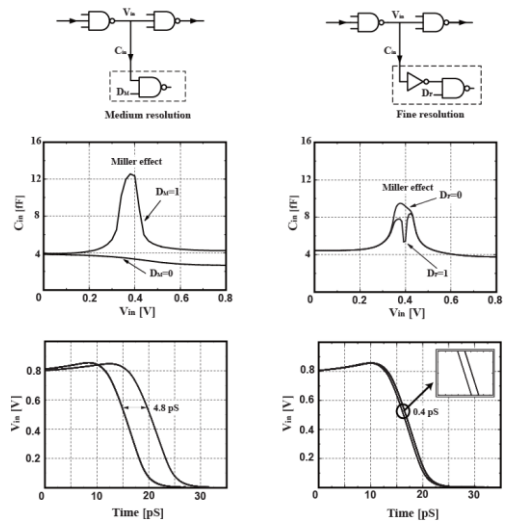

Figure 1: Medium resolution and proposed fine resolution capacitor realization and simulation.

3. Results Analysis

For system requirement, 3-input NAND gate is used to construct a ring oscillator. As shown in Fig.2, a rising edge is used as the input of 3-input NAND gate and the simulation results are shown in the right side for fine capacitor. The falling time is different for fine capacitor case when D_F=0 and D_F=1. For D_F=0, the falling edge is from X node to Y node, which is cross connected with rising edge at node Y1(near VDD/2), where the PMOS and NMOS of NAND have the highest voltage gain as shown in D_F=0 case of Fig.3, therefore largest miller capacitor. For D_F=1 case, when input is VDD/2, the output voltage is at Y2 and the PMOS works in triode region, so the voltage gain is smaller than D_F=0 state, and the gain result is shown in D_F=1 case of Fig.3. Using this capacitor, the PLL could realize a resolution nearly 0.4ps/bit.

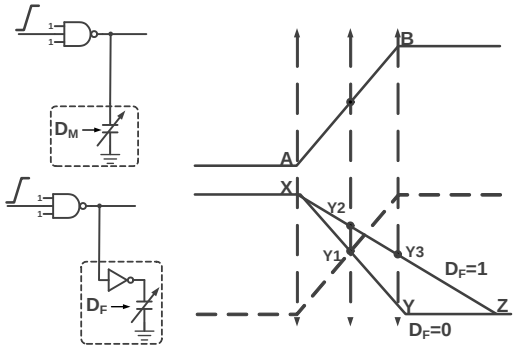

Figure 2: Transient response with proposed fine digitally-controlled capacitor loading

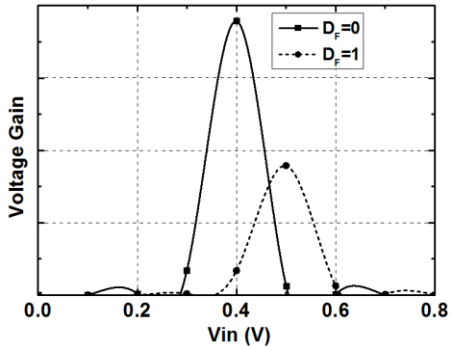

Figure 3: Voltage gain with proposed fine digitally-controlled capacitor loading

4. Conclusion

This paper proposes a digitally-controlled capacitor for a synthesizable DCO using standard cell. Through simulation, the proposed capacitor can be suitable for realizing the high frequency resolution DCO.

Acknowledgements

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References

[1] Y. Park and D.D. Wentzloff, "An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS," IEEE Custom Integrated Circuits Conf., pp. 1-4, Sep. 2011.

[2] Wei Deng, Dongsheng Yang, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, and Akira Matsuzawa, "A 0.0066-mm^2 780-uW Fully Synthesizable PLL with a Current Output DAC and an Interpolative-Phase Coupled Oscillator using Edge Injection Technique,"*ISSCC Dig. Tech. Papers* , 2014.