A Digitally Synthesized PLL with a DAC and Phase-Coupled Oscillator using Standard Cells Only

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1. Introduction

Phase-locked loops (PLLs) are widely used for clock generation in modern digital systems. This paper proposes a fully synthesizable PLL [1] using standard digital library only, with a current output digital-to-analog converter (DAC) for maintaining frequency linearity and duty balance, an interpolative phase-coupled oscillator for minimizing output phase imbalance from automatic P&R.

2. Circuit Design and Implementation

Block diagram of the proposed PLL with a DAC and an interpolative phase-coupled oscillator is given in Figure 1. All circuits that makeup the PLL, including the DAC and DCO, are implemented using digital standard cells in the automated design procedure. A dual-loop PLL architecture is employed and improved in this design to provide continuous tracking of voltage temperature variations and avoid timing problems in the conventional injection-locked PLLs.

In order to relieve the oscillator output phase imbalance caused by the automatic P&R, an interpolative phase-coupled oscillator built by three 3-stage oscillators is developed based on the concept. Due to its internal feedback and feedforward control using phase interpolators for the oscillator, the phase difference within the ring and between all adjacent rings will remain fixed with time, leading to balanced output phases. To maintain the control code resolution and extend the operating frequency range, the oscillator is designed to operate with a coarse, a medium, and a fine tuning. An analog equivalent DAC built from standard CMOS NAND gates is proposed as the coarse tuning circuitry and contributes to reduce the overall power consumption and occupied chip area without sacrificing phase balance. Tri-state buffers are not used since they are sometimes not provided in standard cell libraries. The proposed DAC consists of a PMOS-current source array and an NMOS current mirror. The PMOS-current-source array is built by connecting outputs of 4 NAND gates together with one of each NAND gate inputs driven by a digital control bus. The NMOS current mirror is built by connecting one input of NAND gate to its output and the other input connects to logic HIGH.

3. Measurement results

The proposed fully synthesizable PLL is fabricated in a 65nm digital CMOS process. The PLL occupies only 110 µm × 60 µm layout area as shown in Figure 2. The phase noise is evaluated by using a signal source analyzer (Agilent E5052B) and the spectrum is measured by using a spectrum analyzer (Agilent E4407B). The measured frequency tuning range of the PLL is 0.39 to 1.41 GHz. At a 0.9 GHz output, the power consumption is 780 µW excluding output buffers from a 0.8 V power supply. Figure 3 shows the measured phase noise and output spectrum at 0.9 GHz output using a 150 MHz reference clock. The phase noise maps to a 1.7 ps jitter when integrated from 10 kHz to 40MHz.

4. Conclusion

To conclude, a fully synthesized PLL with a current output DAC and an interpolative phase-coupled oscillator based on standard digital library without any modification, which was designed using digital design flows without using any manual placements, is presented in this paper.

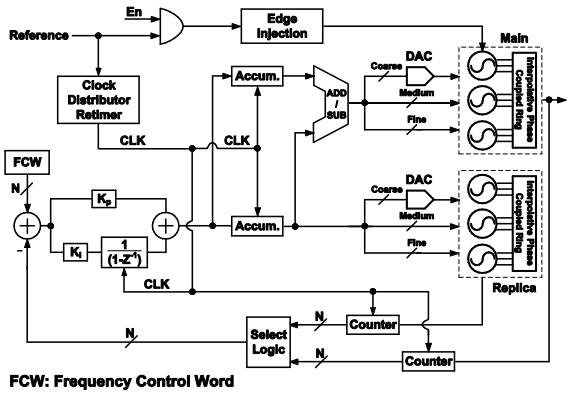

Figure 1: Block diagram of the proposed fully synthesizable PLL with a DAC and a phase-coupled oscillator.

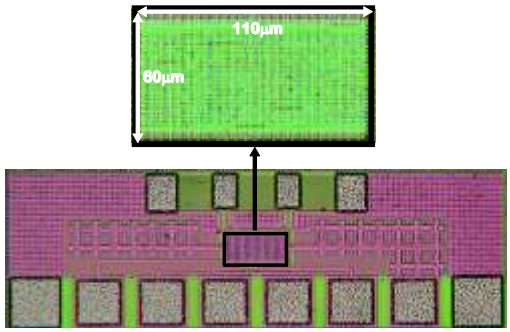

Figure 2: Chip microphotograph.

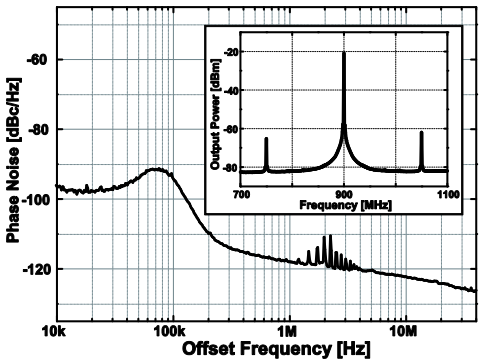

Figure 3: Measured phase noise at a carrier of 0.9 GHz.

Acknowledgements

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References

[1] Wei Deng, Dongsheng Yang, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, and Akira Matsuzawa,, "A 0.0066mm^2 780µW Fully Synthesizable PLL with a Current Output DAC and an Interpolative-Phase Coupled Oscillator using Edge Injection Technique,"*ISSCC Dig. Tech. Papers* , 2014.