A Dual-Step-Mixing ILFD using a Direct Injection Technique for High-Order Division Ratios in 60GHz Applications

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Abstract A wide-locking-range and low-power injection-locked-frequency-divider (ILFD) using direct injection in dual-step mixing is proposed to widen locking range (LR) of divide by 4 and 6 operations. Two main advantages over the previously-reported progressive mixing ILFD are less headroom required and less sensitivity over large injection amplitude. This work achieves the widest LR reported of 4.3GHz for divide-by-6 and 5.7GHz for divide-by-4 operation while consuming 3.1mW without frequency tuning. The divide-by-4 and divide-by-6 operation of this ILFD can cover the required frequency range for 60GHz wireless standards.

Keyword wide-locking-range, low-power, Dual-Step Mixing, Direct Injection, ILFD

1. INTRODUCTION

Due to its smaller size, a ring-based ILFD is more preferable comparing to an LC-based counterpart. However, a technique to increase locking range of a high-divide-ratio ring-based ILFDs is necessary to avoid more power dissipated at higher oscillation speed in mm-wave applications. As shown in Fig.1 (a), and (b), a single-staged divide-by-4 or a divide-by-6 ILFD can directly down-convert mm-wave signals to low enough frequency where low-power digital dividers can operate. Combining a high-divide-ratio inductor-less ILFD in a 60GHz PLL based on push-push [1] or sub-harmonic injection [2] technique, this will significantly help reduce its total power consumption and area.

2. PROPOSED DUAL-STEP-MIXING ILFD

Conventional ILFD based on direct mixing suffers from narrow locking range which is not robust over PVT variations for higher division ratios, *i.e.*, 4 or 6. This is because for a division ratio of 6, the injected signal mixes with a weak fifth harmonic at the output nodes resulting in a narrow locking range.

By first utilizing stronger harmonics to mix with the injected signals in a progressive mixing operation, locking range of higher division ratios can be enhanced [3]. An additional cascoded tail transistor is required in order to allow progressive mixing operation as shown in Fig.2. Due to the PMOS loads, an intrinsic free-running frequency of an oscillator is varied by large injection amplitudes applied at the gate of cascoded tail transistors resulting in asymmetrical locking range in Fig.2.

In this work, a dual-step mixing which is suitable for mm-wave applications is utilized. Fig.3 shows the proposed ILFD which is composed of 4 resistor-loaded delay cells. Free running frequency of this ILFD can be tuned through current tuning which reduces the effect from large injection amplitude. An NMOS switch is placed across the common-nodes of the first and third delay cells acting as a primary mixer which inject the signal to the even-harmonic oscillator. This results in less voltage headroom required. For a divide-by-6 operation, the injected signal is first mixed with a strong fourth harmonic that is naturally exists in a common-node of delay cell resulting into a frequency near second harmonic. Then, it further mixes with the fundamental signal through a built-in single-balanced mixer into a frequency near fundamental which pull the free-running frequency of an ILFD and lock to the injected signal. For a divide-by-4 operation, injected signal first mixes with second harmonic at the primary mixer.

3. MEASUREMENT RESULTS

The proposed ILFD is fabricated in a 65nm CMOS process shown in Fig.4. It achieves the widest locking range of 4.5GHz (13%) and 6.6GHz (28%) for divide-by-6 and divide-by-4 operations while consuming 3.6 and 4.2mW, respectively. Both operations cover the required frequency range for 60GHz wireless standards as shown in Fig.5.

4. CONCLUSION

The proposed ILFD achieves the widest locking range reported for a divide-by-6 operation and competitively wide locking range for divide-by-4 operation. It is suitable to be integrated in push-push or sub-harmonic injection locked 60GHz PLL

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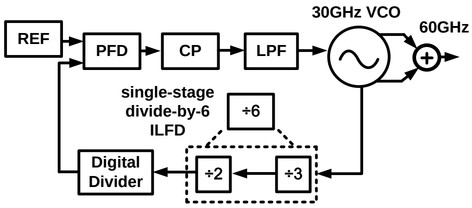
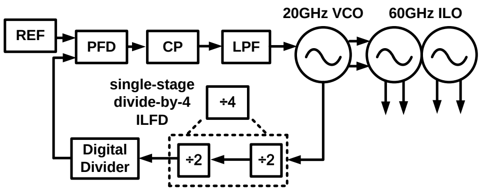


(a) 60GHz push-push VCO



(b) Sub-harmonic injection based on 20GHz PLL

Fig.1. 60GHz frequency synthesizers proposed in [1],[2]

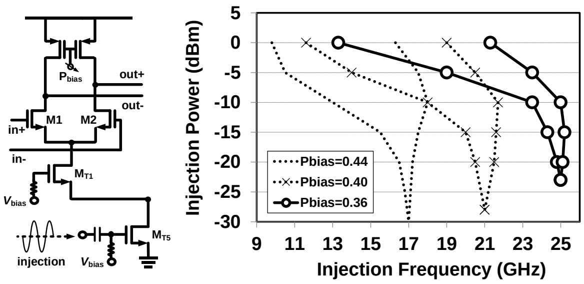
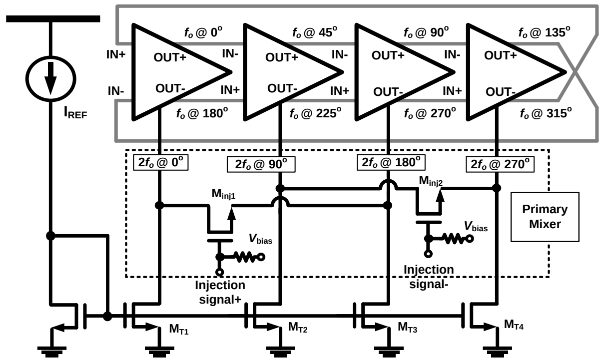


Fig.2 Asymmetrical locking range caused by large injection amplitude in an ILFD proposed in (2)

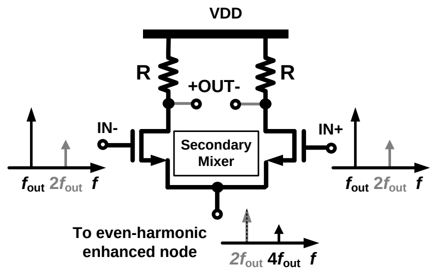
TABLE I PERFORMANCE COMPARISON WITH DIVIDE-BY-6 AND DIVIDE-BY-3 ILFDS

	Features	Div. Ratio	Locking Range* (GHz)	Locking Range* (%)	Power (mW)	FoM (%/mW)	Area (mm²)
[5]	Direct mixing	3	21.7-24.9	13.7	8.3	1.7	0.140
[6]	Direct mixing	6	141.0-144.3	2.7	14.0	0.2	1.160
[7]	Direct mixing	6	10.2-11.3	11.0	6.8	1.6	0.007
This	Dual-Step Direct Injection	6	28.5-32.8	13.4	3.6	3.7	0.002

*without tuning mechanisms, FoM = (% Lock Range)/(mW Power)



(a)



(b)

Fig.3. Detailed circuit schematic of the proposed (a) dual-step-mixing ILFD and (b) its delay cell

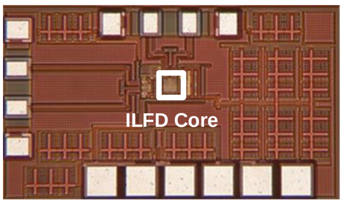
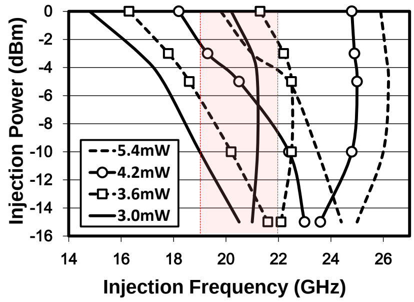
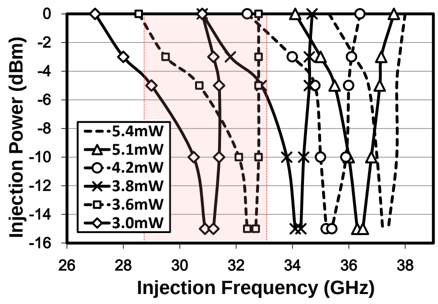


Fig.4. Chip Micrograph of the proposed ILFD



(a) Divide-by-4 operation



(b) Divide-by-6 operation

Fig.5. Measured locking range of the proposed ILFD