Novel Design Method for ~GHz DAC & Automated Design Program

~GHz DAコンバータの新設計手法と自動設計

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発表概要

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- これまで新たなDACの設計方法と、自動設計のｱｲﾃﾞｨｱを発表してきました
  - レイアウト・ドリブン　(レイアウト最優先設計)
  - サブ・ミクロン・スライス構造 (MOM容量、R)
  - 自動設計ﾌﾟﾛﾄﾀｲﾌﾟ・ﾌﾟﾛｸﾞﾗﾑ (R-DAC)
- 今回は、
  - MIM容量へ適用し、このﾀｲﾌﾟでもサブミクロン・スライスを実現できることを報告
  - この設計ﾅﾚｯｼﾞを、いかに自動設計へ応用したかの報告

Abstract

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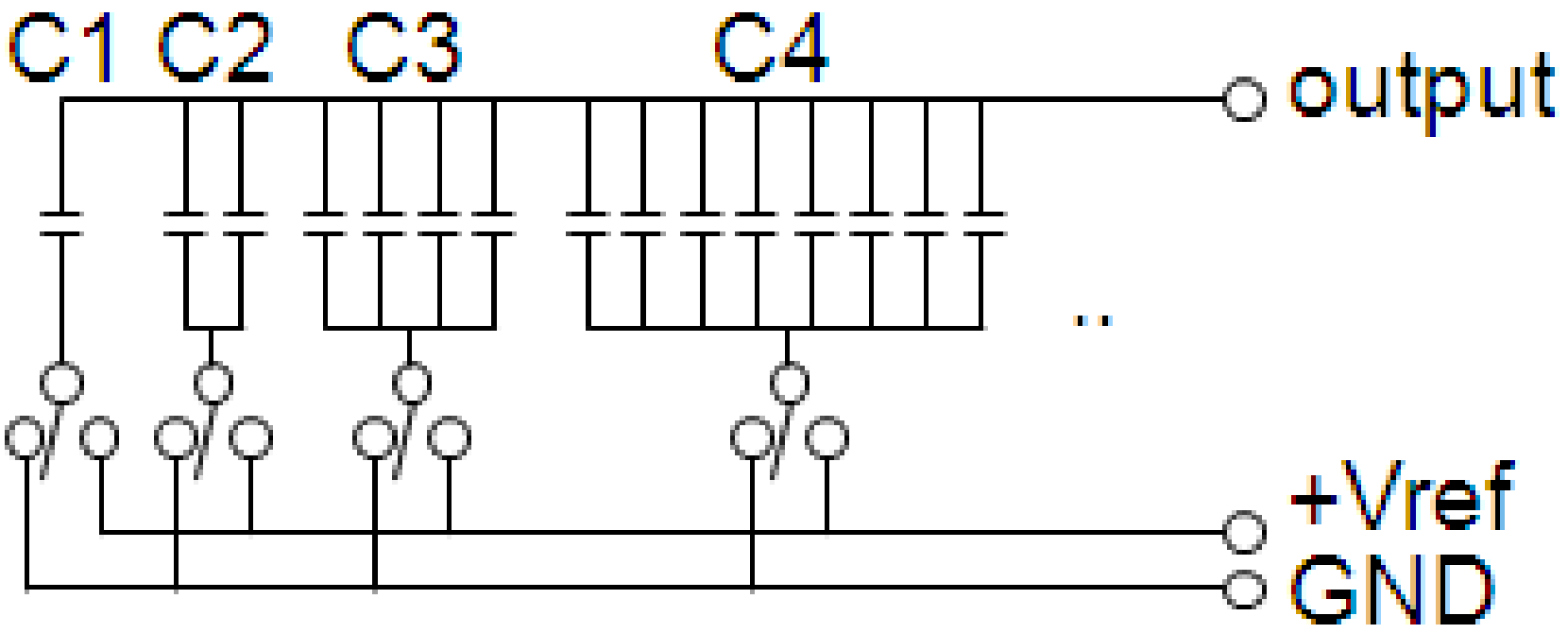
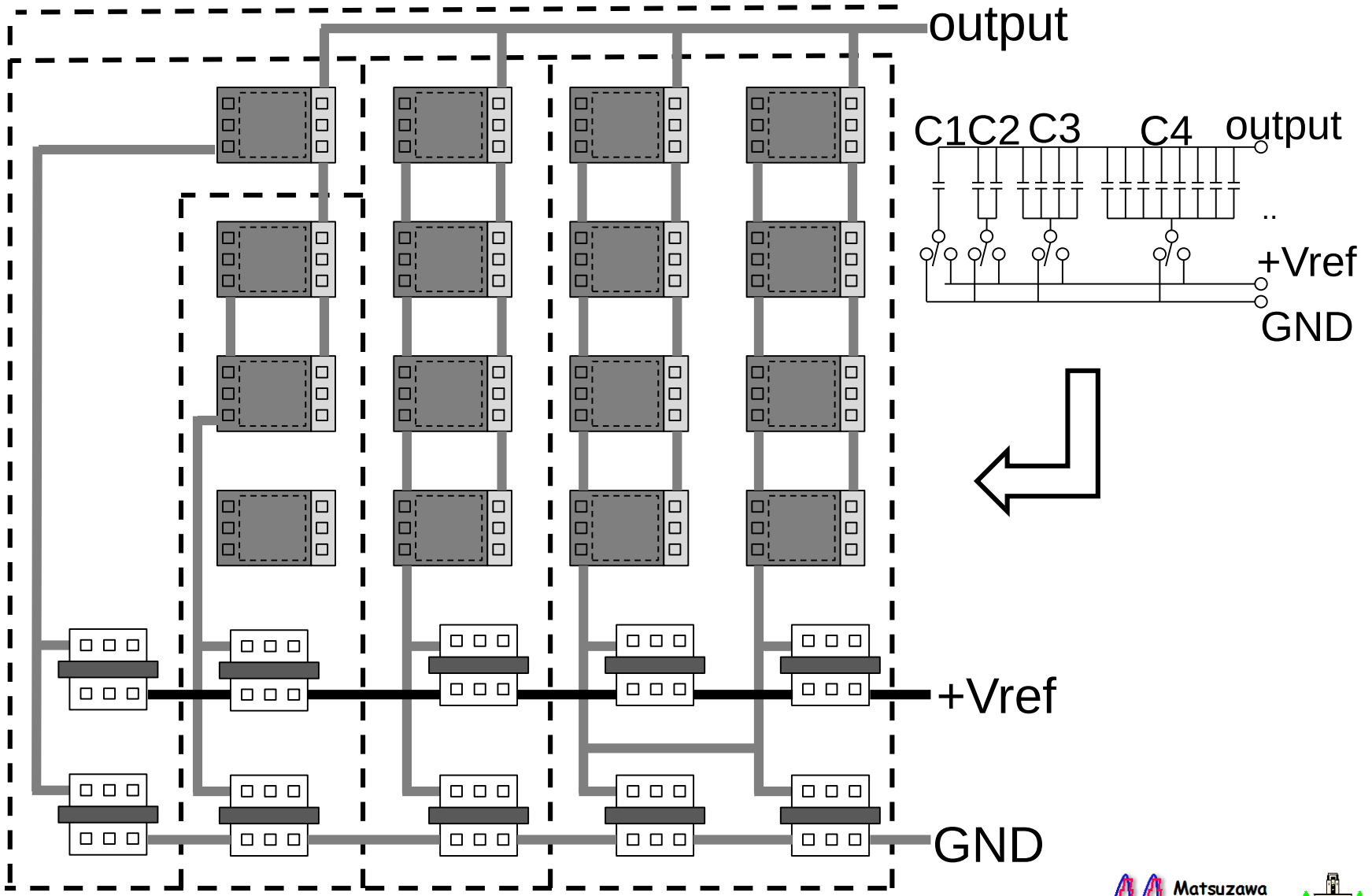
- **We are developing an automated design tool for ~GHz DACs.**
- **We apply proposed "layout-driven design methodology" into MIM capacitor type DAC. Finally we reached "sub-micron-wide slice structure"**
  - We give 1st priority to layout.
- **I explain slice-based DAC design knowledge-base, and outline of our prototype automated DAC design program**

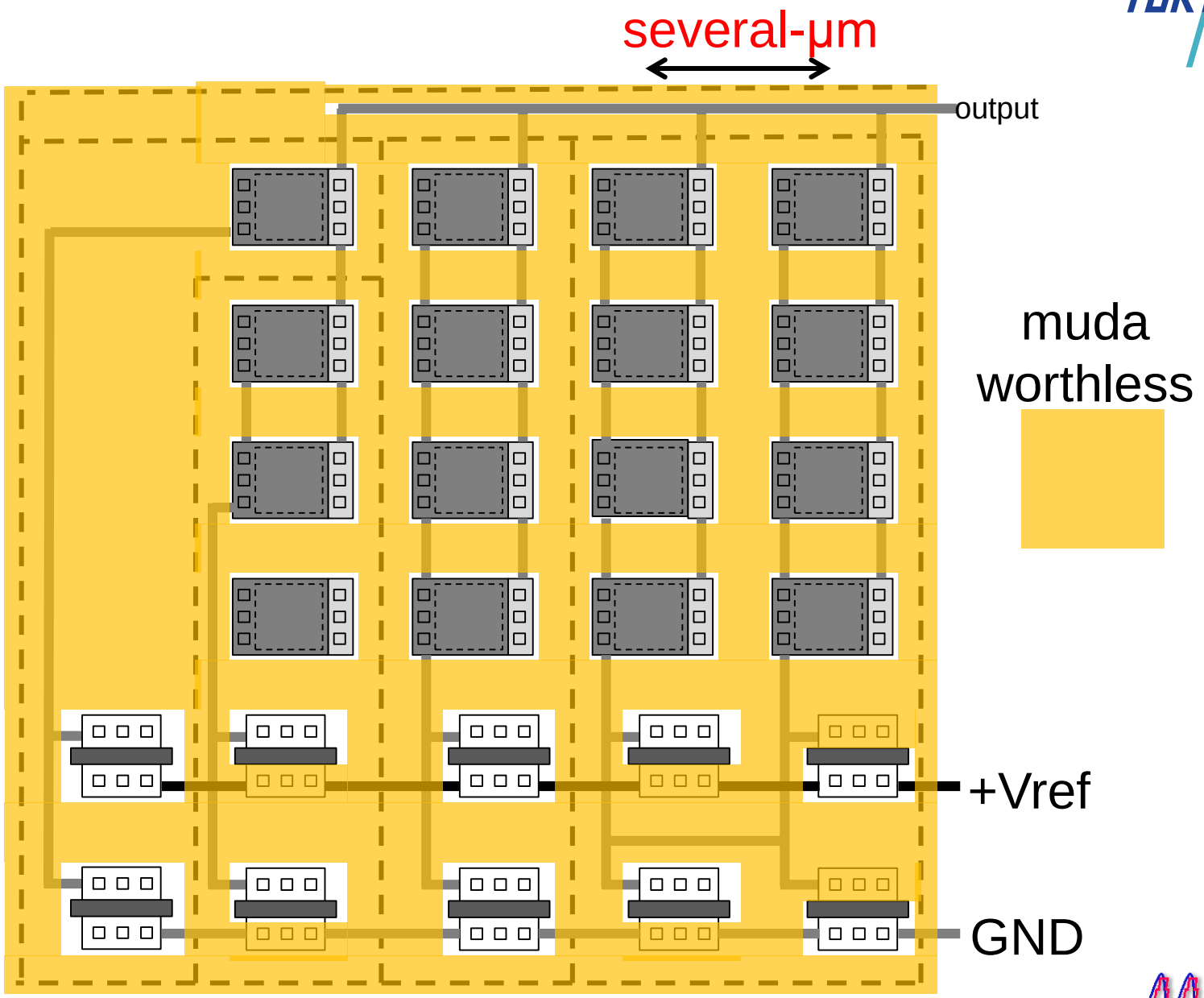
DAC design schematic example



Previous DAC design example



Worthless (muda) area in Previous



How to cut "muda" by layout-drive design method

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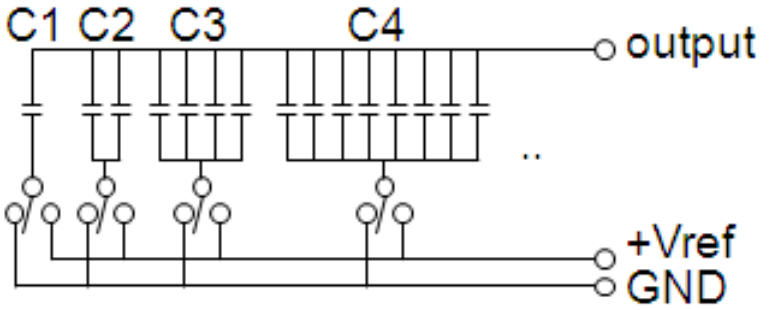
- **No isolations**
  - Because one of nodes of capacitors is commonly connected with output node

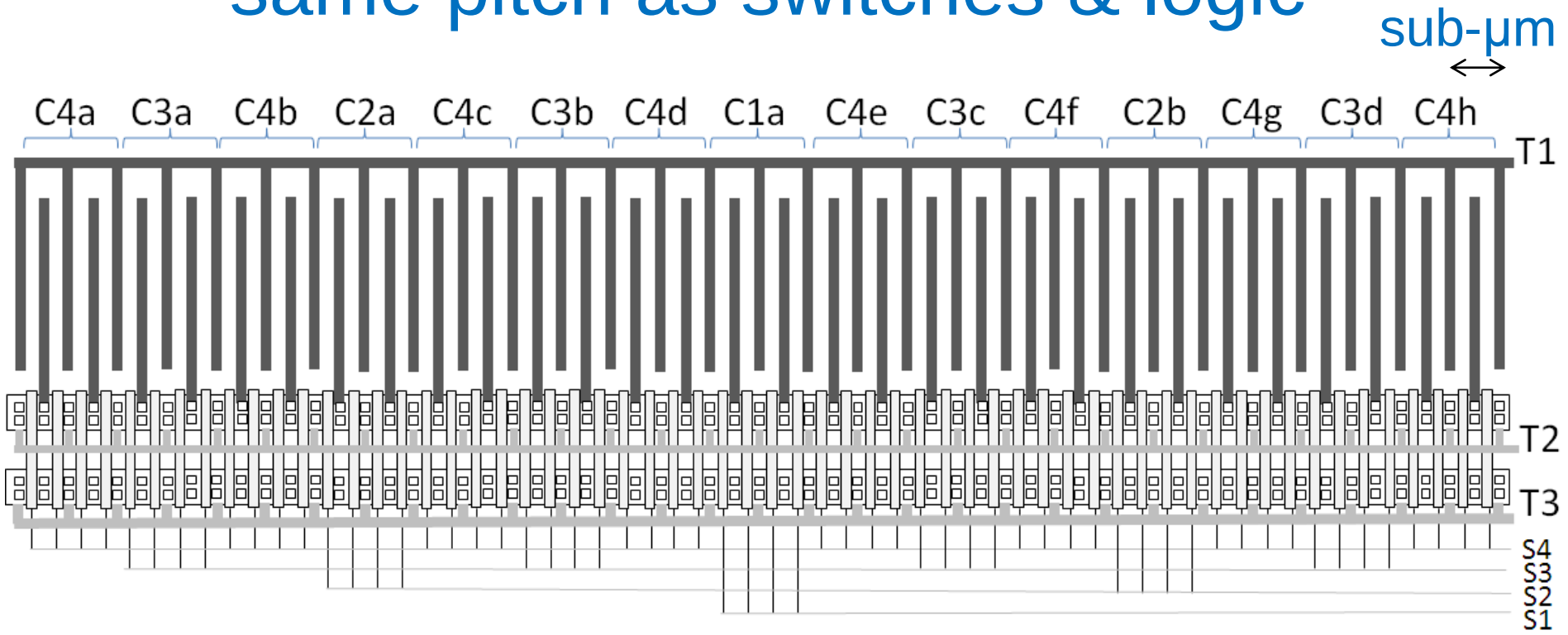


- **No shields**
  - Other nodes of capacitors are connected to either +Vref or GND through switches
- **No wiring areas rather than above the elements**
  - We propose unit capacitor width is adjusted same pitch as switches & logic
- **Common sources**

Our proposed sub-μm slice structure

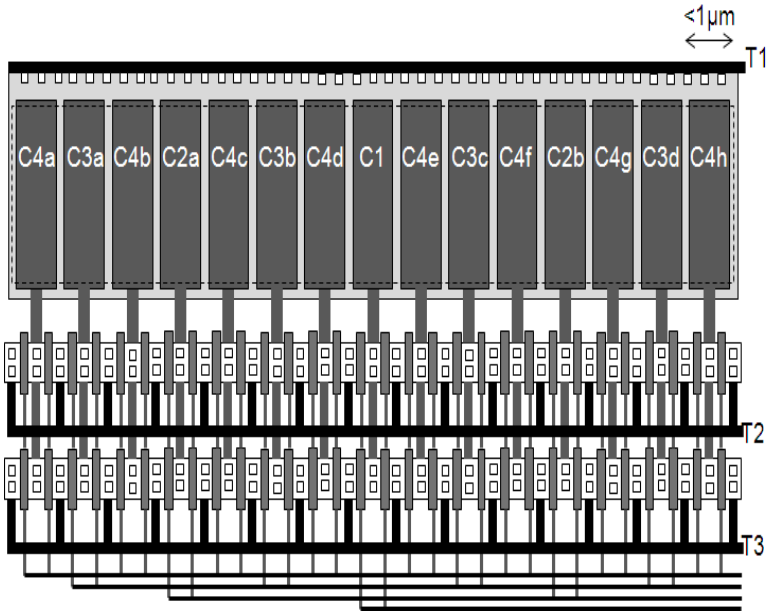
Reference

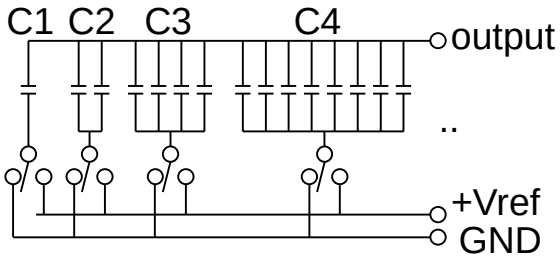
unit capacitor width is
same pitch as switches & logic



M.Sugawara, K.Mori, S.Lee, M.Miyahara, A.Matsuzawa, “Proposal of layout-driven 1/2.8 size DAC design methodology”, Silicon Analog RF study committee by IEICEJ, Nov.2013

Proposed MIM type C-DAC layout





Less than half size of previous

Proposed MIM type C-DAC layout

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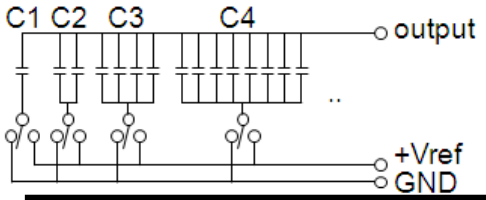
Zoomed



sub-μm

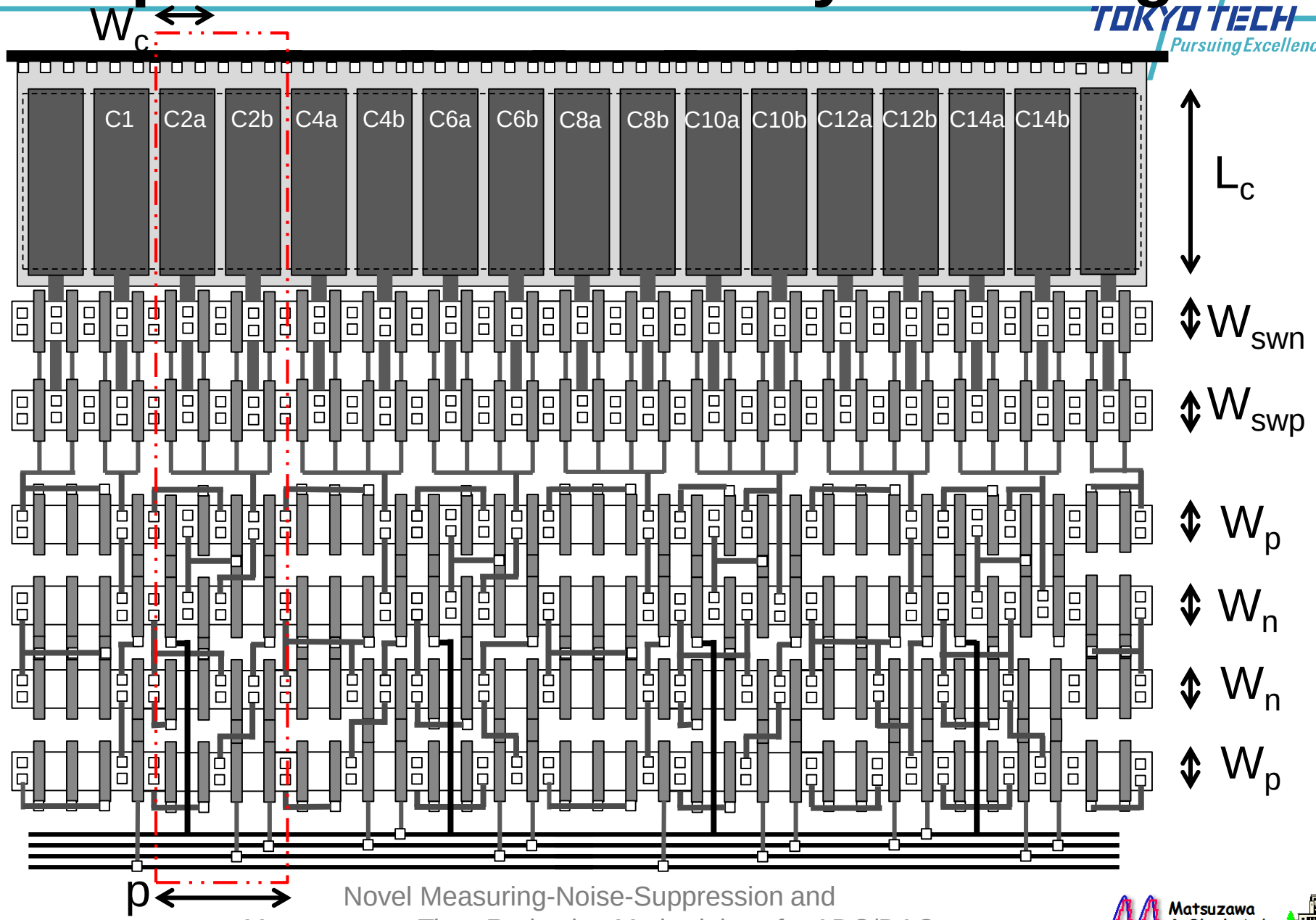
output

C4a C3a C4b C2a C4c C3b C4d C1 C4e C3c C4f C2b C4g C3d C4h

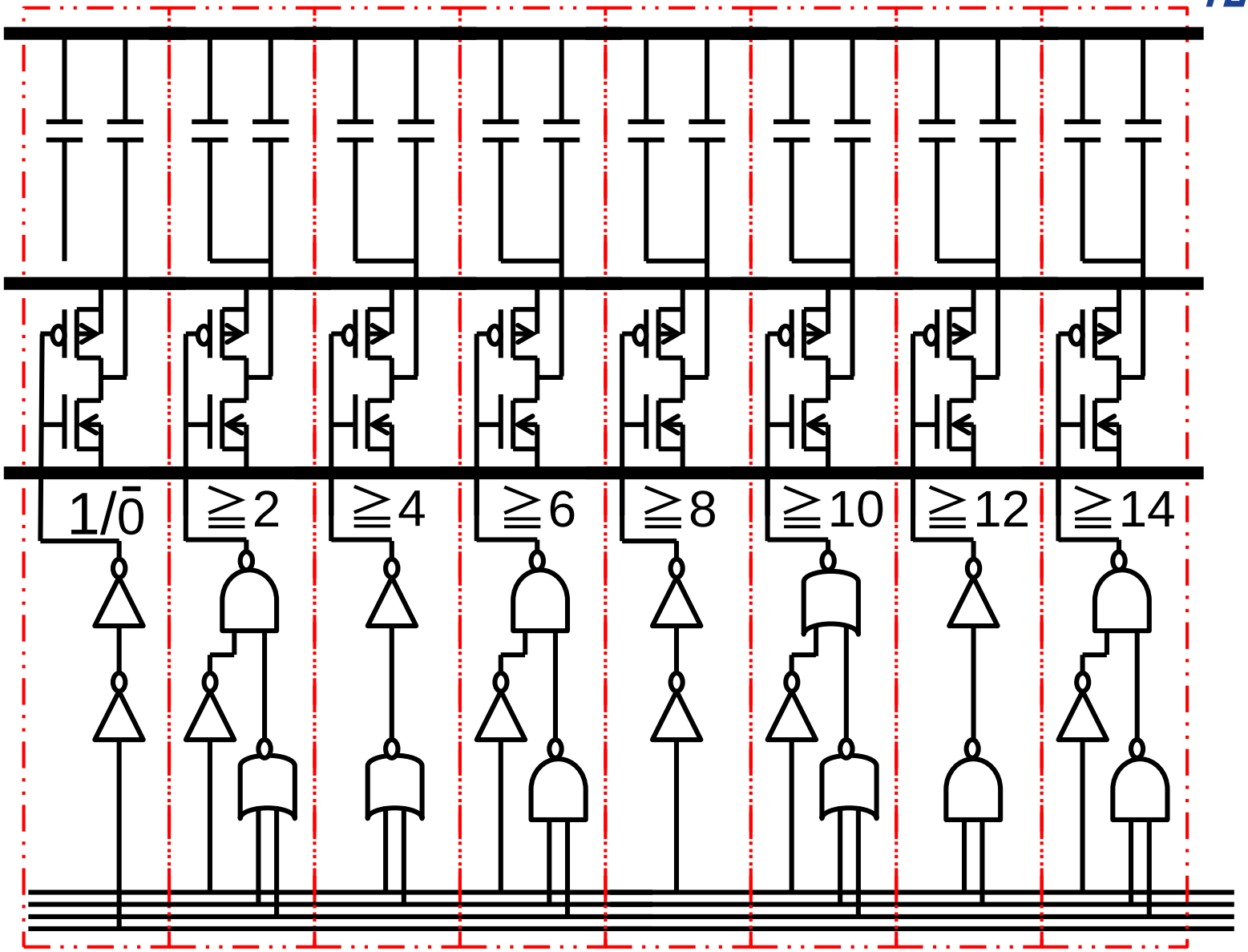
+Vref

GND

Proposed MIM C-DAC layout w/ logic



Proposed MIM-DAC schema w/ logic



Pros

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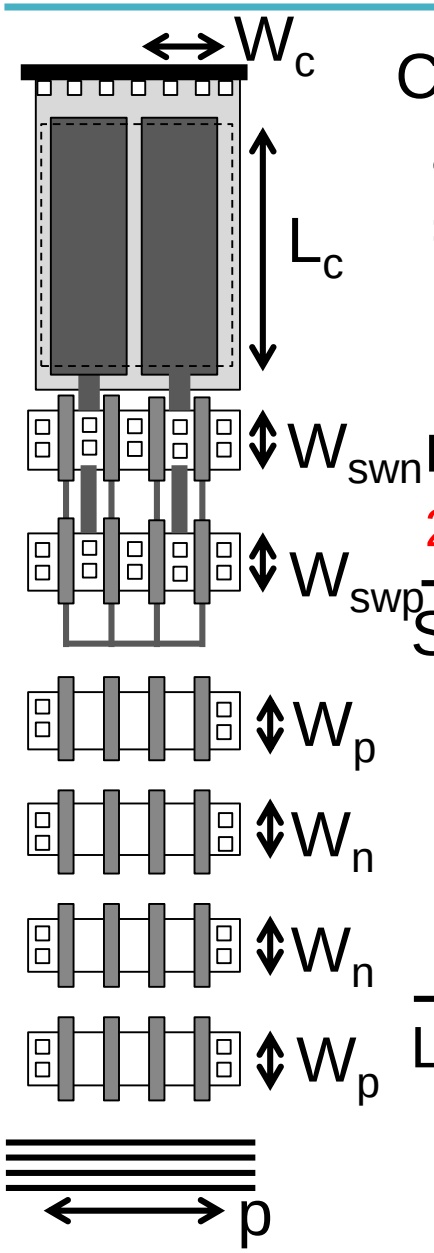
- **Smaller size than previous (<1/2)**
- **Higher speed & lower power consumption**
  - Because wires are straight and sub-μm
  - Stray capacitance and stray resistance are significant lower (<1fF) than previous
- **Easy for thermometer coding logic**
  - In-line with each switch and MIM capacitor
  - Small overhead in addition to binary code
  - Against process variation, less glitch
- **No more extra digital wire bundle areas**

Element size calculation



Capacitor :

allowable error = $m / 2^{b-n}$

=process variation = k_σ *pelgrom_coef / sqrt(L_c*W_c)

unit capacitor $C = \varepsilon * \varepsilon_0 * L_c * W_c / d$

Bigger value of Lc*Wc is survive.

Here, m = 1/4, k_σ = 4 @ default

2(Wc + metal_space) = pitch p.

Switch transistors :

allowable impedance = $(m_{sw} / 2^{b-n}) * (1/2\pi fC)$

= switch on-resistance = $\beta n *(V_{DD}-V_T)* W_{swn} / L_{swn}$

Here, L_{swn} is process minimum length @analog use.

p = (Lswn + drain_source_width) * 4

Logic transistors :

L_n is process minimum.

$W_n = (W_{swn} * 4) / fan\_outs$

Automated design tool development

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- **Proposed "sub-micron slice structure"**
  - is better performance than previous.
  - is easy to layout.
- **Why not to develop automated layout tool ?**

Automated tool IO

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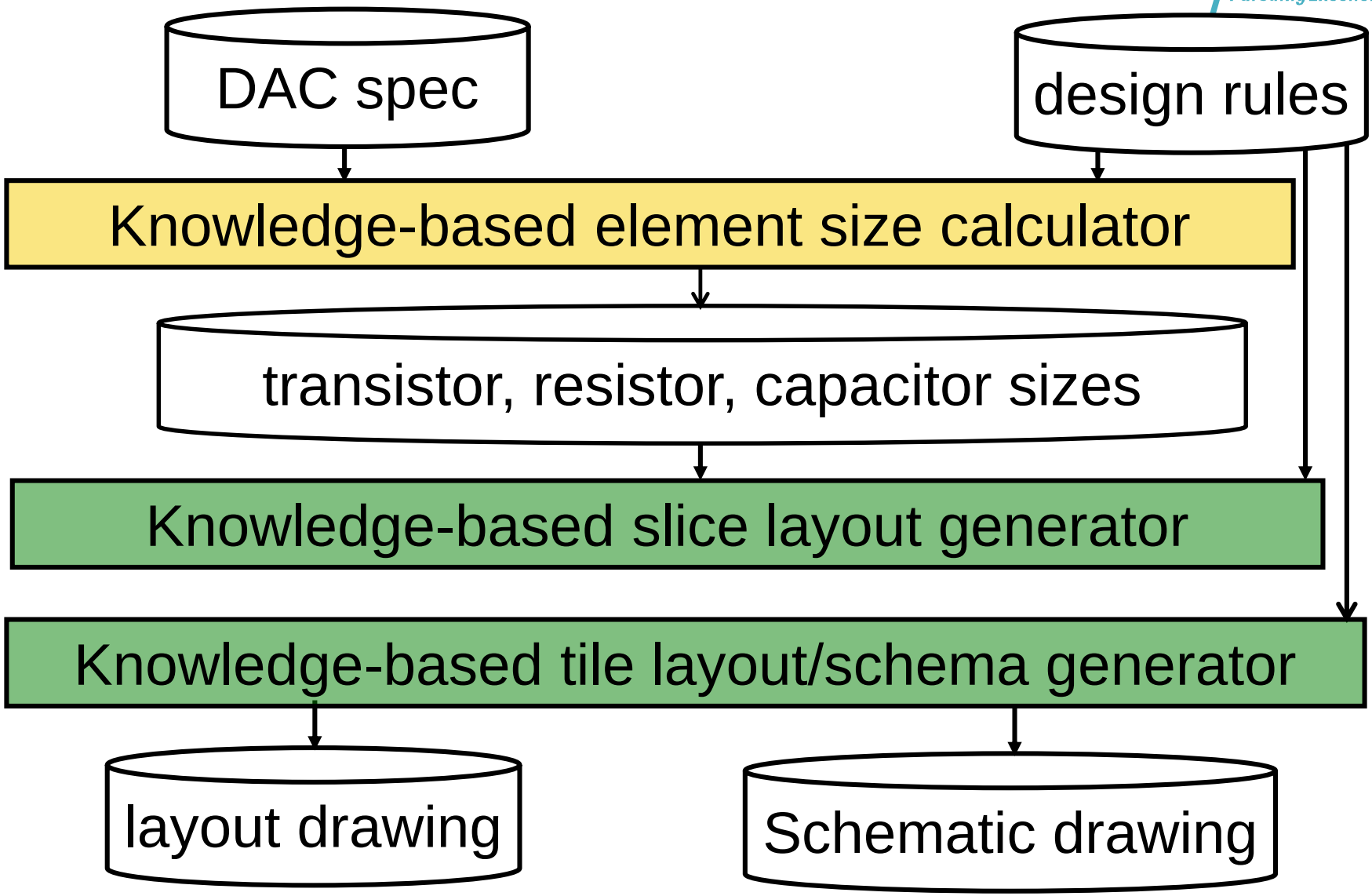
- **Inputs :**
  - Given DAC bit size
  - Either C or R, and given unit value or output value
  - Conversion speed
  - Design rule table from each process technology kit
  - Process portability, and at least X axis scalable.
  - Evaluation function (area, etc.) to determine final n value
  - Best match n or all n cases can be designed.
  - Additional switch option for ADC bottom plate injection
  - Full automation or semi automation
- **Outputs :**
  - Layout
  - Schematics for LVS or manual modification
  - DRC, LVS, LPE results if required (basically clean by design)

Proposed automated DAC design flow



Experimental results 1

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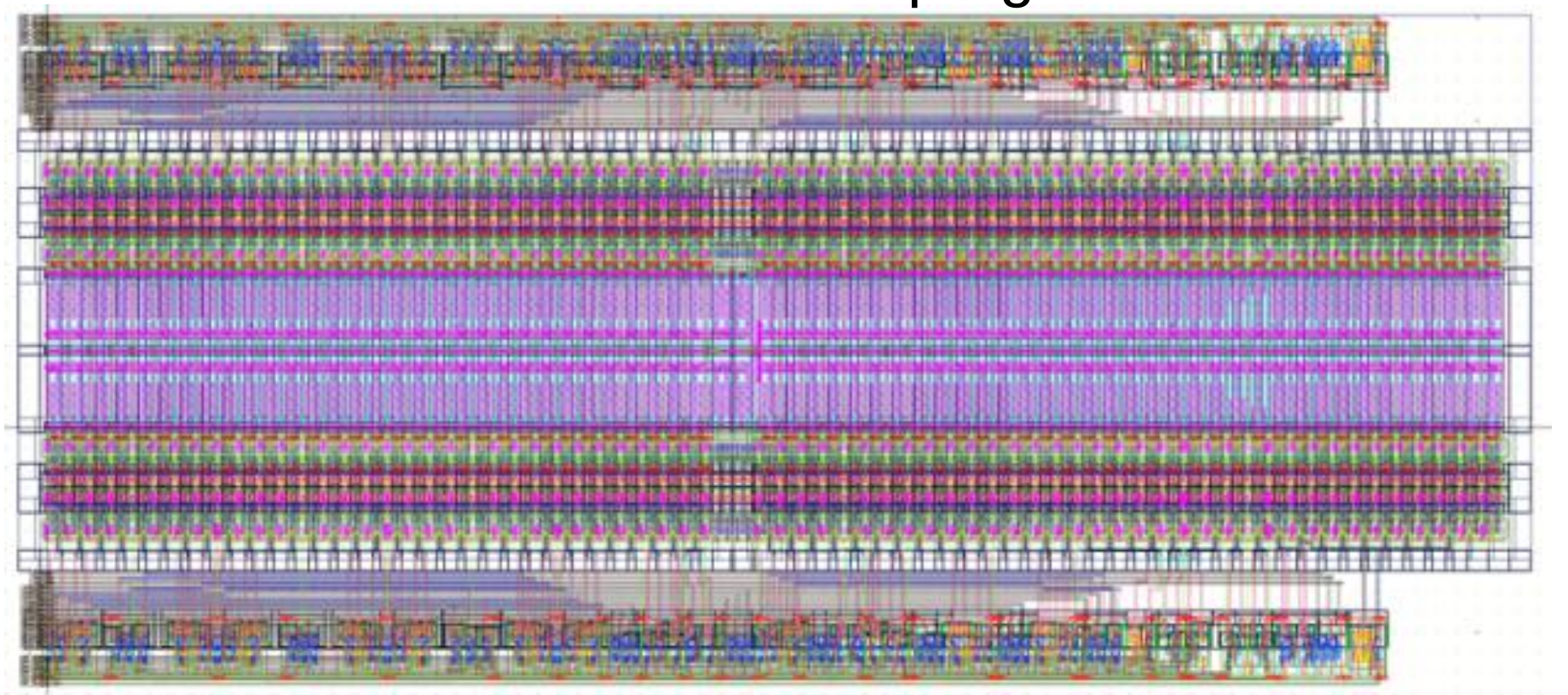
Manual layout result of
1Gsps 9bit C-DAC in 33μm × 72μm on 65μm CMOS
by using proposed sub-μm slice structure
before automated program



Experimental results 2

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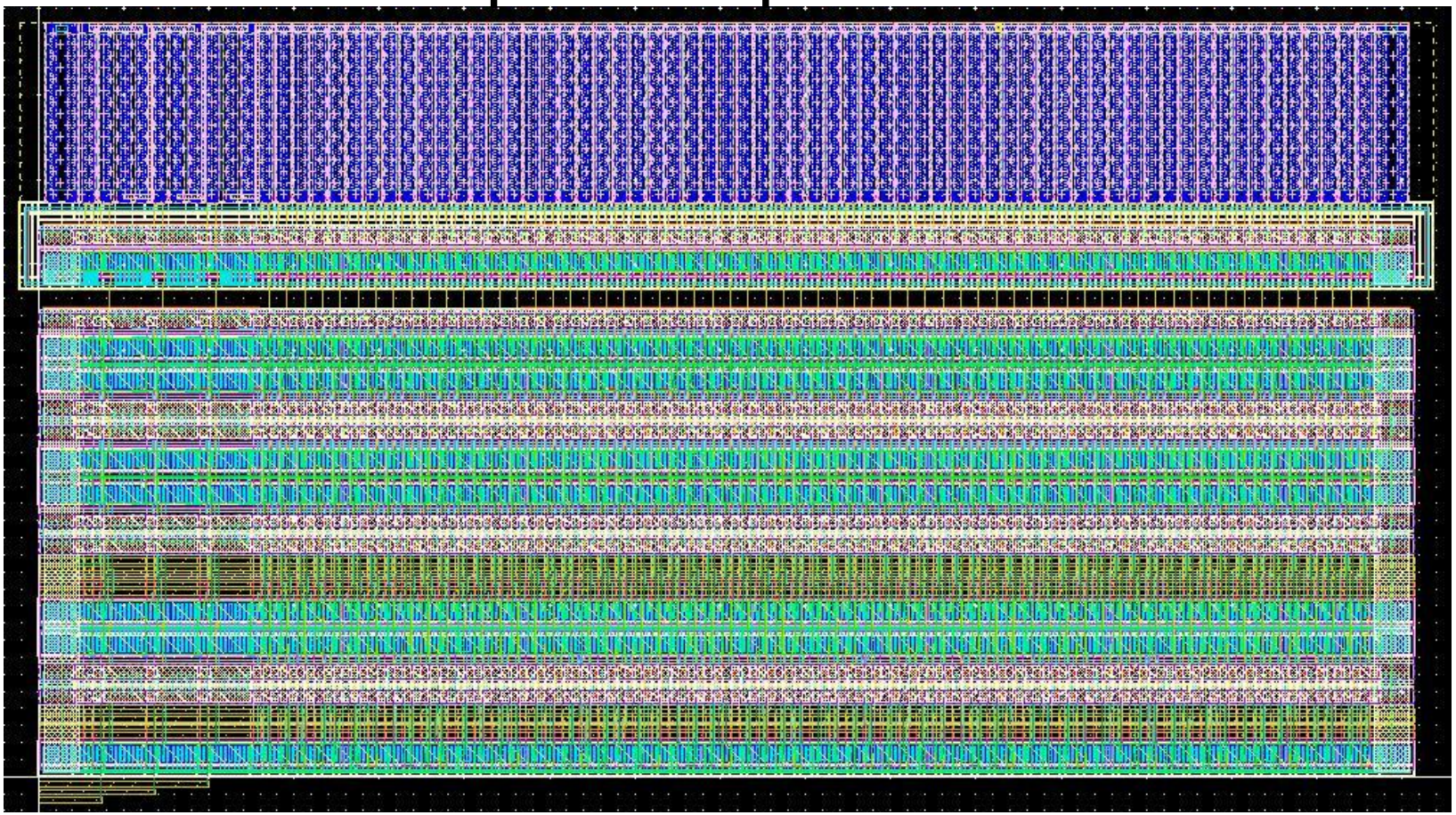
Automated design result of
9bit R-DAC with revised prototype program
0.04mm^2 = 46μm x 83μm in 65nm CMOS



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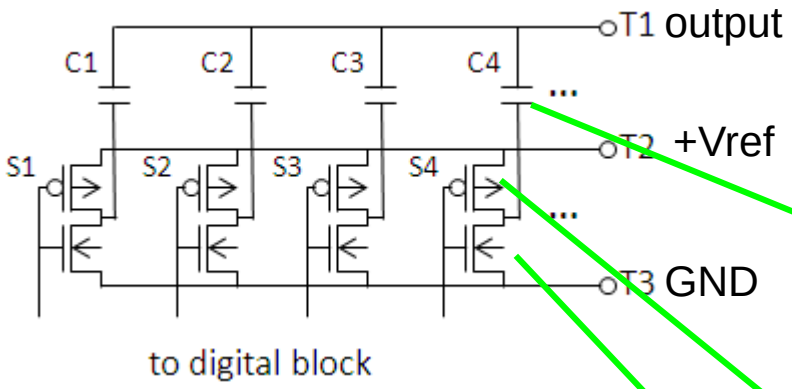
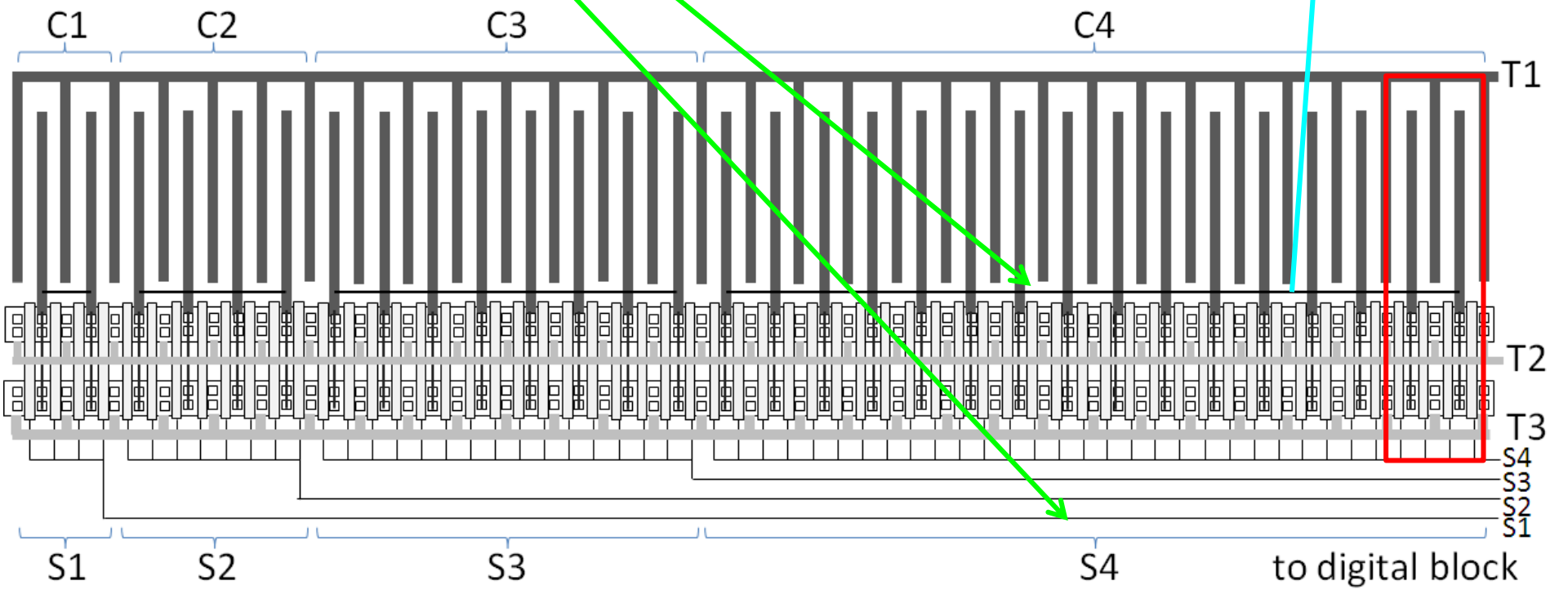
BACKUP SLIDES

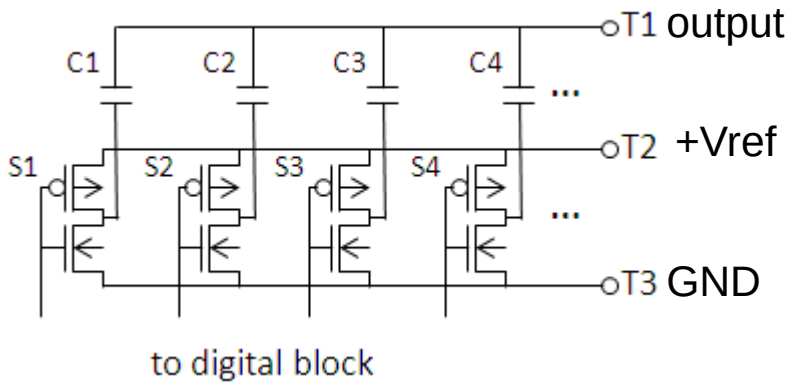
Proposed method: binary coded C-DAC



We can cut short bars due to same voltages



Proposed method: scrambled binary



Cancel gradient of capacitances, such as metal thickness.

Better INL, DNL

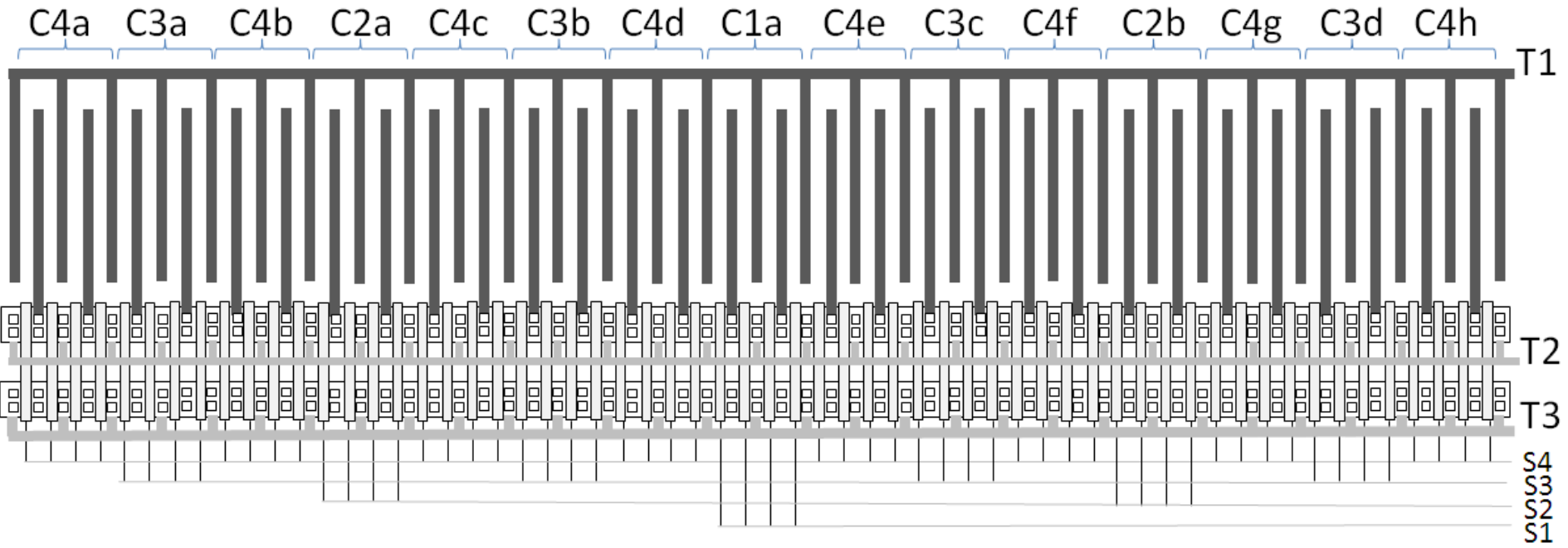
C1=C1a

C2=C2a+C2b

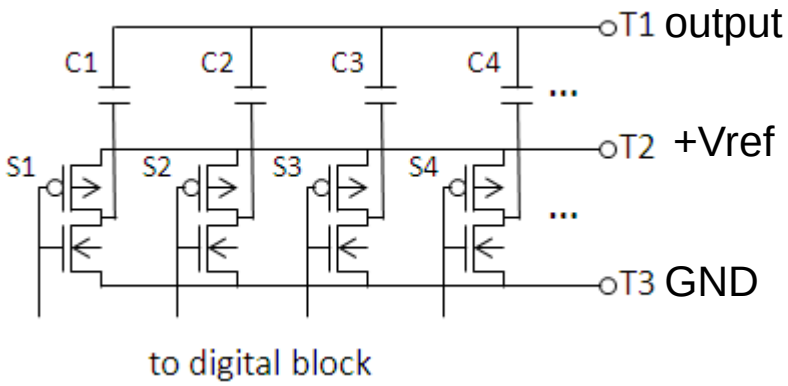
C3=C3a+C3b+C3c+C3d

C4=C4a+C4b+C4c+C4d+C4e+C4f+C4g+C4h

Controlled by switch logic connections.

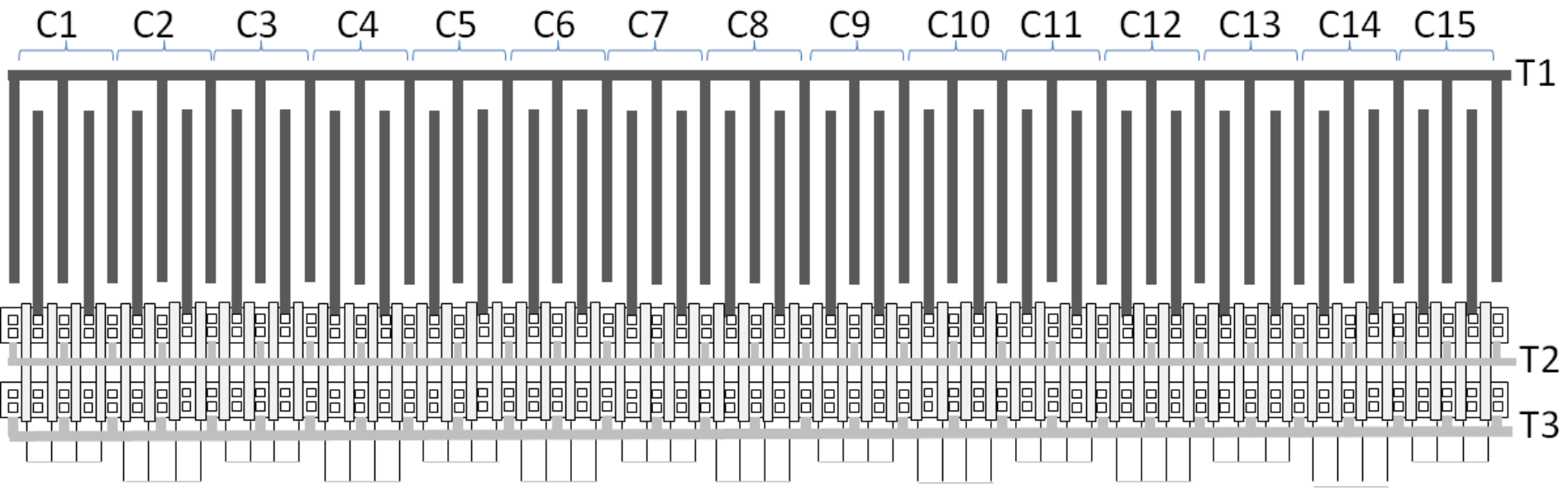


Proposed method: thermometer coded

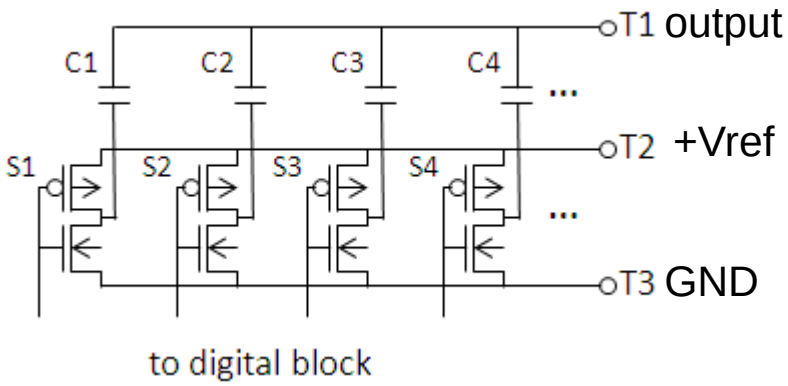


Equal valued capacitors.
Monotonicity is guaranteed.
The code operates to add one by one.

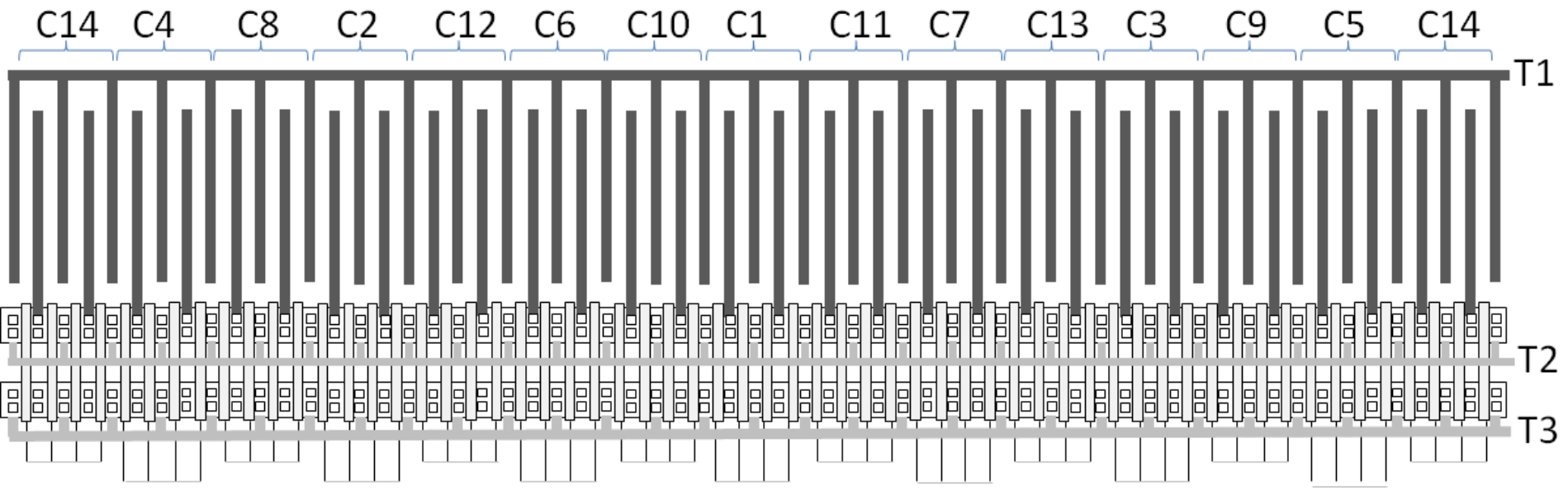
0: all off
1: C1 on
2: C1,C2 on
3: C1,C2,C3 on
:



Proposed method: scrambled thermometer

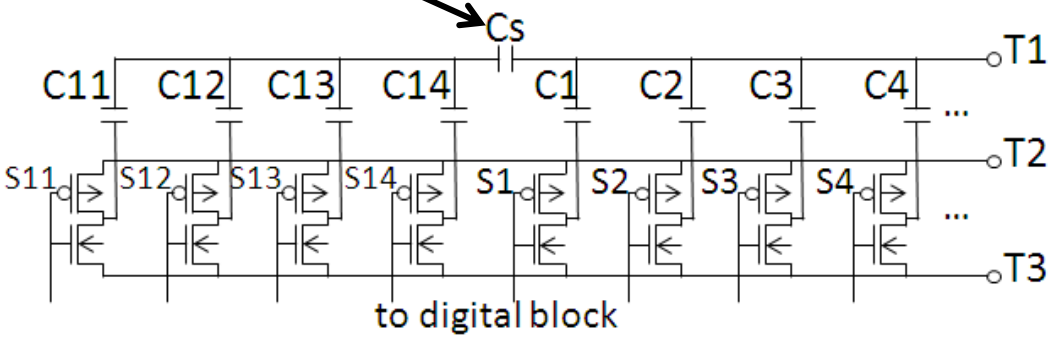


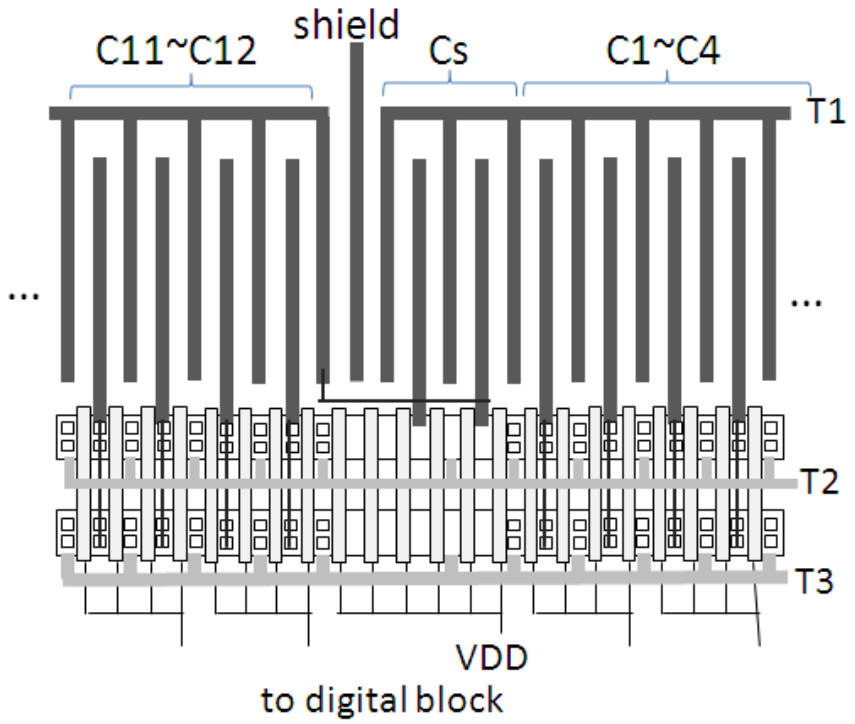
Monotonicity is guaranteed.
Better INL



Proposed method: scaling capacitor layout

- Scaling capacitor (2uint capacitance value) can be located in same slice except metal wires.
- It makes better match to keep same





Proposed method: experimental results

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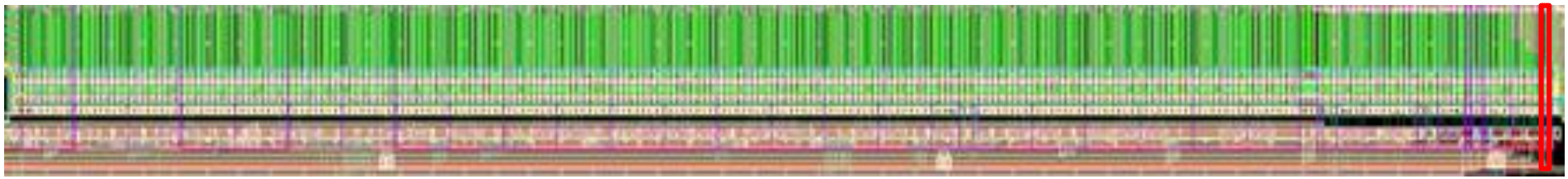
- **Our silicon samples' experimental results**
  - 12bit DAC in SAR ADC
  - DAC core size: 0.0035mm^2=230μm x 15μm (65nm) =1/2.8 of our previous design* (90nm)
  - Clock speed 1GHz. +20% higher then previous design*
  - Power consumption <2mW

*Z.Xu, M.Miyahara, A.Matsuzawa, "A 1ps-resolution Integrator -based Time-to-Digital Converter Using a SAR-ADC in 90nm CMOS", NEWCAS 2013 IEEE 11th International, 16-19

Layout



Proposed method: C+Sw+logic in slice

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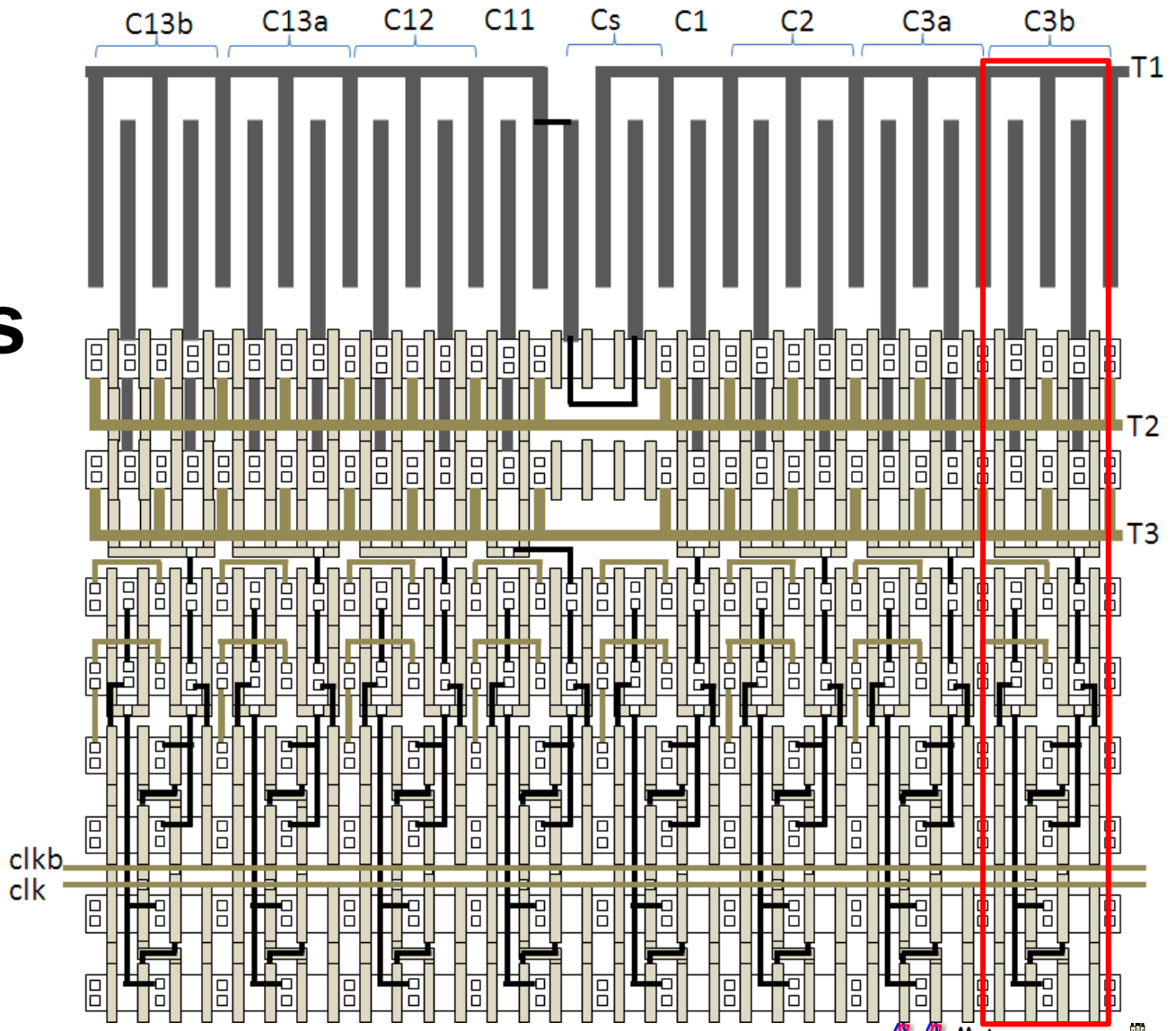
- **Example of capacitor +switches +logic in slice.**
- **Half capacitor in a slice**



Proposed method: R-DAC schematic

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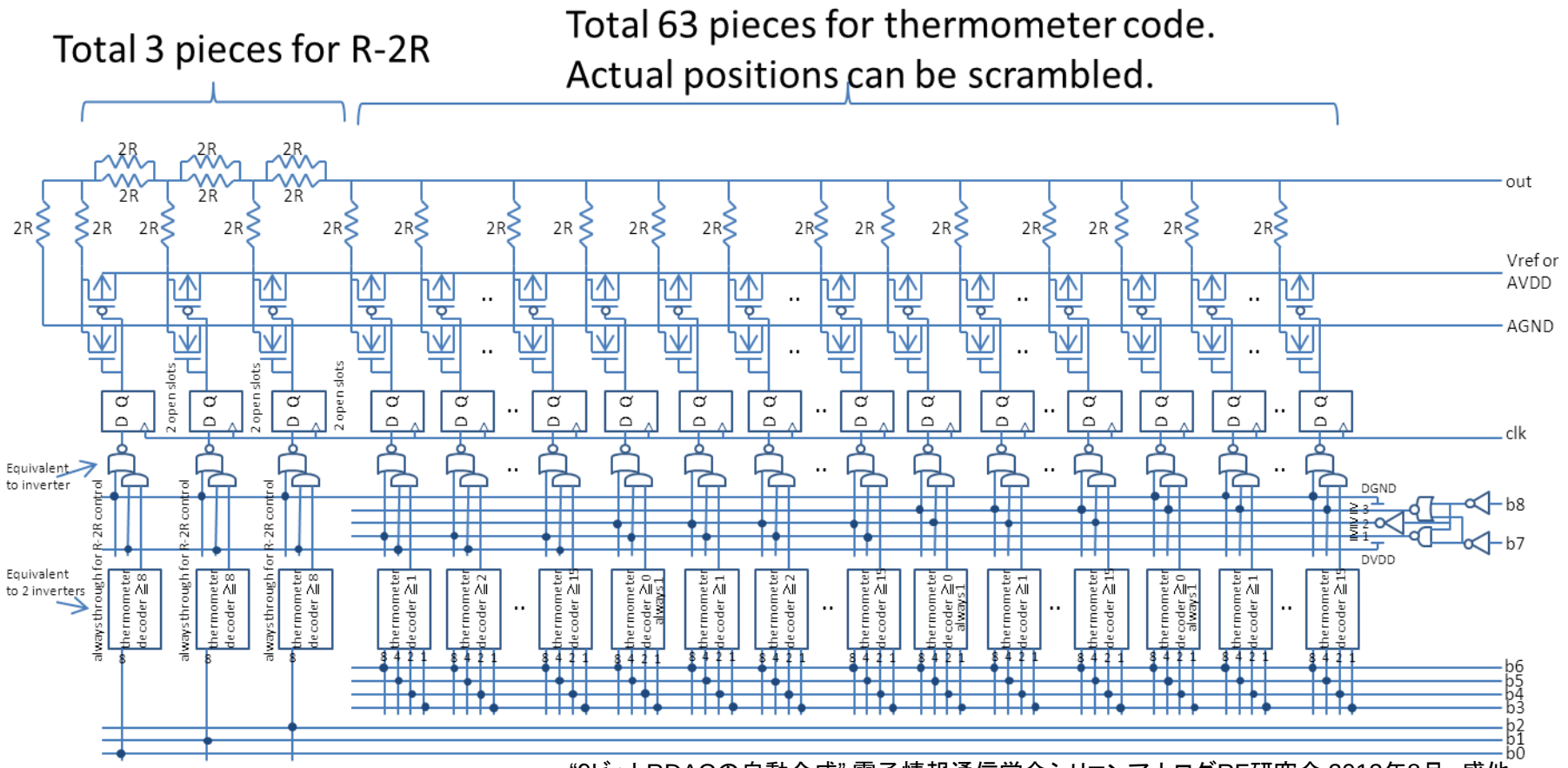
- **Apply to R-2R + segment 9bit DAC**
  - 2R resistor based
  - R + switches + DFF + thermometer coder



"9ビットRDACの自動合成" 電子情報通信学会シリコンアナログRF研究会 2013年8月　盛他

Proposed design method 1

- A required accuracy of unit resistor is calculated as $m/2^{b-n}$, where m is margin
- Its standard deviation σ is given as $\sigma=pelgrom\_coef/sqrt(L*W)$. $m/2^{b-n}=k*pelgrom\_coef/sqrt(L*W)$ (1)
- $R=\rho_s(L+\Delta L)/(W+\Delta W)+2R_c$ (2)
  $R\sim\rho_s*L/W+2R_c$ (2')

Proposed design method 2

- **Where**
  - b: total DAC bit (given)
    n: bit of segment portion (variable)
    R: unit resistor value (given)
  - m=1/4 (default)
    k=3 or 4 (default)
  - pelgrom_coef (from PDK)
    ρ_s (from PDK)
    ΔL (from PDK)
    ΔW (from PDK)
    R_c (from PDK)

Proposed design method 3

- **Hence,**
  $W=(k*\rho_s/m)2^{b-n}sqrt(pelgrom\_coef/R)$ (3)
  If $W<W_{min}$(in PDK) then $W=W_{min}$
- **$L=(R-2R_c)(W-\Delta W)/\rho_s+\Delta L$ (4)**
  If $L<L_{min}$(in PDK) then $L=L_{min}$
  recalculate W