Novel Design Method for ~GHz DAC & Automated Design Program
~GHz DA コンバータの新設計手法と自動設計

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We are developing an automated design tool for D-to-A converters (DACs) up to GHz operation by using knowledge-based technique. First of all, we propose a best-performance layout structure. Then we have developed element size calculation methodology and automated layout methodology. Our prototype program has generated 9bit R-DAC layout and schematic into 0.003mm^2 on 65nm CMOS process within 1mimite.

キーワード：DA コンバータ，アナログ，自動設計，レイアウト・ドリブン, ナレッジ・ベース
(Keywords: D-to-A converter, analog, automated design, layout-driven, knowledge-based)

1. Introduction

Even though digital designs after HDL have been fully automated, still many analog designs are handcrafted especially leading edge ADCs and DACs. In a decade of 1990, many analog automated design tools are proposed by using hierarchal analog design methodologies[(1)(2)(3)(4)], however they couldn't get big successes.

Hierarchy design means that architecture→circuit→ layout in Fig.1 [(1)]. Fig.2 [(2)] shows that layout design was required a lot of constraints from higher level design, and layout design process has iteration loops to meet the constraints including size requirement.

Typical layout engineer can only generate cells by using a cell generator in a layout tool, then put them and route them as an example in Fig.3a and 3b [(5)]. He can give LPE result to circuit engineer. As every analog engineer knows that post layout can only guarantee final performance, layout engineer is given the lowest priority or less design freedoms. Even though iteration path form layout design to circuit or architecture design is figured out in Fig.1, previously layout engineers never initiate the best circuit or architecture designs.

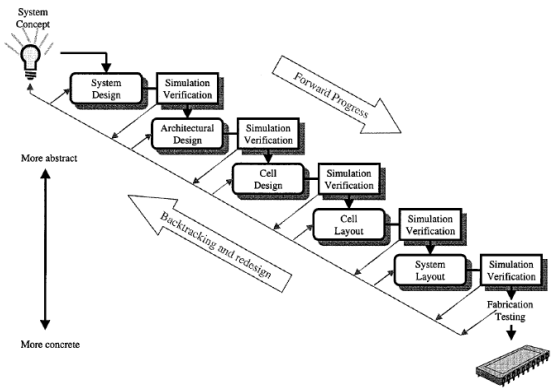


Fig.1 previous automated mixed signal design methodology

2. Proposed novel layout-driven design method

Our design targets are always high-end, and post layout is very important. Thus our approach is to give layout the first priority. First, we tried to reduce worthless ("muda" in Japanese) individual isolations, wires, shields, dummies, etc. as many as possible, by not

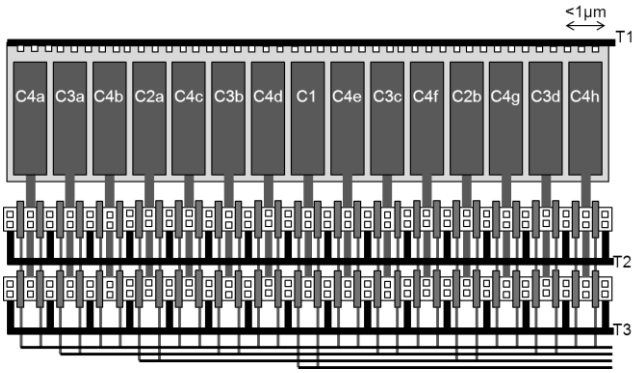


Fig.4 proposed "sub-micron slice" design for DACs

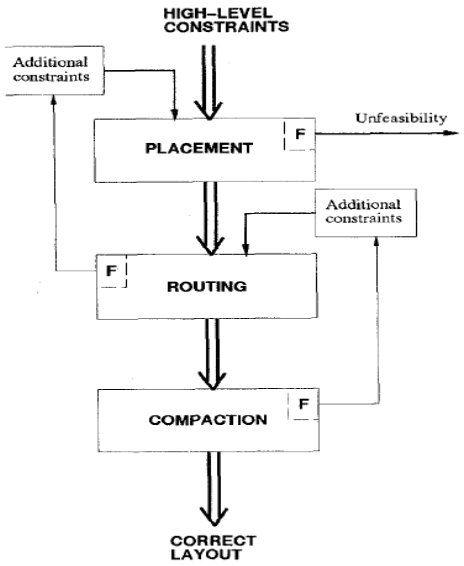
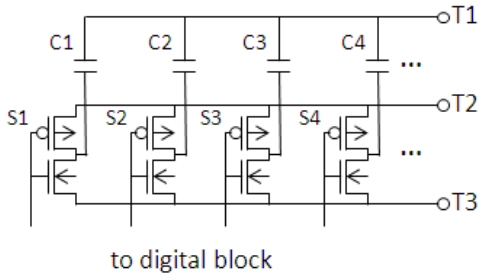


Fig.2 a previous automated layout methodology



1. C1=20fF, C2=40fF, C3=80fF, C4=160fF, ...
2. S1 NMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ...
3. S1 PMOS W/L=2um/Lmin, S2=x2, S3=x4, S4=x8, ...
4. Separate each capacitors or shield.
5. Separate between capacitors and digital block or shield.

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Fig3a a previous C-DAC schematic and layout constraints

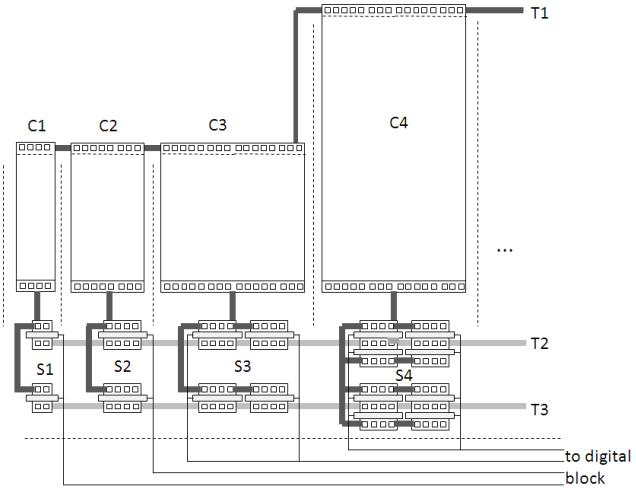

Fig.3b previous C-DAC layout example

using a cell generator. Actually “muda” was necessary evils.

Now we have reached “sub-micron wide slice design” in deep sub-micron CMOS process, shown in Fig.4 instead of Fig.3b.

Because one of nodes of capacitors is connected together to T1 in Fig.2a, no isolation is needed between them. The other nodes of the capacitors will be connected to either T2 (+Vref) or T3 (GND) through switches, why shields are needed between them? We propose unit capacitor width is adjusted to keep same pitch as switches in below columns.

As one side of each switch is connected to either common +Vref or GND, we have laid them with common source structure, connected together through upper metal layers, to reduce isolations and source areas. Pitch or length of 4 gate transistor should be less than 1μm in deep sub-micron CMOS processes. Due to same pitch, the wires between drains and capacitor are straight and less than 1μm. Stray capacitance and resistance are also significant lower than previous design like Fig.3a. Less stray capacitances give us higher speed and lower power consumption than previous designs. We reported [5] other slice structures with MIM capacitors and resistors.

We are also proposing to lay switch control logic out in same pitch. The slice layout rule is that both sides are source nodes. Fig.5 includes thermometer coding logic are located next to each switch, then digital wire lengths between them are 1μm or shorter. No more wire bundle areas are needed between logic block and switch block. In the other words, thermometer control can be realizes with small overhead in addition to binary control. Wires which connect common sources over the transistors with higher metals are not shown in Fig.5. As other logic example, we have reported D flip plop laid in the area [5][6].

The proposed layout structure makes following benefits. We place the slices as tiles, therefore highly regularity with dummies acting shields located only at both ends. Everything in the tiles are same at least analog portions, therefore highly matching is available. No more shield is required if differential. In a case of single-end, top-side only needs shield. Wires on digital portion may be modified at slice by slice.

Again, the sub-micron slice layout structure earns significant lower stray capacitance and resistance without shield losses, then it has higher speed and lower

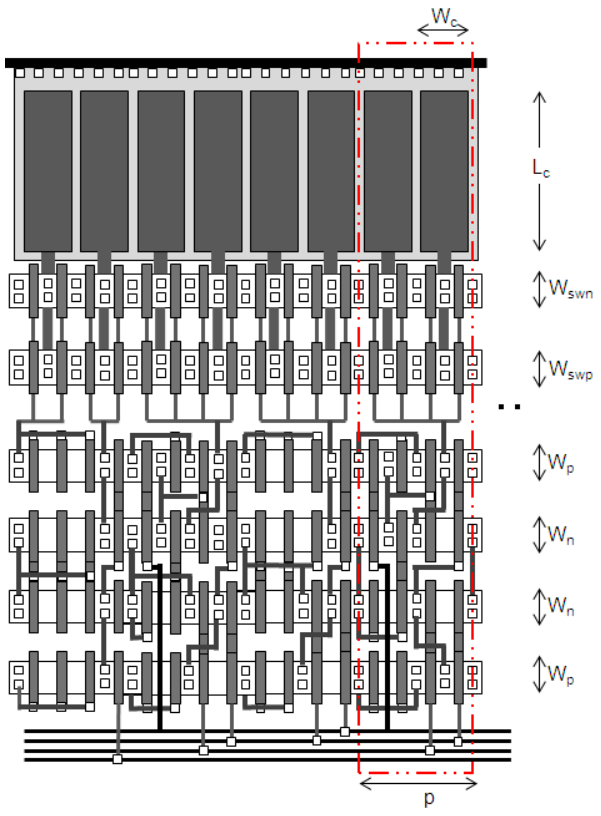

Fig.5 proposed "sub-micron slice with logic" design for DACs

power performances and smaller size than our previous leading edge DACs [7].

3. Proposed element size calculation methodology

Based on above sub-micron slice layout structure, we can select binary control, thermometer control, or their sub-ranging combination. We introduce a variable n as thermometer control for top n bit, including n=0.

We put a given DAC bit number b, and a given unit capacitor or resistor value. Sometimes output capacitance or resistance may be given, in the cases unit capacitor is $x2^{-n}$ or unit resistance is $x2^{n}$.

Unit MIM capacitor size L_c and W_c in Fig.5 is calculated by allowable error vs standard deviation and unit value;

$m / 2^{b-n} = k * pelgrom\_coef / sqrt(L_c * W_c)$

$C = \varepsilon * \varepsilon_0 * L_c * W_c / d$

Here, m and k are margins, and default values are m = 1/4, k = 4. Bigger (L_c*W_c) in above 2 equations is survive. W_c is determined by slice pitch p. The calculations have no iterations.

As we have reported [8] for R-DAC, unit resistor area (L_R * W_R) and value are calculated as

$m / 2^{b-n} = k * pelgrom\_coef / sqrt(L_R * W_R)$

$R = \rho_s (L_R + \Delta L) / (W_R + \Delta W) + 2Rc$

L_R and W_R are calculated from the equations without iterations.

Each switch on-resistance should be lower than allowable error of unit impedance at the highest operating frequency (~GHz). Here, L_{swn} and L_{swp} are set minimum length at analog use, and W_{swn} and W_{swp} are calculated by β_n, β_p, and said allowable on-resistance without iterations.

Logic transistors' L_n and L_p are usually selected minimum values in design rules per process. W_n and W_p are determined by allowable fan-outs (default is 3) or minimum values without iterations.

These element size calculation formulas are similar enough to manage by our program software.

4. Requirements of our automated DAC design tool

We strongly believe above DAC design methodology is suitable for automated designs up to GHz operation. We have started development of automated DAC design tool. The inputs are;

- Given DAC bit size
- Either C or R, and given unit value or output value
- Conversion speed
- Design rule table from each process technology kit
  It guarantees process portability, and at least X axis scalable.
- Evaluation function (area or aspect ratio, etc.) to determine final n value
- Best match n or all n cases can be designed.
- Additional switch option for ADC bottom plate injection, etc.
- Full automation or semi automation

The outputs are;

- Layout
- Schematics for LVS or manual modification
- DRC, LVS, LPE results if required (basically clean by automated design)

5. Automated layout, schematic drawing tool design

We have developed a prototype program for 9bit R-DAC layout and schematic synthesis with SKILL language shown in Fig.6. Element size calculator calculates each L and W from DAC spec and process design rule kit, based on proposed DAC design knowledge. Slice layout and schematic generator generates proposed slice structure by using DAC design

knowledge. Entire DAC layout is generated with tile layout and schematic generator. Our layout approach is straight forward slice placement as tiles basically without additional routing, without iteration and without compaction.

Layout is separated base layers and wiring layers, because base layers are really repeatable and routing layers have more logic variations per slice. We have reported some software architectures [6][9].

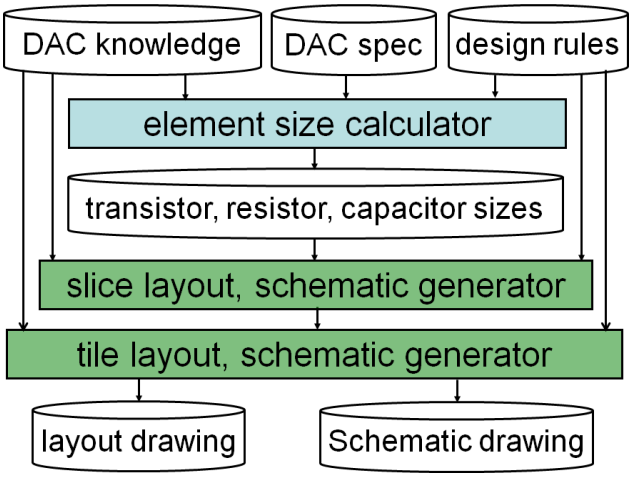

Fig.6 proposed automated design flow

6. Experimental results

We applied proposed design methodology in section 2 and 3 with manual design, before our automated program is ready.

Fig.7 is layout design of 6bit SAR ADC, including 6bit 900Msps C-DAC within 0.003mm² in 65nm CMOS process.

Fig.8 was reported [5][9][10][11] 12bit SAR ADC including a pair of 12bit C-DACs. The C-DAC works 1Gsps, less than 2mW, laid out with in 0.0035mm² in 65nm CMOS process.

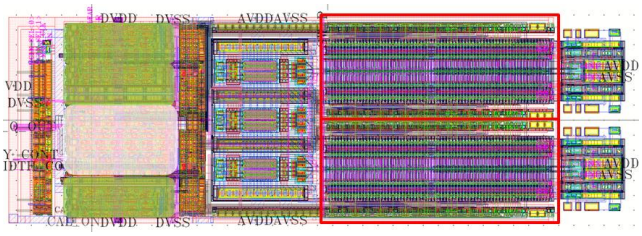

Fig.7 6bit SAR ADC layout including 6bit 900Msps C-DACs

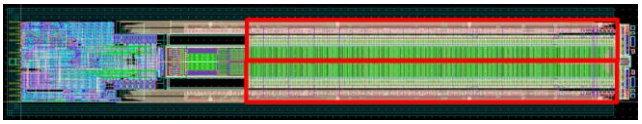

Fig.8 12bit SAR ADC layout including 12bit 1Gsps C-DACs

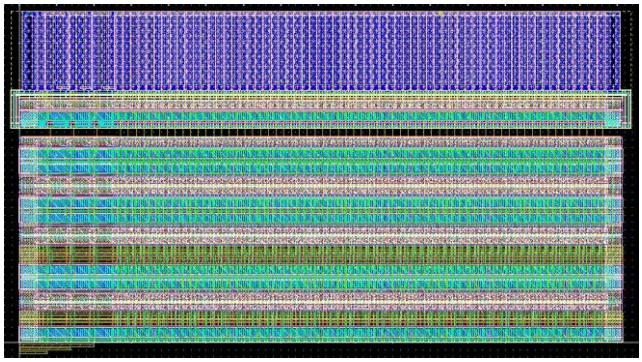

Fig.9 An automated design result of 9bit R-DAC

Fig.9 is a fully automated design result of 9 bit R-DAC by using our prototype program. This result is updated from previous report [5][6] for better DAC linearity.

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