A 60-GHz Efficiency-Enhanced On-Chip Dipole Antenna Using Helium-3 Ion Implantation Process

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***Abstract*—A 60-GHz CMOS on-chip dipole antenna with efficiency-enhancement technique is presented. A helium-3 ion irradiation process is used to reduce the substrate losses of the on-chip antenna. The radiation efficiency of the antenna is doubled using the ion implantation technique. The antenna is fabricated in a 65-nm CMOS technology with a core area of 0.48 mm^2. The on-chip antenna achieves a peak gain of -4.1 dBi at 60GHz and a gain fluctuation of around ±1dB from 57 GHz to 67GHz.**

Keywords—Millimeter-wave, on-chip dipole antenna, CMOS, efficiency-enhanced, helium-3 ion implantation

I. INTRODUCTION

Recently, 60-GHz CMOS wireless transceivers have been investigated intensively because multi-gigabit-per-second wireless communications can be achieved by a small and low-power mobile device [1], [2], [15], [16]. In 60-GHz band, the connections between RF circuits and off-chip antennas introduce parasitic components and radiation loss deteriorating the circuit performance and design flexibility [3]. Moreover, the off-chip antennas largely increase the device size and degrade monolithic integrity.

Fortunately, on-chip antennas do not suffer from the issues mentioned above. However, the on-chip antenna normally has poor radiation efficiency due to the low resistivity of the silicon substrate used in CMOS technologies [4]. Much research has been conducted to improve the radiation efficiency of the CMOS on-chip antennas. Literature [5] and [6] successfully reduce the substrate loss by using artificial magnetic conductor (AMC) at the cost of excessive chip area. Proton implantation techniques [7], [8] are very effective to increase the resistivity of the silicon substrate. Nevertheless, a high dose amount (>10^{15} cm^{-2}) is usually required for the proton implantation, which results in less reliability and high process cost [9], [10].

In this paper, a CMOS on-chip dipole antenna at 60-GHz band with a novel helium-3 ion implantation process [11], [12] is presented. Three different conditions of helium-3 ion irradiation are applied to the on-chip antennas after chip fabrication. The maximum radiation efficiency and power gain of the ion-implanted antennas are improved to twice as much as those of the antennas without implantation with a small dose amount of 3x10^{13} cm^{-2}. The antenna is fabricated in a 65nm CMOS technology with a core area of 0.48 mm^2.

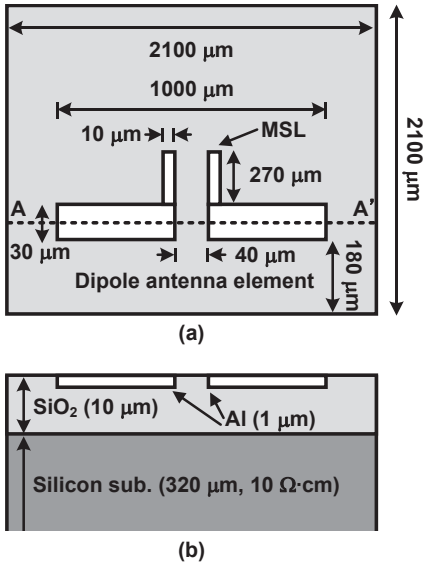

Fig.1. Analysis model of an on-chip dipole antenna (a) top view with antenna configurations; (b) A–A' cross-section view

II. DESIGN OF THE PROPOSED ANTENNA

A. 60-GHz CMOS On-Chip Antenna

It is well-known that the CMOS on-chip antenna generally performs low radiation efficiency and power gain because of the low resistivity and high permittivity of the lossy silicon substrate used in CMOS technologies. In order to gain a quantitative insight for the loss contribution, an analysis model of an on-chip dipole antenna is constructed as depicted in Fig.1. The top metal layer (Al) with 1 μm thickness is used for the dipole elements which are fed by two micro-strip lines (MSLs). The silicon substrate (ε_r = 12) is modeled by a lossy layer with resistivity of 10 Ω·cm and 320 μm thickness. The detailed dimensions of the antenna are illustrated in Fig. 1 (a). Fig. 2 (a) shows the simulated radiation gain pattern of the dipole antenna at 60 GHz using the model described in Fig. 1. The radiation gain at X direction with φ=0° is -8.2 dBi which corresponds to an efficiency of 26%. It is interesting to note that the silicon substrate contributes around 70% of losses. Therefore, reducing the substrate loss is an effective solution to improve on-chip antenna efficiency and power gain.

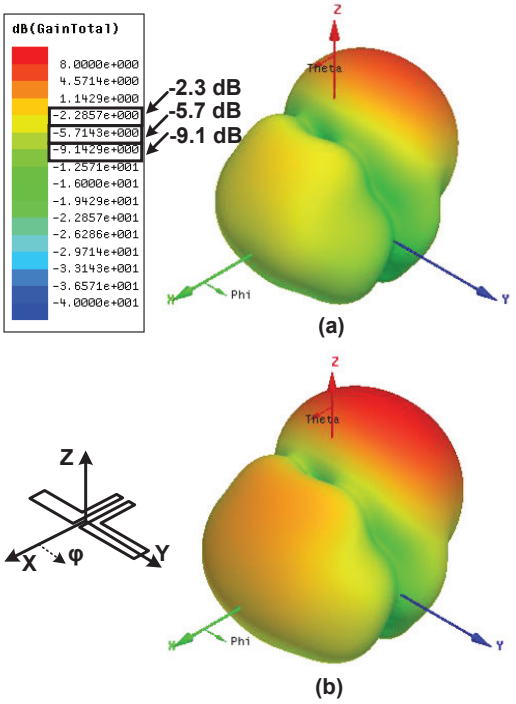

Fig.2. Simulated 3-D gain pattern of the on-chip antenna (a) with lossy substrate (10 Ω·cm); (b) with high resistivity substrate (1000 Ω·cm)

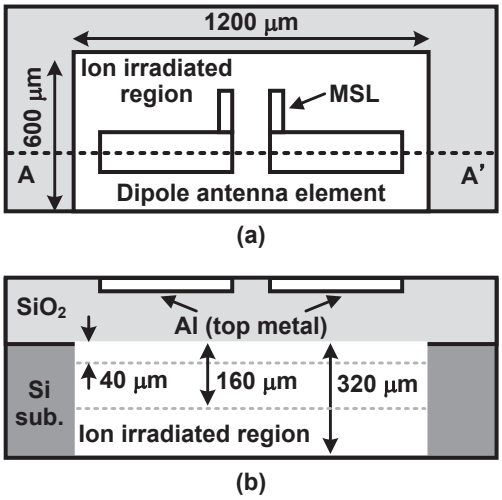

Fig.3. The proposed helium-3 ion implanted dipole antenna (a) top view; (b) A–A' cross-section view

B. *Helium-3 Ion Implantation*

In this work, a novel helium-3 ion implantation technique is used to enhance the on-chip antenna efficiency and power gain by effectively increasing the substrate resistivity. The helium-3 ions are implanted to the antenna chip using a cyclotron after the chip is fabricated. An aluminum mask plate with 0.5 mm thickness is used to protect the chip area outside of the ion-irradiated region. Due to charge trappings created by the irradiation and Coulomb scattering of the charged traps, the

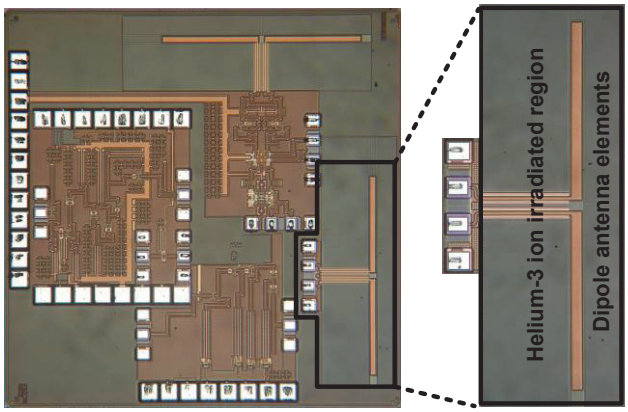

Fig. 4. Die micro-photograph. Core area: 0.48 mm^2

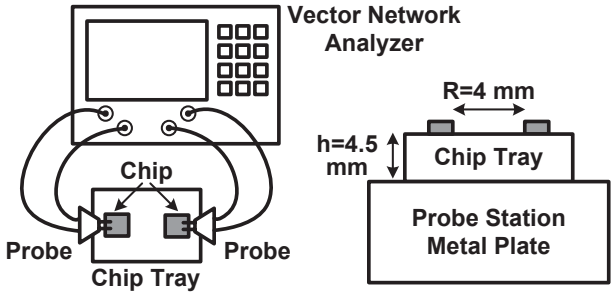

Fig.5. Illustration of the on-wafer measurement setup for the power gain of the on-chip antenna.

substrate resistivity increases with the increasing of the dose amount. Typically, the substrate resistivity can be effectively increased from 6 Ω·cm to over 1000 Ω·cm with a small dose amount of $3x10^{13}$ cm^{-2} by utilizing the helium-3 ion implantation technique. Meanwhile, helium-3 ion has less lateral scattering compared with proton. The calculated beam spread range for helium-3 ion is about half of that for proton at 300-μm stopping range [12]. Therefore, a high-reliability low-process-cost ion implantation technique can be utilized to increase the substrate resistivity. Fig. 3 shows the proposed CMOS on-chip dipole antenna with helium-3 ion implantation technique. The antenna configuration is the same as in Fig. 1 except the 600 μm×1200 μm white area around the antenna indicates the ion irradiated region. To further investigate the ion implantation technique, three different irradiation depths of helium-3 ions (40 μm, 160 μm, and 320 μm) are applied to the on-chip antenna. Simulations results demonstrate that the radiation efficiency is increased to 59% when the irradiation depth of 320 μm is applied as shown in Fig. 2(b).

III. Measurement Results and Discussions

To validate the analysis and design, the on-chip dipole antenna is fabricated in a 65 nm CMOS technology. Fig. 4 shows the die micro-photograph of the antenna with a core area of 0.48 mm^2. The helium-3 ions are implanted within the area indicated in Fig. 4 after the chip is fabricated. Three different

TABLE I
COMPARISON WITH PREVIOUSLY REPORTED 60-GHZ BAND ON-CHIP ANTENNAS

Ref.	Process	Type of antenna	Frequency	Antenna gain	Core area
This work	65 nm CMOS	Dipole with helium-3 ion implantation	60 GHz	**-4.1 dBi**	**0.48 mm^2**
[4]	180 nm CMOS	Yagi	60 GHz	-10 dBi	0.74 mm^2*
[5]	180 nm CMOS	Circularly polarized with AMC	65 GHz	-4.4 dBi	3.24 mm^2
[6]	90 nm CMOS	Yagi with AMC	60 GHz	-7.2 dBi	1.04 mm^2
[13]	65 nm CMOS	Slot loop	60 GHz	-5.0 dBi*	0.64 mm^2*
[14]	Post-back-end-of-line	Inverted-F	61 GHz	-19.0 dBi	0.20 mm^2*
		Quasi-Yagi	65 GHz	-12.5 dBi	0.59 mm^2*

* Estimated from literature

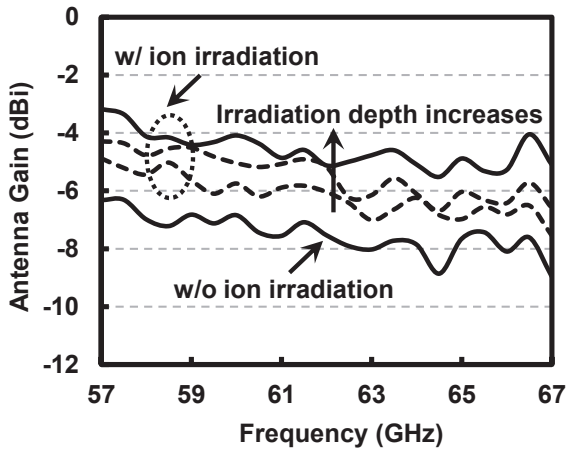

Fig.6. Measured antenna power gain with and without helium-3 ion irradiation

irradiation depths of helium-3 ions (40 μm, 160 μm, and 320μm) are employed for the on-chip antenna with the same dose amount of 3x10^{13} cm^{-2}. The on-chip antenna without ion implantation is also measured for comparison.

The power gain of the on-chip antenna is measured using the setup shown in Fig. 5. Two identical antennas located on the probe station are placed face-to-face with a distance R=4mm. The losses of the measurement equipments and cables are calibrated to the probe tips using standard impedance substrates. The power gain of one single antenna can be expressed as [4]

$$G\ (\mathrm{dB}) = \frac{1}{2}[\mathrm{IL(dB)} - \mathrm{PL(dB)}] \quad (1)$$

$$\mathrm{PL\ (dB)} = 10\log[\left(\frac{\lambda_0}{4\pi R}\right)^2 \times \left|1 - \frac{R}{\sqrt{R^2+4h^2}}\, e^{-ik_0\left(\sqrt{R^2+4h^2}-R\right)}\right|^2] \quad (2)$$

$$\mathrm{IL\ (dB)} = 10\log\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) \quad (3)$$

where PL is the path loss considering the effect of the metal plate on the probe station. IL is the measured insertion loss between the two antennas from the vector network analyzer (VNA).

Fig. 6 shows the measured power gain of the on-chip antenna with and without the ion implantation. When the ion irradiation is not applied, the radiation gain of over -9 dBi is achieved from 57 GHz to 67 GHz with the gain variation of less than 3 dB. It can be observed that with the increasing of the helium-3 ion irradiation depth, the antenna gain is gradually enhanced, which implies that the radiation efficiency of the on-chip antenna is improved. When the irradiation depth of 320μm is applied, the radiation gain is improved to be higher than -5.5 dBi. The average gain improvement is about 3 dB over the 10-GHz band of interest. The wide-and-flat gain characteristic of the on-chip antenna is maintained after the ion-irradiated processing.

The S-parameter of the on-chip antennas is also measured for accurately de-embedding the losses of the measurement equipment as illustrated in Fig. 7. The degradation of the input reflection coefficient for the ion-irradiated antennas is caused by the change of the dipole antenna characteristics after ion implantation. The losses due to the reflection are de-embedded for the gain measurement.

The radiation gain pattern of the on-chip antenna for XY-plane at 60 GHz is measured and illustrated in Fig. 8. The on-chip antennas without ion irradiation and with ion irradiation depth of 320 μm are used for the measurement. The improvement of the power gain for different directions is obvious as demonstrated in Fig. 8.

Table I shows a performance comparison of the proposed on-chip dipole antenna and other state-of-the-art on-chip antennas at 60-GHz band. The proposed antenna achieves

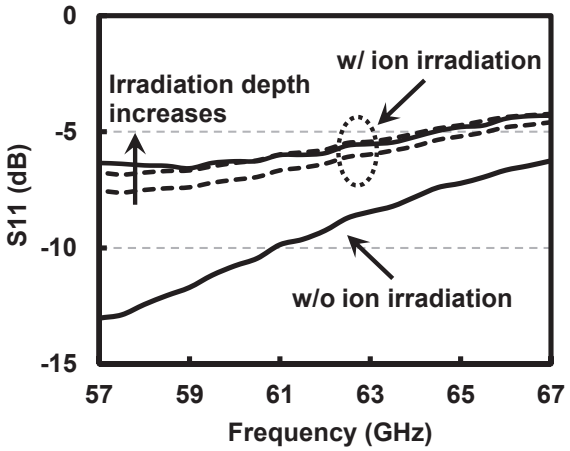

Fig.7. Measured S11 of the on-chip antenna with and without ion irradiation

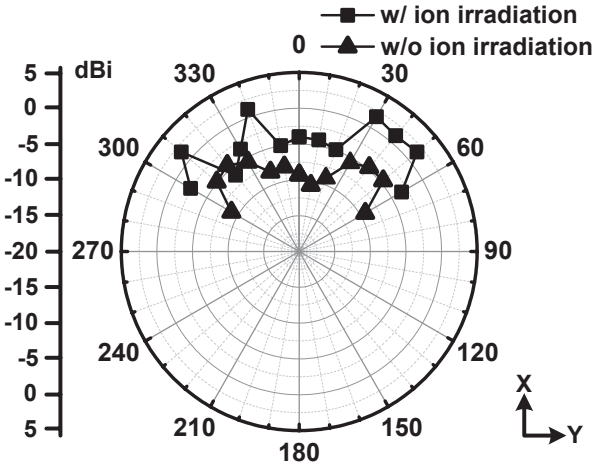

Fig.8. Measured XY-plane radiation pattern of the on-chip antenna at 60 GHz with (320 μm depth) and without ion irradiation.

relatively high power gain (-4.1 dBi@60 GHz) with reasonable area occupation (0.48 mm^2).

IV. Conclusion

This paper presents a 60-GHz on-chip dipole antenna with helium-3 ion implantation technique in a 65 nm CMOS technology. By using the small dose amount of $3x10^{13}$ cm^{-2} for ion implantation process, 3-dB average gain improvement of the antenna is achieved across 57 GHz to 67 GHz. The peak gain of the antenna at 60 GHz is -4.1 dBi and the chip core area is only 0.48 mm^2.

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References

[1] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3 Gb/s 60 GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 218–219.

[2] K. Okada, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, S. Kondo, T. Ueno, Y. Takeuchi, T. Yamaguchi, A. Musa, R. Wu, M. Miyahara, and A. Matsuzawa, "A 64-QAM 60 GHz CMOS Transceiver with 4-channel Bonding," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 346–347.

[3] T. Hirano, T. Yamaguchi, N. Li, K. Okada, J. Hirokawa, and M. Ando, "60 GHz on-chip dipole antenna with differential feed," in *Proc. Asia-Pacific Microwave Conference*, 2012, pp. 304–306..

[4] H.-R. Chuang, L.-K. Yeh, P.-C. Kuo, K.-H. Tsai, and H.-L. Yue, "A 60-GHz millimeter-wave CMOS integrated on-chip antenna and bandpass filter," *IEEE Transactions on Electron Devices*, vol. 58, no. 7, pp. 1837-1845, Jul. 2011.

[5] X.-Y. Bao, Y.-X. Guo, and Y.-Z. Xiong, "60-GHz AMC-based circulary polarized on-chip antenna using standard 0.18- μm CMOS technology," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 5, pp. 2234-2241, May 2012.

[6] H.-C. Kuo, H.-L. Yue, Y.-W. Ou, C.-C. Lin, and H.-R. Chuang, "A 60-GHz CMOS sub-harmonic RF receiver with integrated on-chip artificial-magnetic-conductor Yagi antenna and balun bandpass filter for very-short-range gigabit communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1681-1691, Apr. 2013.

[7] C. Liao, T.-H. Huang, C.-Y. Lee, D. Tang, S.-M. Lan, T.-N. Yang, and L.-F. Lin, "Method of creating local semi-insulating regions on silicon wafers for device isolation and realization of high-Q inductors," *IEEE Electron Device Letters*, vol. 19, no. 12, pp. 461–462, Dec. 1998.

[8] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, T. S. Duh, and W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-quartz," *IEEE International Electron Devices Meeting (IEDM)*, 2001, pp. 40.6.1-40.6.4.

[9] K. T. Chan, A. Chin, Y. D. Lin, C. Y. Chang, C. X. Zhu, M. F. Li, D. L. Kwong, S. McAlister, D. S. Duh, and W. J. Lin, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 11, pp. 487-489, Nov. 2003.

[10] L. S. Lee, C. Liao, C.-L. Lee, T.-H. Huang, D. D.-L. Tang, T. S. Duh, and T.-T. Yang, "Isolation on Si wafers by MeV proton bombardment for RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 928–934, May 2001.

[11] R. Wu, W. Deng, S. Sato, T. Hirano, N. Li, T. Inoue, H. Sakane, K. Okada, and A. Matsuzawa, "A 17-mW 5-Gb/s 60-GHz CMOS transmitter with efficiency-enhanced on-chip antenna," *IEEE RFIC Symp. Dig.*, 2014, pp. 381-384.

[12] N. Li, K. Okada, T. Inoue, T. Hirano, Q. Bu, A. T. Narayanan, T. Siriburanon, H. Sakane, and A. Matsuzawa, "High-Q inductors on locally semi-insulated Si substrate by helium-3 bombardment for RF CMOS integrated circuits," *IEEE Symp. VLSI Technology Dig. Tech. Papers*, 2014, pp. 189-190.

[13] L. Kong, D. Seo, and E. Alon, "A 50mW-TX 65mW-RX 60GHz 4-element phased-array transceiver with integrated antennas in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 234–235.

[14] Y. P. Zhang, M. Sun, and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1664–1668, Jul. 2005.

[15] V. Vidojkovic, G. Mangraviti, K. Khalaf, V. Szortyka, K. Vaesen, W.V. Thillo, B. Parvais, M. Libois, S. Thijs, J.R. Long, C. Soens, and P. Wambacq, "A low-power 57-to-66 GHz transceiver in 40 nm LP CMOS with -17 dB EVM at 7 Gb/s," *IEEE ISSCC Dig. Tech. Papers*, 2012, pp.268–269.

[16] T. Mitomo, Y. Tsutsumi, H. Hoshino, M. Hosoya, T. Wang, Y. Tsubouchi, R. Tachibana, A. Sai, Y. Kobayashi, D. Kurose, T. Ito, K. Ban, T. Tandai, and T. Tomizawa, "A 2 Gb/s-throughput CMOS transceiver chipset with in-package antenna for 60 GHz short-range wireless communication," *IEEE ISSCC Dig. Tech. Papers*, 2012, pp.266–267.