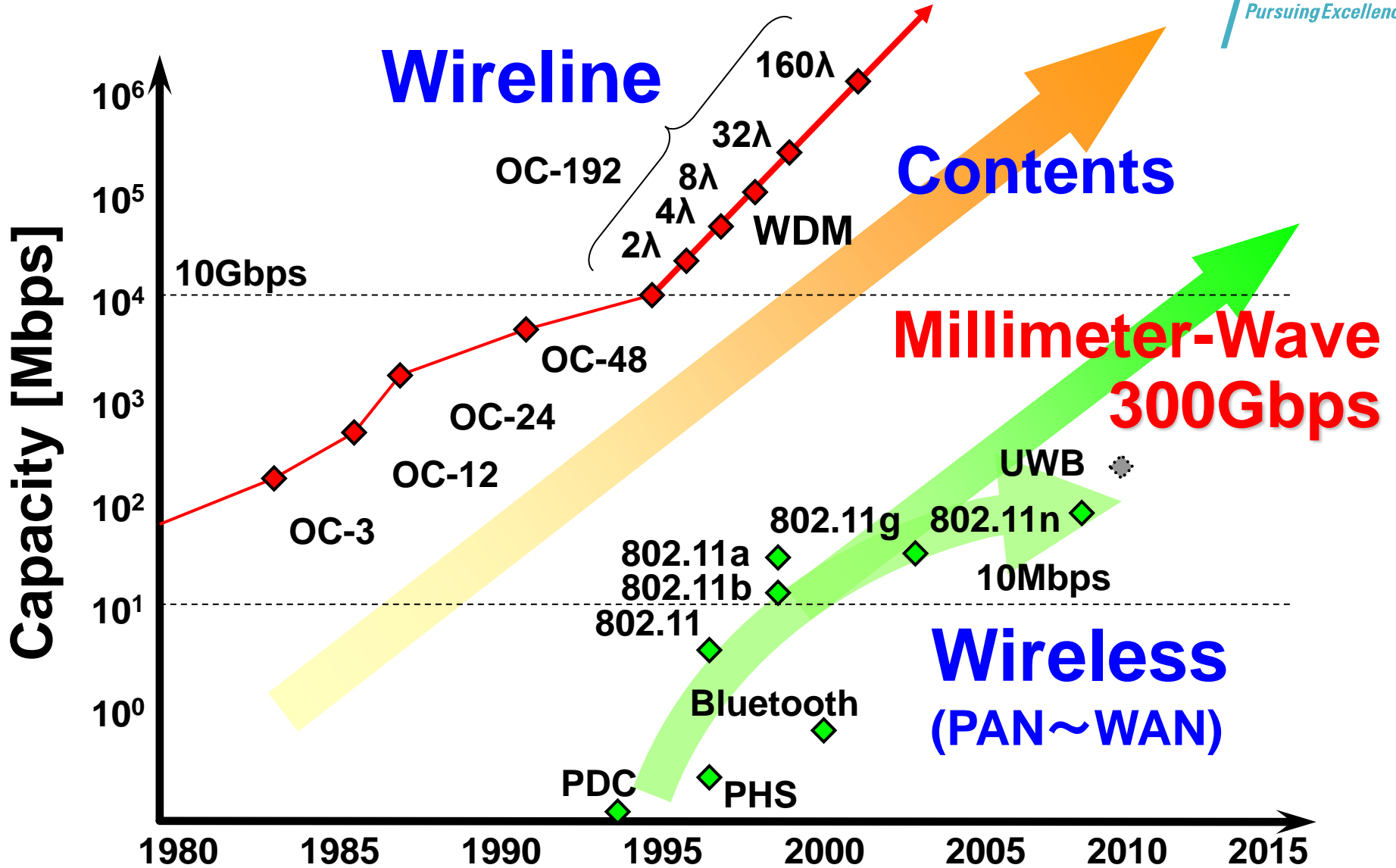


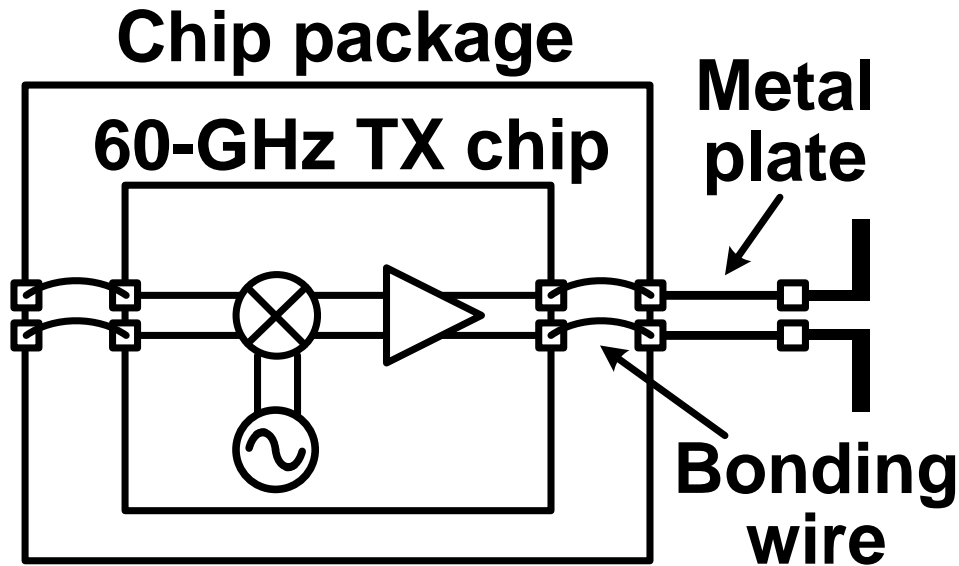
# A 60-GHz Efficiency-Enhanced On-Chip Dipole Antenna Using Helium-3 Ion Implantation Process

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**Tokyo Institute of Technology, Japan**

- **60-GHz Application and CMOS On-Chip Antenna**
- **Conventional Solutions**
- **Proposed On-Chip Antenna using Helium-3 Ion Irradiation**
- **Performance Comparison and Conclusions**

# Motivation

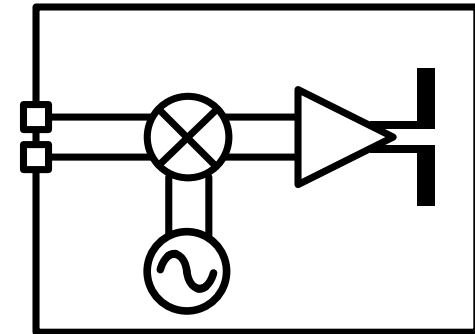




## Off-chip antenna:

- 😊 High radiation gain
- 😞 parasitic components and loss for connection
- 😞 Degrade system performance and design flexibility

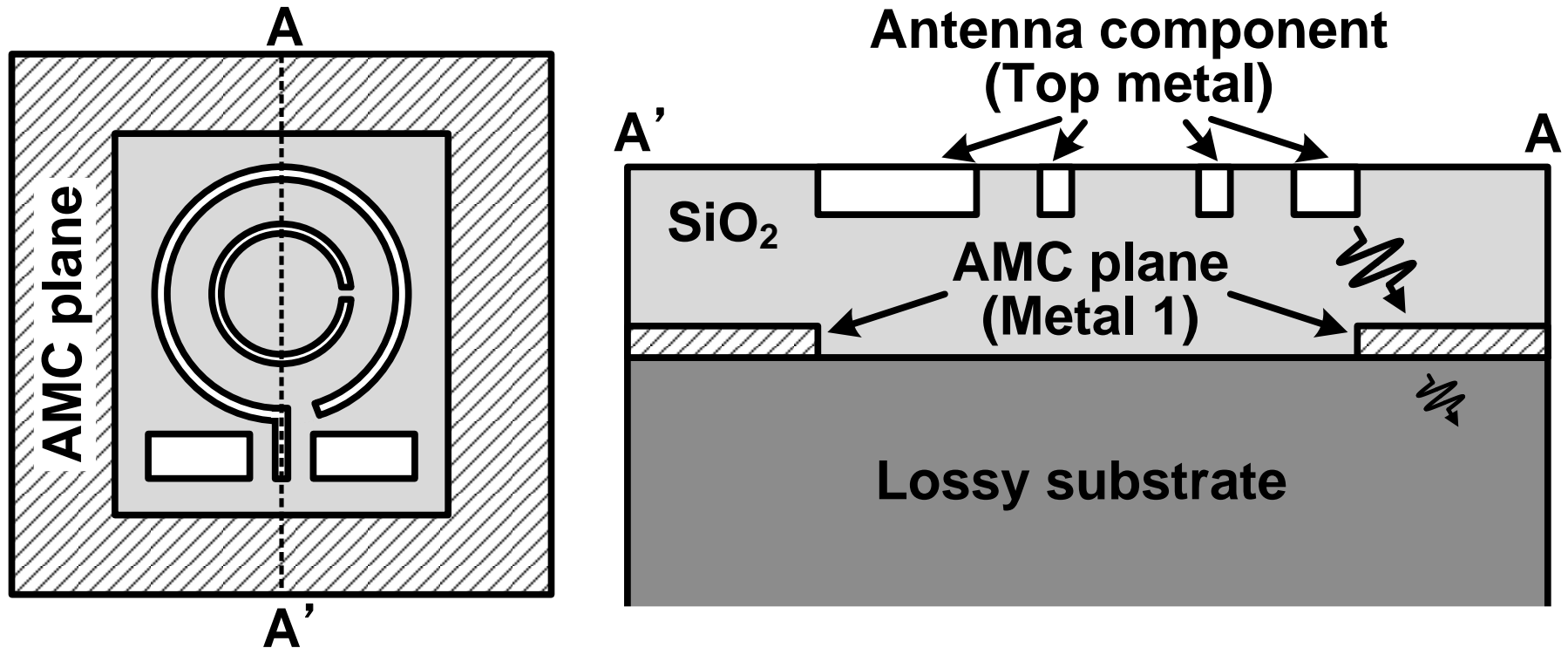
## 60-GHz TX chip



## CMOS On-chip antenna:

- 😊 Much less parasitic and connection loss
- 😊 flexible design and monolithic integration
- 😞 Poor radiation gain due to lossy substrate

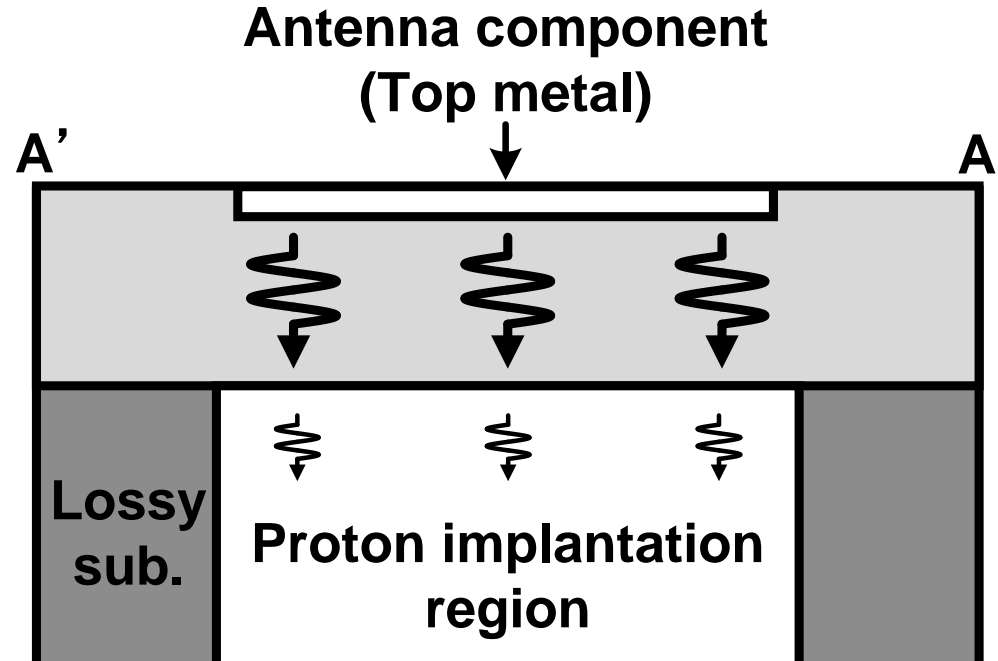
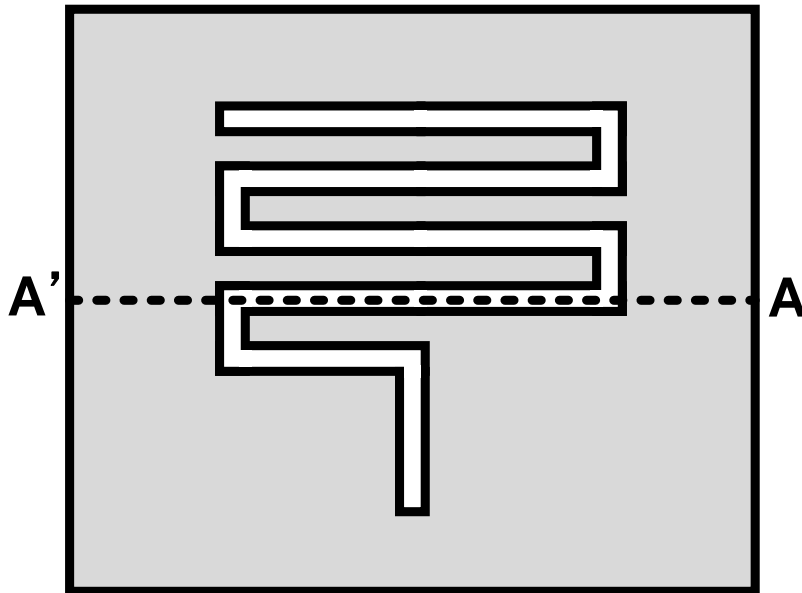
- Artificial Magnetic Conductor (AMC)



- ☺ High-Z surface to prevent EM field induced in the lossy substrate
- ☹ Large area for AMC pattern

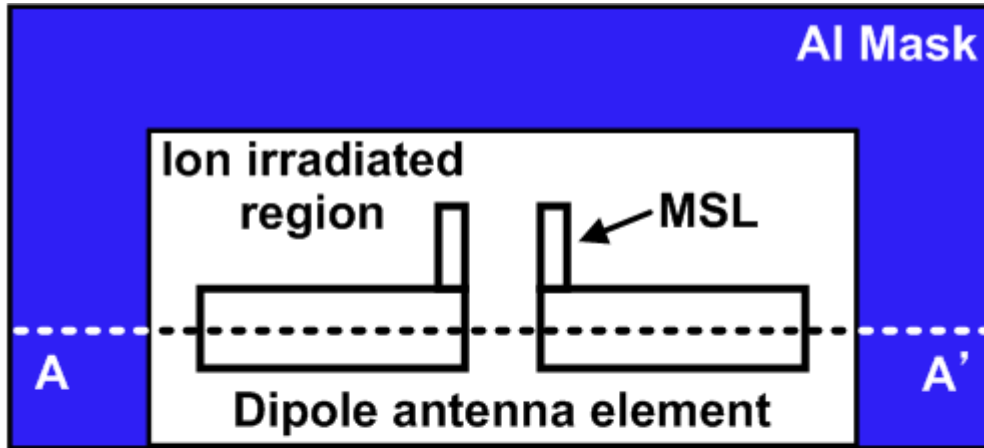
[1] X.-Y. Bao *et al.*, ITAP 2012

- Proton implantation



- ☺ Increase substrate resistivity to prevent induced EM field
- ☹ High dose amount and process cost

[2] K.-T. Chan *et al.*, IEDM 2001

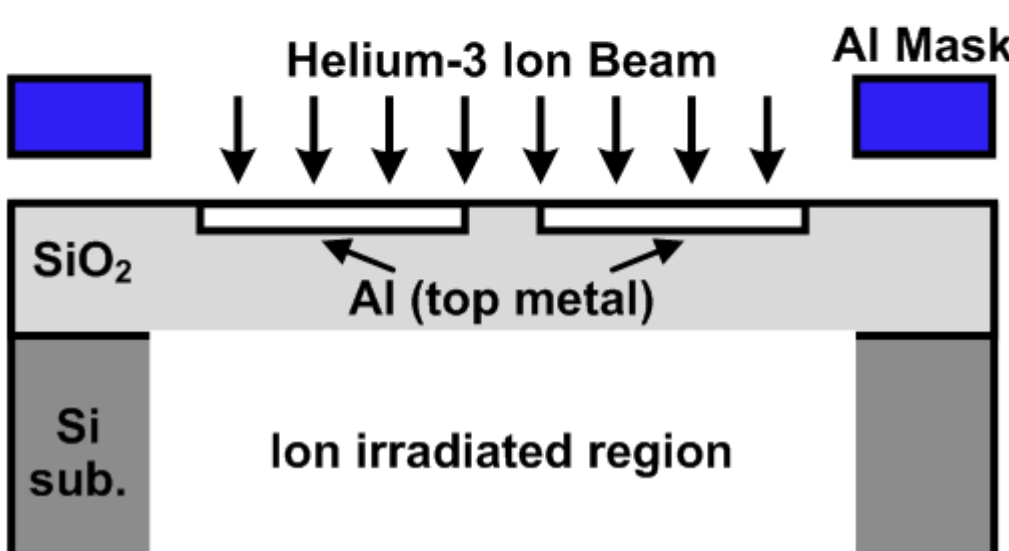


**Helium-3 ion irradiation**

☺ **Increase substrate resistivity ( $\approx 10^3 \Omega \cdot \text{cm}$ )**

☺ **Less dose amount and process cost**

☺ **Less lateral scattering and higher reliability**



# Helium-3 Bombardment Procedure

7

TOKYO TECH

**Confidential**

Auto-Transport Wafers  
irradiated one by one

Set wafer in plate



Move plate into  
chamber



Vacuum pumping



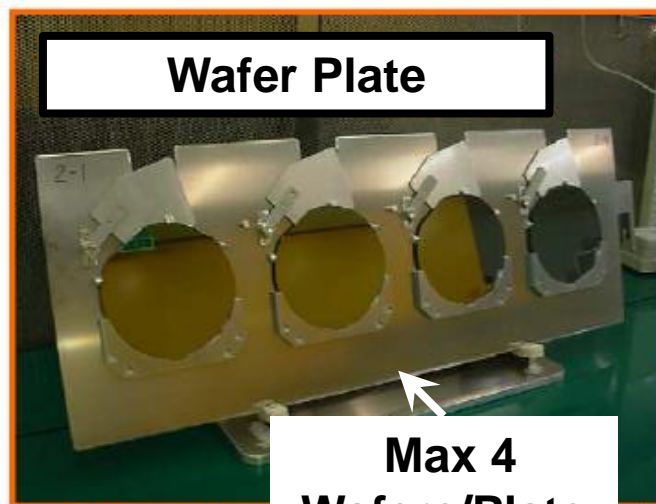
Ion irradiation



Air pumping



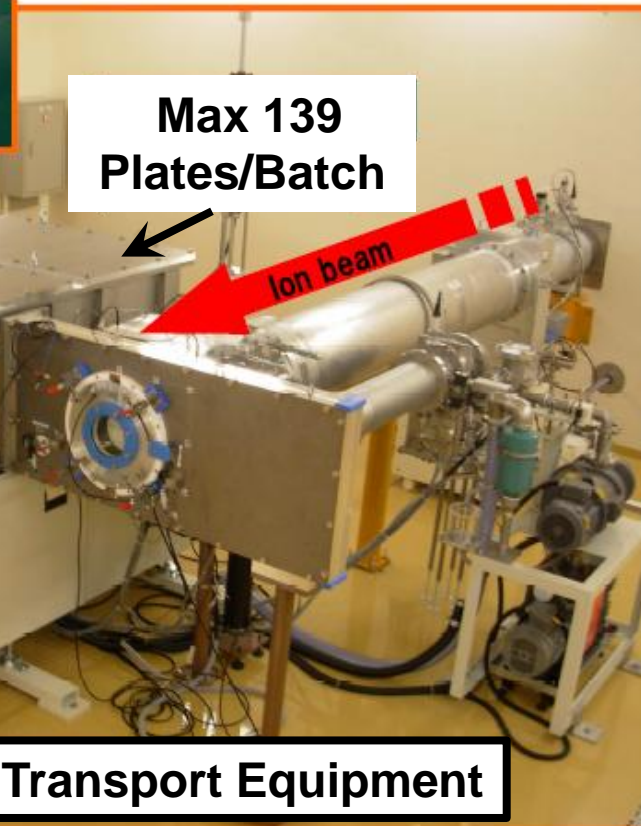
Move plate out of  
chamber



Wafer Plate

Max 4  
Wafers/Plate

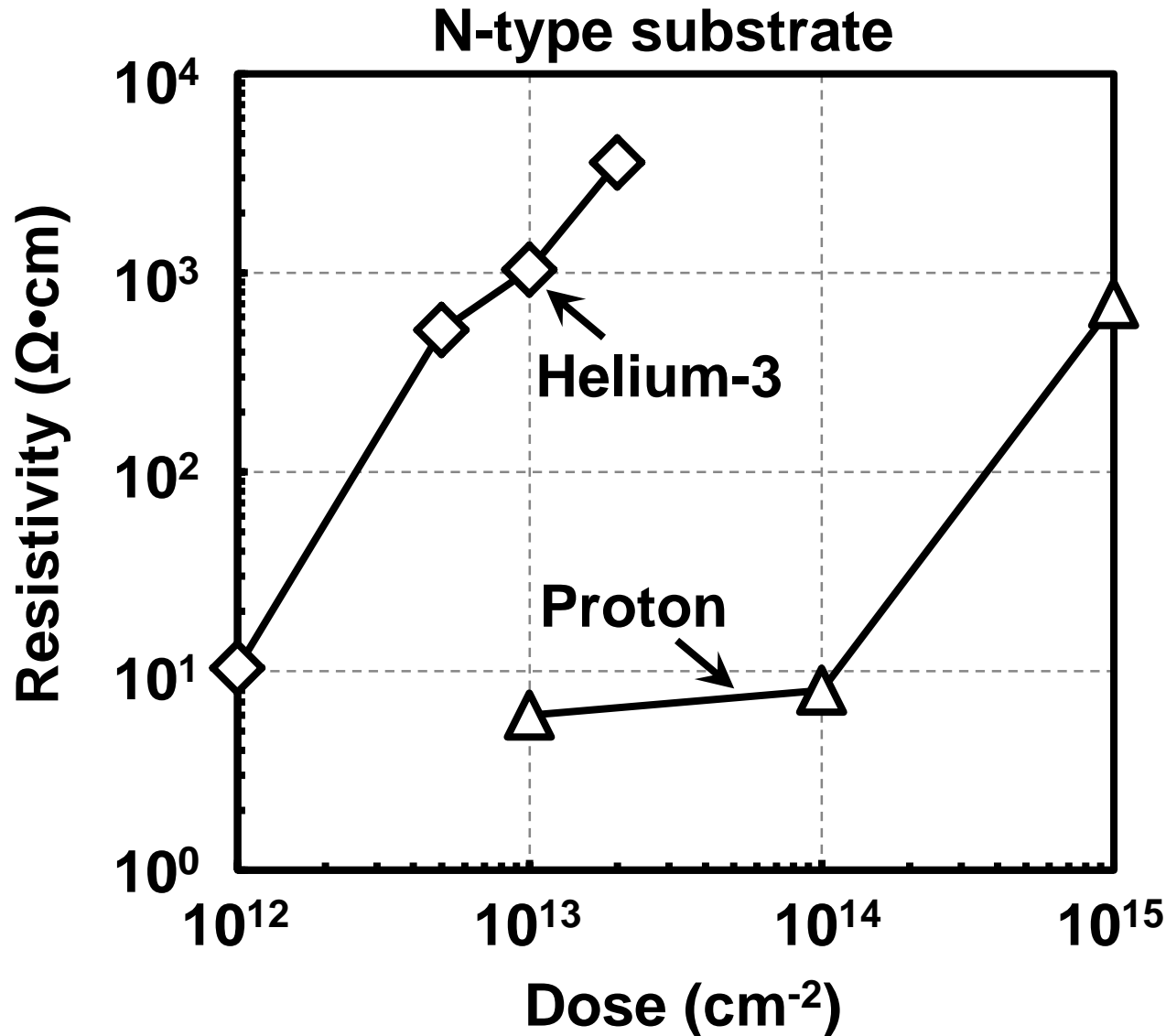
Wafer Chamber



Max 139  
Plates/Batch

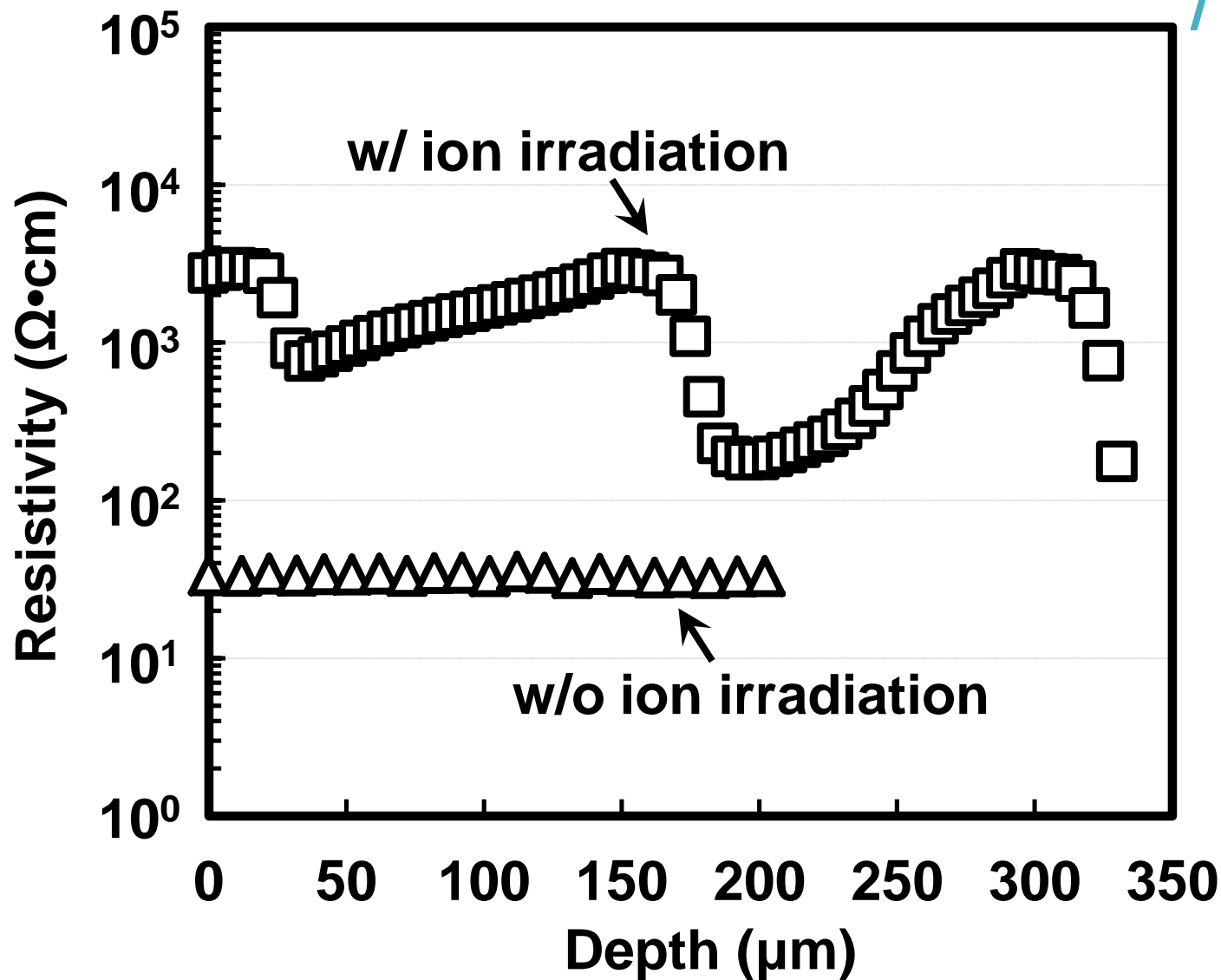
Wafer Transport Equipment



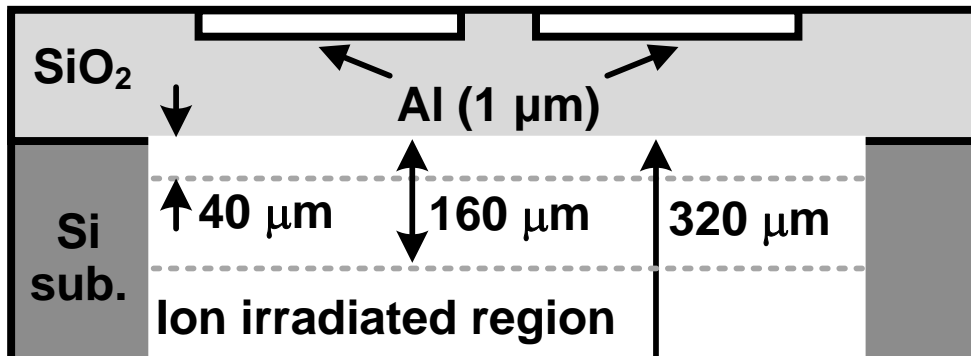
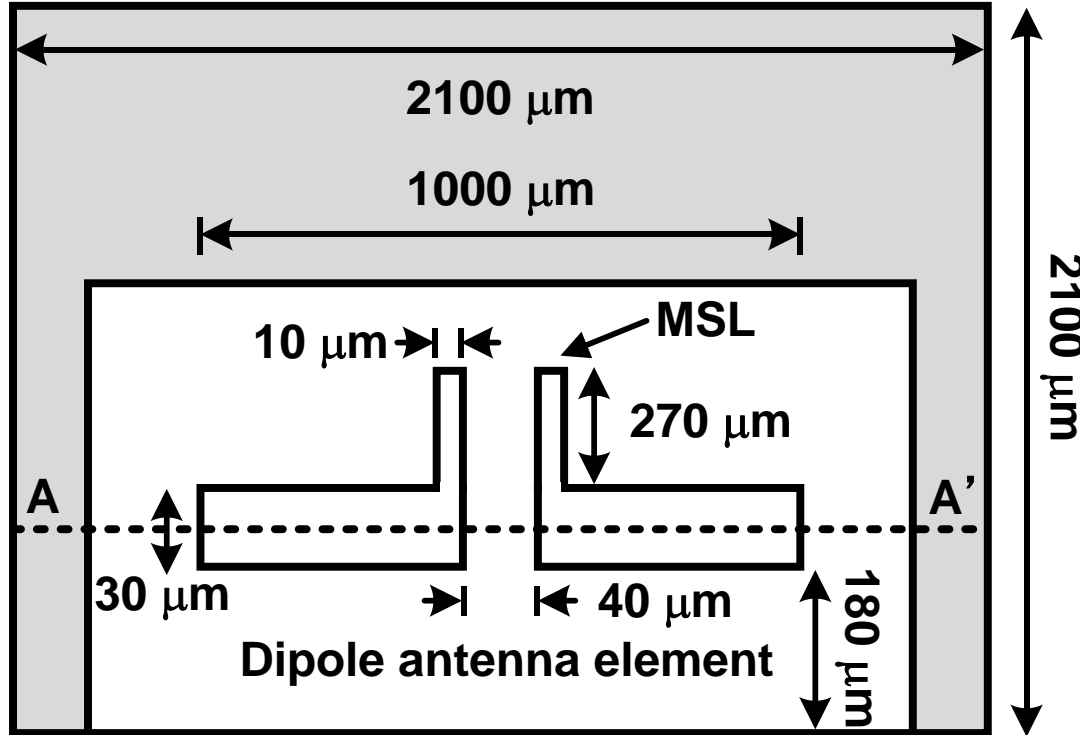


[3] N. Li *et al.*, VLSI Technology 2014

[4] L.-S. Lee *et al.*, ITED 2001

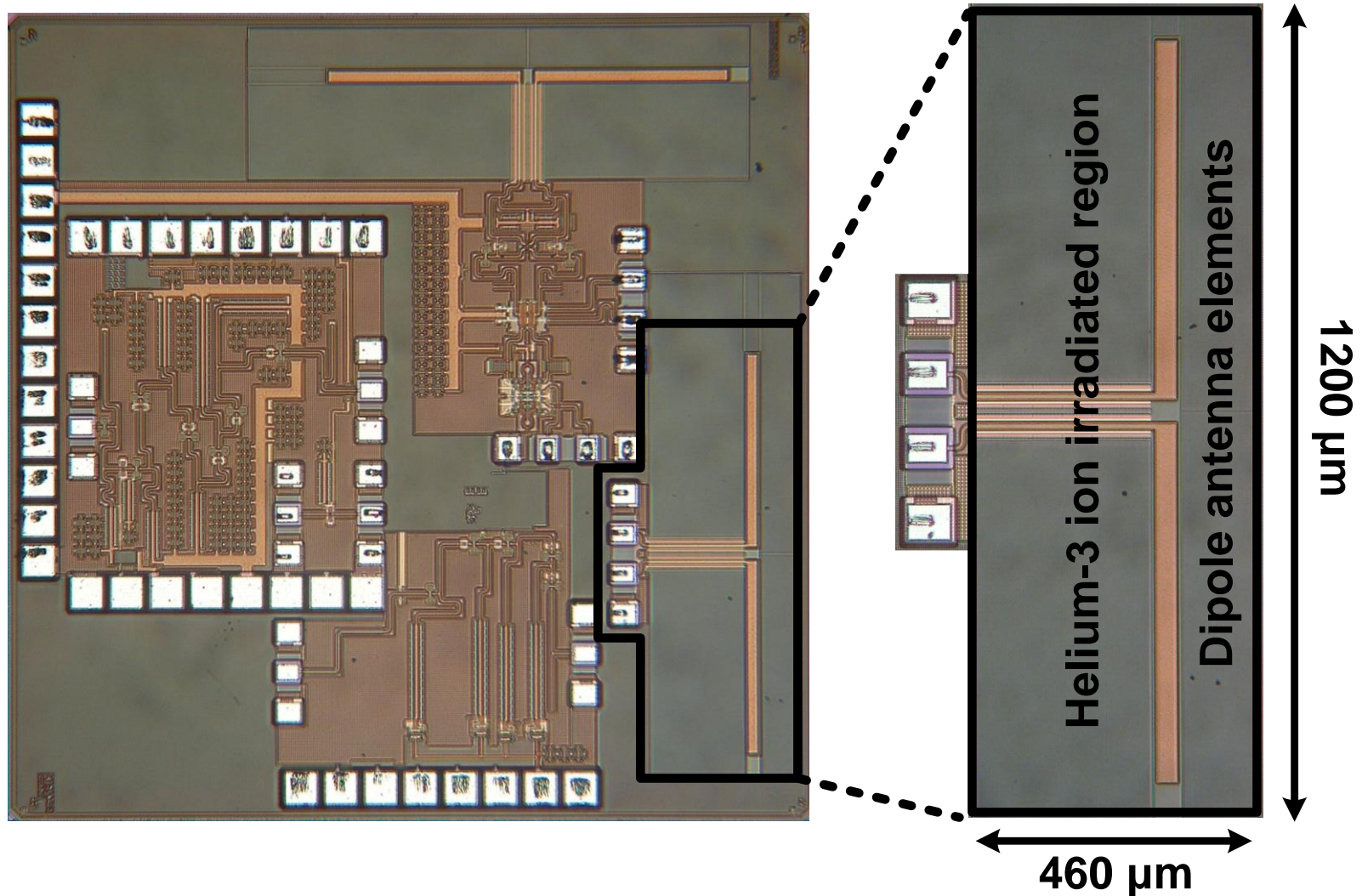


# On-Chip Antenna Configuration

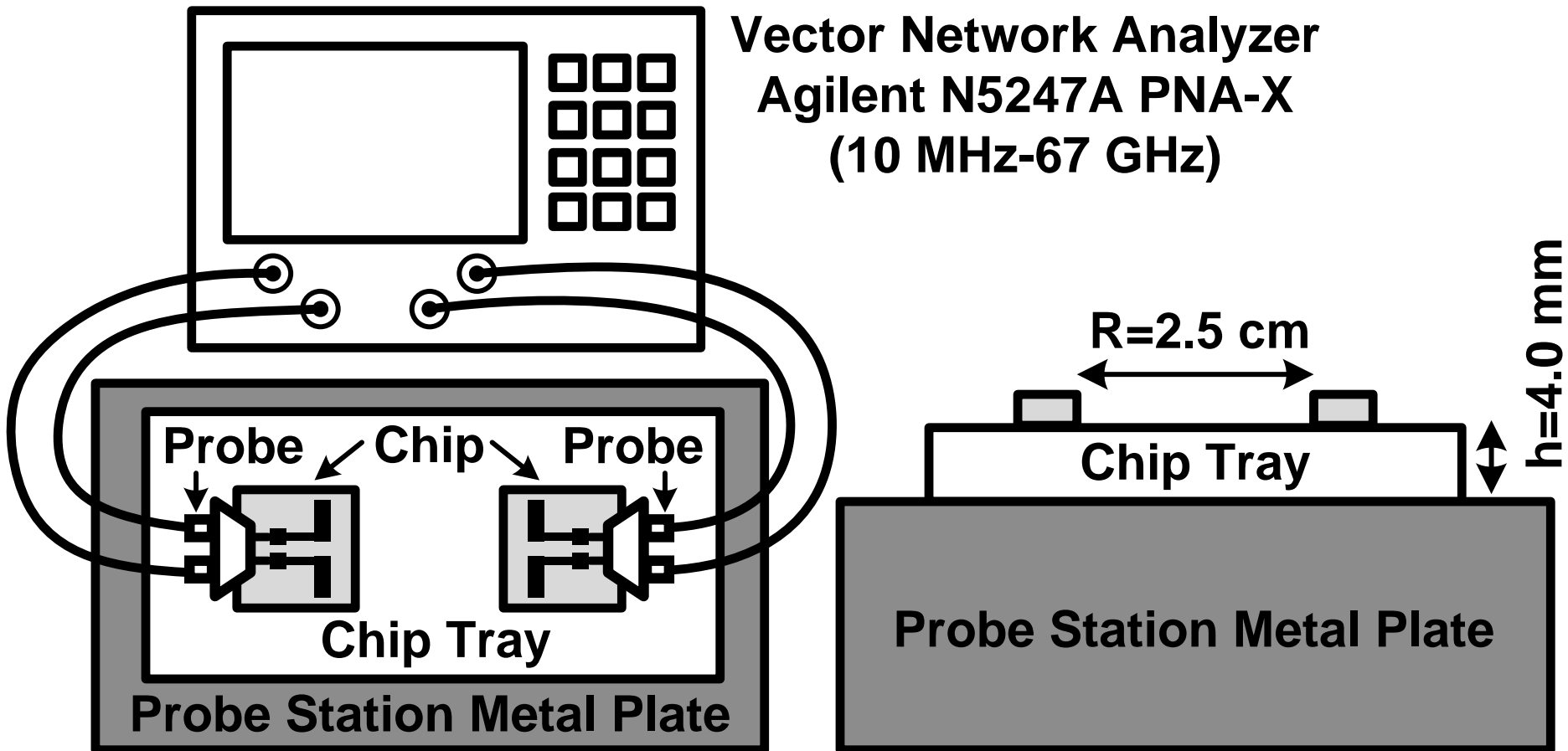


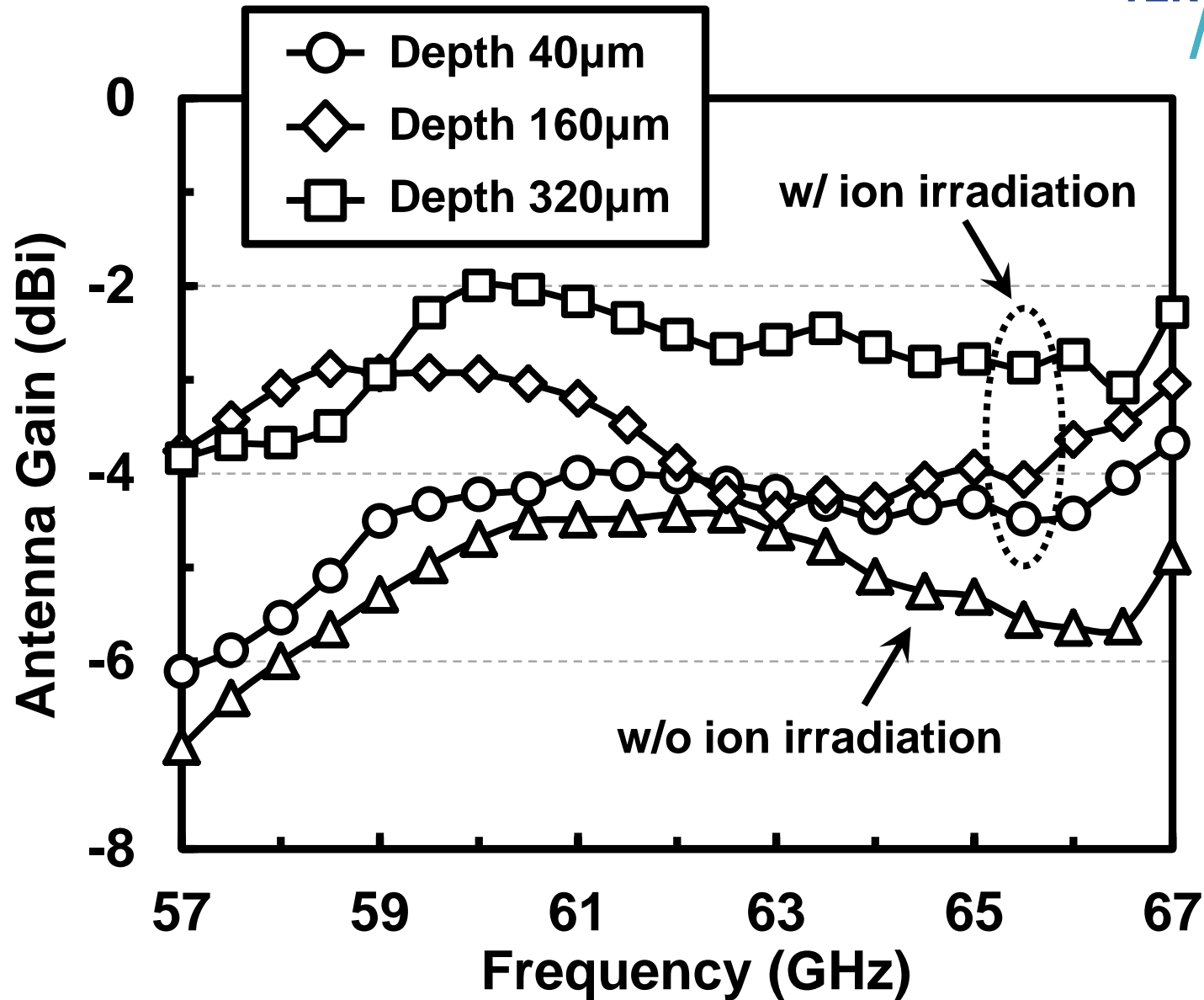
# Die Micro-photograph

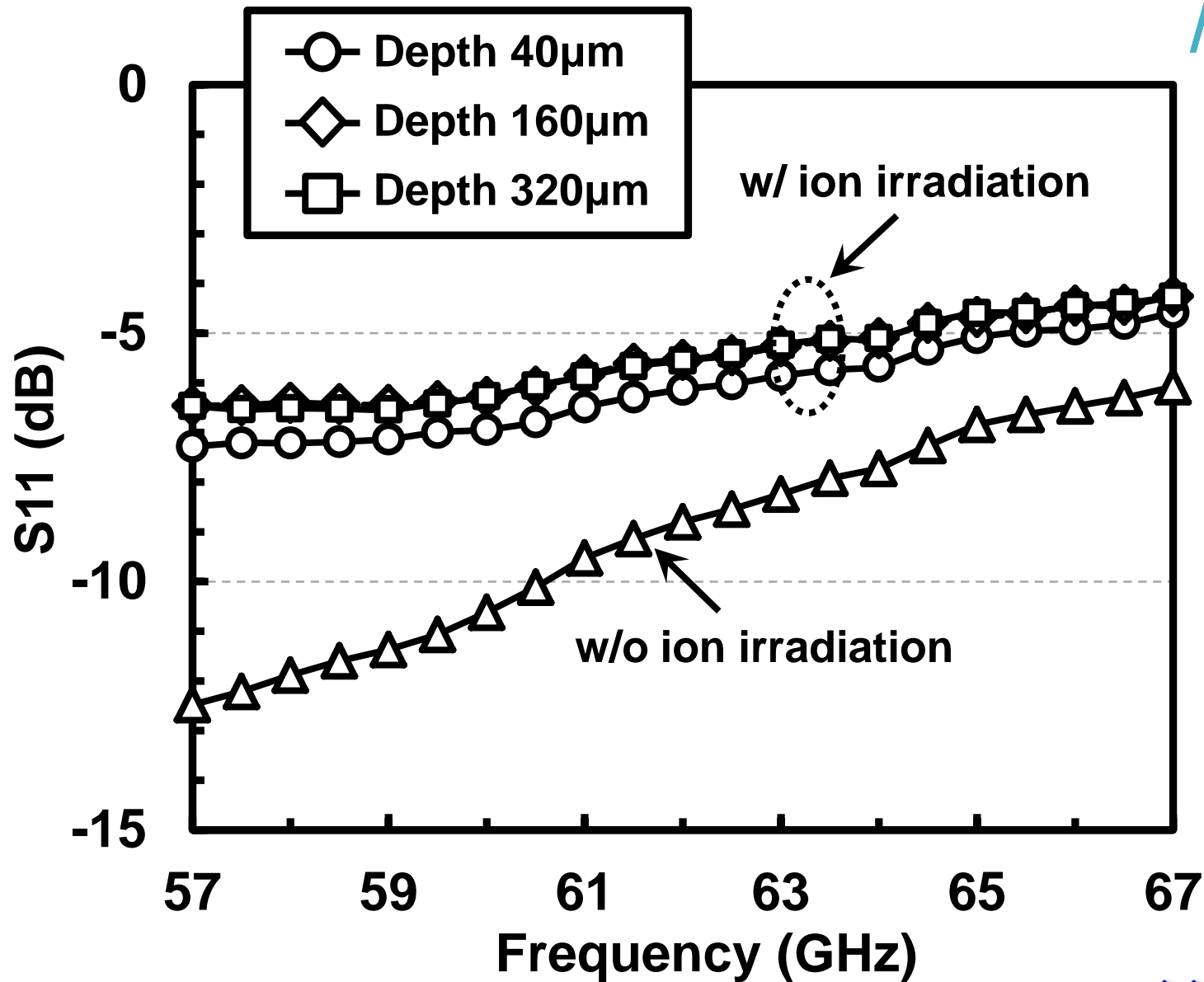
65 nm CMOS technology



Vector Network Analyzer  
Agilent N5247A PNA-X  
(10 MHz-67 GHz)







# Performance Comparison

Ref.	CMOS Process	Type of on-chip antenna	Freq.	Antenna gain	Core area
This work	65 nm	Dipole with helium-3 ion irradiation	60 GHz	-2.0 dBi	0.48 mm <sup>2</sup>
[1]	180 nm	Circularly polarized with AMC	65 GHz	-4.4 dBi	3.24 mm <sup>2</sup>
[5]	180 nm	Yagi	60 GHz	-10.0 dBi	0.74 mm <sup>2*</sup>
[6]	90 nm	Yagi with AMC	60 GHz	-7.2 dBi	1.04 mm <sup>2</sup>
[7]	65 nm	Slot loop	60 GHz	-5.0 dBi*	0.64 mm <sup>2*</sup>
[8]	Post-back-end-of-line (10 Ω•cm)	Inverted-F	61 GHz	-19.0 dBi	0.20 mm <sup>2*</sup>
		Quasi-Yagi	65 GHz	-12.5 dBi	0.59 mm <sup>2*</sup>

\*Estimated from literature

[5] H.-R. Chuang *et al.*, ITED 2011

[7] L. Kong *et al.*, ISSCC 2013

[1] X.-Y. Bao *et al.*, ITAP 2012

[6] H.-C. Kuo *et al.*, ITMTT 2013

[8] Y.-P. Zhang *et al.*, ITED 2005



- **60-GHz on-chip dipole antenna with helium-3 ion implantation technique**
- **Small dose amount ( $3 \times 10^{13} \text{ cm}^{-2}$ )**
- **Average 3-dB gain improvement across 57 GHz~67 GHz**
- **Peak gain of -2.0 dBi @ 60 GHz with  $0.48 \text{ mm}^2$  area**

**Thank you very much for your attention**

**Q & A**