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# High-Q Inductor Modeling on Locally Semi-Insulated Si CMOS Substrate by Helium-3 Bombardment

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2014/12/5

### Outline

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#### Background

- Motivation
- Conventional methods to improve inductor quality factor
- Helium-3 bombardment
- Simulation and experimental results
- Inductor modeling
- Conclusions



# Background

- CMOS on-chip inductors are indispensable for RF circuits.
   > High integration
   > No need for 50-Ω interface
   > VCOs, LNAs, PAs, etc
- RF circuits suffer from the poor performance.
  - ≻Thin metal line
  - >Low substrate resistivity less than  $10\Omega$ ·cm
  - ➢Q is around ten for on-chip inductor.



#### Inductor Loss Mechanisms

- Losses by currents in metal coil
  - Ohmic loss, skin effect, proximity effect
  - Improved by using thick metal

#### Substrate loss

Eddy currents in substrate

$$Q(\omega) \cong \frac{\omega L}{R}$$

- Q: quality factor ω: frequency in radius
- L: inductance
- R: parasitic resistance

Ref.: Bunch, IEEE Microwave magazine June 2002.



# Improve quality factor of on-chip inductors by decreasing silicon substrate loss

# Ensure circuits working well No damage on active devices



#### **Conventional Methods to Improve Q**

### Post-passivation interconnect (PPI)

#### Proton bombardment



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#### Conv. Meth. to Improve Q (Cont'd)

Post-passivation interconnect (PPI)

- > limited to wafer level packaging (WLP)
- > Large parasitic from the high aspect ratio via (HAR vi)



Ref.: [1], C. C. Liu et al., IEDM 323, 2012. [2], G. J. Carchon, et al., MTT 2004



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Ref.: [1], L. S. Lee, et al., TED 2001. [2] D. D. Tang, et al, IEDM 2003.



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# Why Helium-3?

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Method	Reliability	Cost	Q improvement
Thick metal <sup>[1]</sup>	Good	Fair	Good (thickness limitation)
<b>PPI</b> <sup>[2]</sup>	Good	High	Good (Package limitation)
Silicon on Insulator <sup>[3]</sup>	Good	Very High	Fair(failed in high freq.)
Proton <sup>[4]</sup>	Poor	High	Good
Helium-3 (This work)	Good	Fair	Good

#### **Compared to Proton, Helium-3**

- higher vacancies generation ability
- higher irradiation efficiency
- high throughput
- less lateral scattering
- Iess dose
- less process cost

Ref.: [1], J. R. long, et al., JSSC 1997. [2], C. C. Liu, et al., IEDM 2012. [3], J. H. Kim, et al., RFIC 2003. [4], L. S. Lee, et al., TED 2001.



#### Helium-3 Bombardment

# Improving substrate resistivity 500-μm AI mask is used to protect active devices.



Matsuzawa & Okada Lab.

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#### Helium-3 Bombardment (Cont'd)

#### イオン照射手順及びウエハ搬送設備



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generation per ion at the same flight distance in silicon

Larger vacancy

- Vacancies/ion of Helium-3 is more than 5~6 times larger than that of proton
- 300 <sup>3</sup>He<sup>2+</sup> 'acancies/lon 250 (This work) 200 150 100 Proton 50 0 200 300 400 500 0 100 Flight Distance in Si [ µm]

Calculated by Transport of ions in matter (TRIM) of a software named Stopping and Range of Ion in Matter (SRIM)

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# Vacancy Generation per Ion

#### Resistivity

#### Small dose

> For  $R_{sub}$ >1k $\Omega$ , about 10<sup>13</sup>cm<sup>-2</sup>

#### Iower cost

> 10<sup>13</sup>-cm<sup>-2</sup> dose needs only 3.7min



CZ-N wafer Boron dopant 1x10<sup>15</sup> atms/cm<sup>3</sup>

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Ref.: L. S. Lee, et al., TED, 2001

#### Substrate Resistivity Profile

- Spreading resistance profiler (SRP) method
- Larger dose, higher substrate resistivity
- Peaks are correspond to implantation times and depth.
- About 10<sup>13</sup>cm<sup>-2</sup> dosing twice realizes a 30-µm high resistivity region above 1kΩ. (red line)



Cond	Total time [s]	Target irradiation depth [µm]	Total dose [cm <sup>-2</sup> ]
#1	444	15, 30	2.0 x10 <sup>13</sup>
#2	332	15, 30, 45	1.5 x10 <sup>13</sup>
#3	66	15, 30, 45	3.0 x10 <sup>12</sup>



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# Inductor EM Simulation

- 2-nH inductor
- Two-port
- Open de-embedding
- the 100-µm depth Helium-3 bombardment region
- Above 1-kΩ-cm substrate resistivity



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#### **Inductor EM Simulation Results**

### Specific absorption rate (SAR)

[x10<sup>5</sup> W/kg]

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(b) w/ ion implantation



#### Inductor EM Simulation Results (Cont'd) 18

# Q<sub>peak</sub> improved by 23% from 13.5 (without / bombardment) to 16.1 (with bombardment).





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#### **Inductor Implementation**

- 180-nm CMOS process
- 6 metal layers
- Open de-embedding



#### Chip photo



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#### Chip and mask



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#### Inductor Implementation Results

Q improvement ratios (IR) are 54% for 1-nH inductor.
 Peak shifts to higher frequency while self-resonance frequency does not change.





#### Inductor Implementation Results (Cont'd) 21

# Inductance only has slight change.





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#### Inductor Model

- Standard equivalent circuit for easily modeling
- S-parameter fitting



#### Inductor Model (Cont'd)

#### Good match for Q is realized.





#### Inductor Model (Cont'd)

# Good match for inductance is realized.



Solid lines: model Dash lines: meas.

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#### **Extracted Parameters**

Substrate resistances ( $R_{sub1}$ ,  $R_{sub2}$  and  $R_{sub3}$ ) are adjusted for characterizing the quality factor difference.

Parameter	Without He bombardment	With He bombardment	
<i>L</i> <sub>1</sub> , <i>L</i> <sub>2</sub> [nH]	2.87		
$R_1, R_2 [\Omega]$	4.19		
<i>L</i> <sub>1</sub> , <i>L</i> <sub>2</sub> [nH]	0.56		
$R_1, R_2 [\Omega]$	4.73		
<i>C</i> <sub>12</sub> [fF]	36.40		
<i>C</i> <sub>ox1</sub> [fF]	23.40		
<i>C</i> <sub>ox2</sub> [fF]	24.10		
<i>C</i> <sub>ox3</sub> [fF]	47.50		
$R_{sub1} [\Omega]$	1.00 x 10 <sup>3</sup>	7.60 x 10 <sup>3</sup>	
$R_{sub2} [\Omega]$	3.04 x 10 <sup>3</sup>	16.50 x 10 <sup>3</sup>	
<i>R</i> <sub>sub3</sub> [Ω]	0.75 x 10 <sup>3</sup>	5.21 x 10 <sup>3</sup>	
C <sub>sub1</sub> [fF]	5.00		
<i>C</i> <sub>sub2</sub> [fF]	2.12		
<i>C</i> <sub>sub3</sub> [fF]	7.12		



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#### Conclusions

- Helium-3 bombardment is proposed to create a local semi-insulated substrate of high resistibility.
- Required dose is about 1.0x10<sup>13</sup>cm<sup>-2</sup>, 100 times smaller than the conventional proton bombardment
- **Q** can be improved by 58% for a 1-nH Inductor.
- Accurate models are realized.



#### This work was partially supported by MIC, SCOPE, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.





# Thank you for your attention

