A Swing-Enhanced Current-Reuse Class-C VCO with Dynamic Bias Control Circuits

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Abstract – A swing-enhanced current-reuse class-C VCO which can theoretically achieve same phase noise figure-of-merit (FoM) as other class-C VCOs at the lowest power consumption is presented. A swing enhancement in class-C operation and an oscillation robustness are achieved through dynamic bias control circuits for both NMOS and PMOS transistors. The proposed VCO has been fabricated in 180nm CMOS process while oscillating at 4.6 GHz. The measured phase noise is -119 dBc/Hz at 1 MHz offset while consuming 1.6 mA from 1.5 V supply. An FoM of -189 dBc/Hz is achieved.

I. Introduction

Recently, a rapid growth of personal wireless communication has driven the demands for low-cost low-power wireless transceivers. To perform a reliable communication of a low-power system, a design of low-power and low-phase-noise VCOs has attracted great attentions from both industry and academia.

Due to phase noise performance superiority, LC-based VCOs are usually chosen over ring-based oscillators. For a classical LC-tank oscillators, NMOS and CMOS VCOs are standard choices for RF circuit design. As shown in Fig. 1, even though CMOS VCO shares the same maximum phase noise FoM comparing to an NMOS counterpart, it can achieve 6 dB better FoM with the same power budget and LC tank while operating in current-limited regime. Moreover, its oscillation swing is within the supply rail which help alleviates reliability issue. To achieve similar performance at lower power consumption, a current-reuse VCO consumes only half power that of CMOS VCO [1]. However, in order to avoid asymmetrical waveforms, additional components are required to operate both transistors in current-limited region at expense of a swing headroom. To further improve performance, Class-C VCOs which have higher DC-RF current conversion efficiency can provide a theoretical 3.9dB lower FoM comparing to conventional Class-B VCOs [2]. Similar to conventional class of VCOs, a class-C CMOS VCO can provide 6dB better phase noise compared to class-C NMOS VCO when operating in the current-limited region. In this work, a current-reuse class-C VCO which has a same theoretical FoM comparing to NMOS and CMOS class-C VCOs [2]-[3] while consuming the lowest power consumption is proposed as shown in Fig.1.

II. Circuit Design and Implementation

For a conventional Class-C VCO based on NMOS topology, there exists a tradeoff for larger oscillation swing and robustness in oscillation startup. An approach to overcome this issue is to provide an adaptive gate bias for NMOS transistors to be higher at initial state and lower at the stead state [4]-[5]. In order to further improve power efficiency, a lower-power current-reuse class-C VCO [6] is proposed with a dynamic biasing for both NMOS and PMOS transistors to provide a robustness in oscillation at the initial state and provide high oscillation swing at the steady state.

The detail schematic of the proposed swing-enhanced current-reuse class-C VCO using dynamic bias control circuits is depicted in Fig.2. It is composed of three main components, *i.e.,* a core VCO and dynamic bias circuits for NMOS and PMOS transistors. The core VCO is composed of only one pair of cross-coupled PMOS and NMOS transistors. The dynamic bias control circuits are composed of two modified current mirrors as shown in Fig.2.

If the current-reuse VCO enters voltage-limited region, the outputs will have asymmetric waveforms. Moreover, the conduction angle of devices increases and the drain current shapes are widened which loses its high DC-to-RF current conversion efficiency [2]. To avoid such issue, both NMOS and PMOS transistors should remain in active region. By assuming the same common voltage, the maximum oscillation amplitude is limited by the difference between steady state bias of gate bias and threshold voltage of PMOS and NMOS transistors [6]. To ensure its oscillation start-up, higher and lower gate biases for NMOS and PMOS, respectively, are necessary. Once the steady oscillation has been built, $V_{g,p}$ and $V_{g,n}$ can adaptively change its value to become higher and lower, respectively, which in turns, maximizing oscillation swing at the steady state. The circuit operation can be described as follows. From Fig. 3 and 4, before VCO starts to oscillate, initial gate biases of NMOS and PMOS transistors are determined by $I_{REF,n}$ and $I_{REF,p}$. Once the current in the core oscillator provides enough transconductance to meet the oscillation condition, output voltage starts to swing across V_{CM}. Then, the adaptive bias scheme acts like a negative feedback which senses an oscillation swing and adaptively changes gate biases of both transistors to enhance its maximum swing in a current-limited regime at the steady state.

From simulation, under a 1.5-V supply, at the initial state, gate biases of NMOS and PMOS are 0.6V and 0.8V, respectively, from 68μA of reference current. At the steady state, the gate biases of NMOS and PMOS adaptively change to 0.25V and 1.05V, respectively, as shown in Fig.4. This results to a swing enhancement at steady state. Moreover, the proposed VCO can maintain balanced waveform as shown in Fig.5 and achieve better phase noise performance since both transistors never enter deep triode region.

III. Measurement Results

The proposed circuit is fabricated in a 180-nm CMOS process. The die micrograph is shown in Fig.6. The measured phase noise is given in Fig.7. The measured tuning range is 4.5GHz to 4.6GHz. For 1.5V supply, a phase noise of -119dBc/Hz at 1MHz offset can be achieved while consuming 1.6mA resulting in a figure of merit of -189 dBc/Hz. Table I summarizes the comparison to the state-of-the-art VCOs in current-reuse topologies. The proposed VCO achieves a few dB better than the state-of-the-art CMOS VCO and similar performance comparing to the state-of-the-art current-reuse VCOs.

IV. Conclusion

In this paper, a swing-enhanced current-reuse class-C VCO [6] using dynamic bias control circuits is proposed.

The proposed dynamic bias scheme keeps both transistors in a proper operation for high current efficiency and a balanced tank waveform.

Acknowledgements

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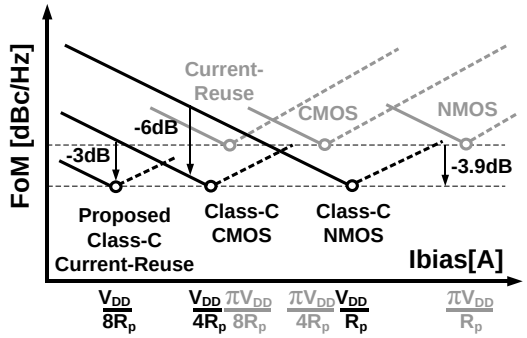


Fig.1. Theoretical FoM limit of conventional class of VCOs and its corresponding Class-C VCOs.

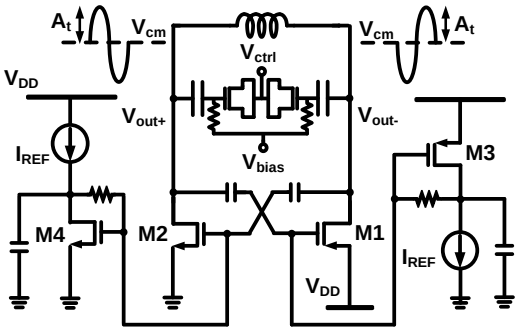


Fig.2. Proposed swing-enhanced current-reuse class-C VCO using dynamic bias control circuits

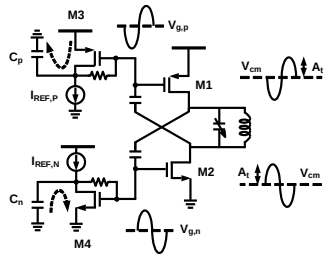


Fig.3. Simplified diagram of the proposed swing-enhanced class-c current reuse VCO to describe its operation.

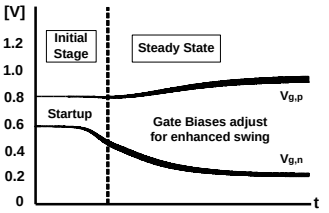
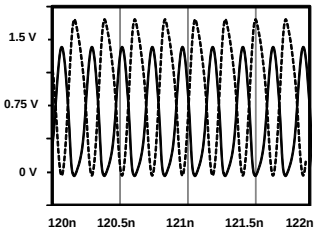
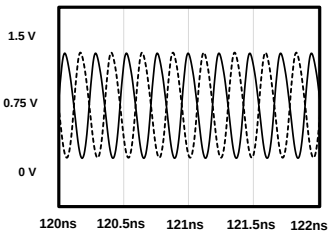


Fig.4. Simulated transient waveforms of dynamic gate bias of PMOS, NMOS.



(a)



(b)

Fig.5 Output amplitude of current-reuse VCO (a) without and (b) with dynamic bias control circuits.

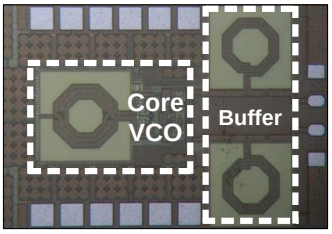


Fig.6. Chip Micrograph

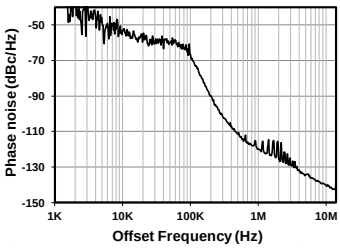


Fig.7. Measured phase noise plot at 4.63GHz

TABLE I COMPARISON WITH THE-STATE-OF-THE-ART VCOS IN A CURRENT-REUSE TOPOLOGY

Ref.	Tech.	VCO Topology	Frequency (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FoM (dBc/Hz)	Additional components for Balanced Amplitude
[7]	65nm	CMOS	3	-114@1MHz offset	0.7	-187	-
[8]	65nm	Current-Reuse	2.1	-126.1@3MHz offset	0.28	-190	-
[9]	180nm	Current-Reuse	16	-111@1MHz offset	8.1	-187	Required
[10]	180nm	Current-Reuse	2.9	-122@1MHz offset	1.7	-188	Required
[1]	180nm	Current-Reuse	2.0	-123@1MHz offset	1	-189	Required
This	180nm	**Class-C Current-Reuse**	4.6	-119 @1MHz offset	2.4	-189	**Not required**