A Dual-loop Injection-locked PLL with All-digital Background Calibration System for On-chip Clock Generation

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Abstract – This paper presents a compact, low power, and low jitter dual-loop injection-locked PLL with synthesizable all-digital background calibration system for clock generation. Implemented in a 65nm CMOS process, this work demonstrates a 0.7-ps RMS jitter at 1.2 GHz while having 0.97-mW power consumption resulting in an FOM of -243dB. It also consumes an area of only 0.022mm^2 resulting in the best performance-area trade-off system presented up-to-date.

I. Introduction

For modern SoC systems, stringent requirements on on-chip clock generators include small-area, low-power consumption, PVT-insensitive, and the lowest possible jitter performance [1-5]. Sub-harmonically injection-locked technique can significantly improve random jitter characteristic of a clock generator. To compensate the free-running frequency shift caused by temperature and voltage variations, this paper [4] proposes the use of a dual-loop topology with one free-running VCO (Replica VCO) placed inside a FLL for tracking temperature and voltage drift. The other VCO (Main VCO) is injection-locked for producing a low-jitter clock, while the free-running frequency shift can be compensated by the replica loop.

II. Proposed IL-PLL with all-digital calibration

Block diagram of the proposed system is given in Fig.1. Aside from the VCO and the 10-bit DAC, all circuits that makeup the FLL are implemented using digital standard cells to have a synthesizable all-digital FLL (AD-FLL) design. Therefore, the proposed work can significantly scale down in area due to the absence of a passive loop filter. The oscillation frequency of replica VCO is measured by a digital counter. This counted number is compared to a predefined frequency control word that maps to the expected number of pulses during one cycle for a certain division ratio. Depending on the sign of the output, the up/down counter adjusts both the main and replica VCO frequency.

Fig.2 shows the detailed calibration algorithm. After the initial frequency calibration of the replica VCO is carried out, the counter connected to the replica VCO is disabled and the multiplexer control lines are set to choose the output of the main VCO counter for calibrating frequency offset. In phase II, an offset is added or subtracted from the main VCO counter to compensate frequency difference between it and the replica VCO that might arise from process variations. By comparing the number of pulse of main VCO to the predefined value and incrementing or decrementing the main VCO counter, the required offset to calibrate any difference in frequency will be added or subtracted. Finally, as both VCOs are having the same frequency, the loop is returned to its initial settings to maintain both VCOs frequency over temperature and voltage variations for robust operation. Schematic of the injection-locked VCO is given in Fig. 3, and both main and replica VCOs share the same topology and layout to minimize mismatches.

III. Measurement Results

The proposed circuit is fabricated in a 65 nm CMOS process. The phase noise before and after performing injection-locking is measured by using a signal source analyzer and is given in Fig.4. This phase noise maps to a 0.7 ps jitter when integrated from 10 kHz to 40 MHz. The proposed dual-loop IL-PLL has an operating range of 0.5-to-1.6 GHz, and it consumes a total power consumption of 0.97 mW excluding output buffer, from a 1 V power supply. The measured reference spur is -57 dBc. The reference clock can be varied from 40 to 300 MHz. All the above-mentioned measurements are performed at the room temperature.

Fig. 5 shows the effect of sweeping the temperature on the measured peak-to-peak and RMS jitter for IL-PLL with and without replica loop, at a carrier of 1.2 GHz. Configured as a conventional IL-PLL without the replica loop, it is observed that the locking point shifts to the edge of the locking range as temperature gradually increases. This causes a significantly deterioration of the peak-to-peak and RMS jitter. On the other hand, it is clearly shown that the proposed IL-PLL with replica loop manages to maintain the locked state and correct frequency over the range from 0 °C to 80 °C, which validates the effectiveness of the IL-PLL with the dual-loop PVT calibration.

Fig .6 gives a comparison between this work and previously published work. The proposed dual-loop IL-PLL achieves comparable performance with the-state-of-the-art, while only occupies 0.022 mm^2 chip area. The figure of merit (FOM) is -243dB at a 1.2 GHz carrier. The proposed circuit realizes a low-jitter and small-area clock generation with a robust operation over different operating conditions. The die micrograph is shown in Fig. 7.

IV. Conclusion

This paper [4] proposes a dual-loop injection-locked PLL with synthesizable all-digital PVT calibration circuits. With carful design, the proposed PLL can be suited for clock generation in wireline and wireless systems.

Acknowledgements

This work was partially supported by STARC, MIC, SCOPE, MEXT, Canon Foundation and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1]A. Elshazly, *et al.*, "A 1.5GHz 890µW digital MDLL with 400fsrms integrated jitter, -55.6dBc reference spur and 20fs/mV supply-noise sensitivity using 1b TDC," *ISSCC Dig. Tech. Papers*, pp. 242-243, Feb. 2012.

[2]B. Helal, *et al.*, "A highly digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve subpicosecond jitter performance," *IEEE J. Solid-State Circuits*, vol.43, no.4, pp. 855-863, Apr. 2008.

[3]G. Xiang, *et al.*, "A 2.2GHz 7.6mW sub-sampling PLL with −126dBc/Hz in-band phase noise and 0.15psrms jitter in 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp.392-393, Feb. 2009.
[4]Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, and Akira Matsuzawa, "A 0.022mm^2 970μW dual-Loop injection-locked PLL with -243 dB FOM using synthesizable all-digital PVT calibration circuits," *ISSCC Dig. Tech. Papers,*pp. 248-249, Feb. 2013.
[5]C. Liang and K. Hsiao, "An Injection-Locked Ring PLL with Self-Aligned Injection Window," *ISSCC Dig. Tech. Papers*, pp. 90-91, Feb. 2011.

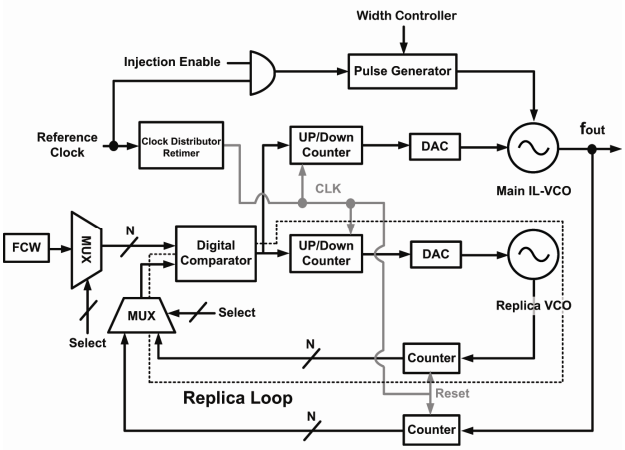

Fig.1. Block diagram of the proposed dual-loop IL-PLL.

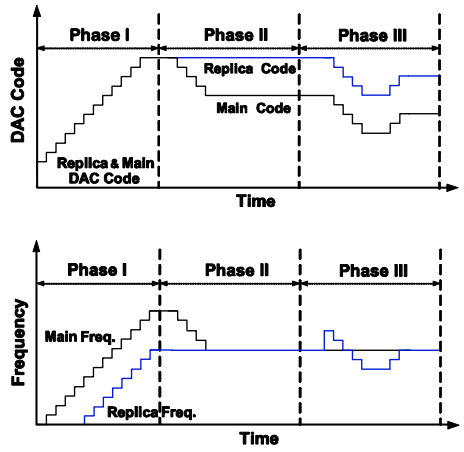

Fig.2. Main and replica DACs output code and output frequency at different calibrations phases.

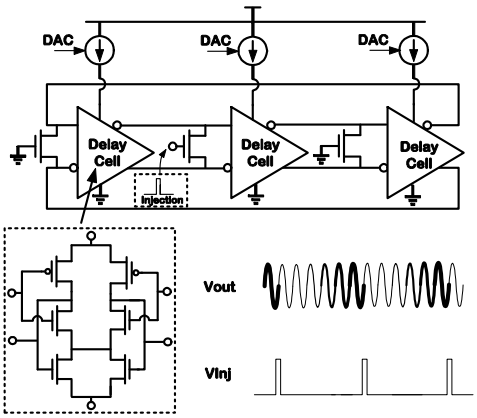

Fig.3. Schematics of the injection-locked ring oscillator.

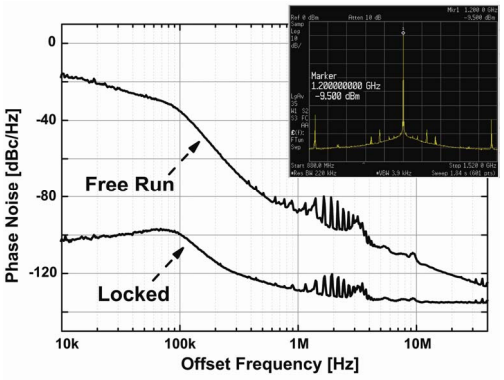

Fig.4. Measured phase noise and spectrum at a carrier of 1.2GHz.

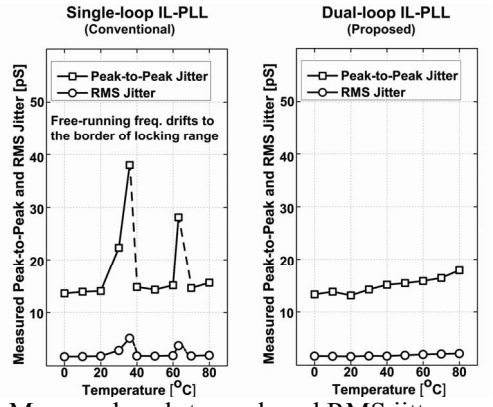

Fig.5. Measured peak-to-peak and RMS jitter against temperature variations.

	This work	[1]		[2]	[5]
	IL-PLL	DMDLL	DPLL	MDLL	IL-PLL
Freq. [GHz]	0.5-1.6	0.8-1.8	0.8-1.8	1.6	0.216
Ref. [MHz]	40-300	375	375	50	27
Power [mW]	0.97	0.89	1.35	12	6.9
Area [mm^2]	0.022	0.25	0.25	0.058	0.03
Integ. Jitter [ps]	0.7	0.4	3.2	0.68	2.4
Jitter RMS/PP [ps]	1.81/19.4 10M hits	0.92/9.2 5M hits	4.2/33 5M hits	0.93/11.1 30M hits	N.A.
Ref. Spur [dBc]	-57	-55.6	-40.5	-58.3	-70.7
FOM [dB]	-243	-248.46	-228.59	-233.76	-225
CMOS Technology	65nm	130nm	130nm	130nm	55nm

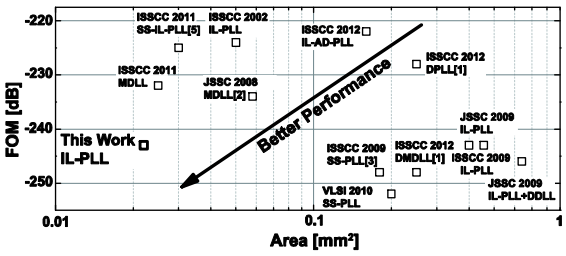

Fig.6. Performance summary and comparison with state-of-the-art prior work.

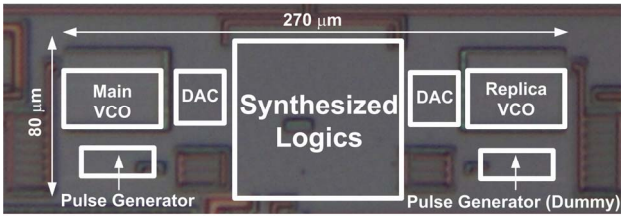

Fig.7. Chip micrograph.