A 60GHz Sub-Sampling PLL Using A Dual-Step-Mixing ILFD

Teerachot Siriburanon, Tomohiro Ueno, Kento Kimura, Satoshi Kondo, Wei Deng, Kenichi Okada, and Akira Matsuzawa

***Tokyo Institute of Technology,* Japan**

Outline

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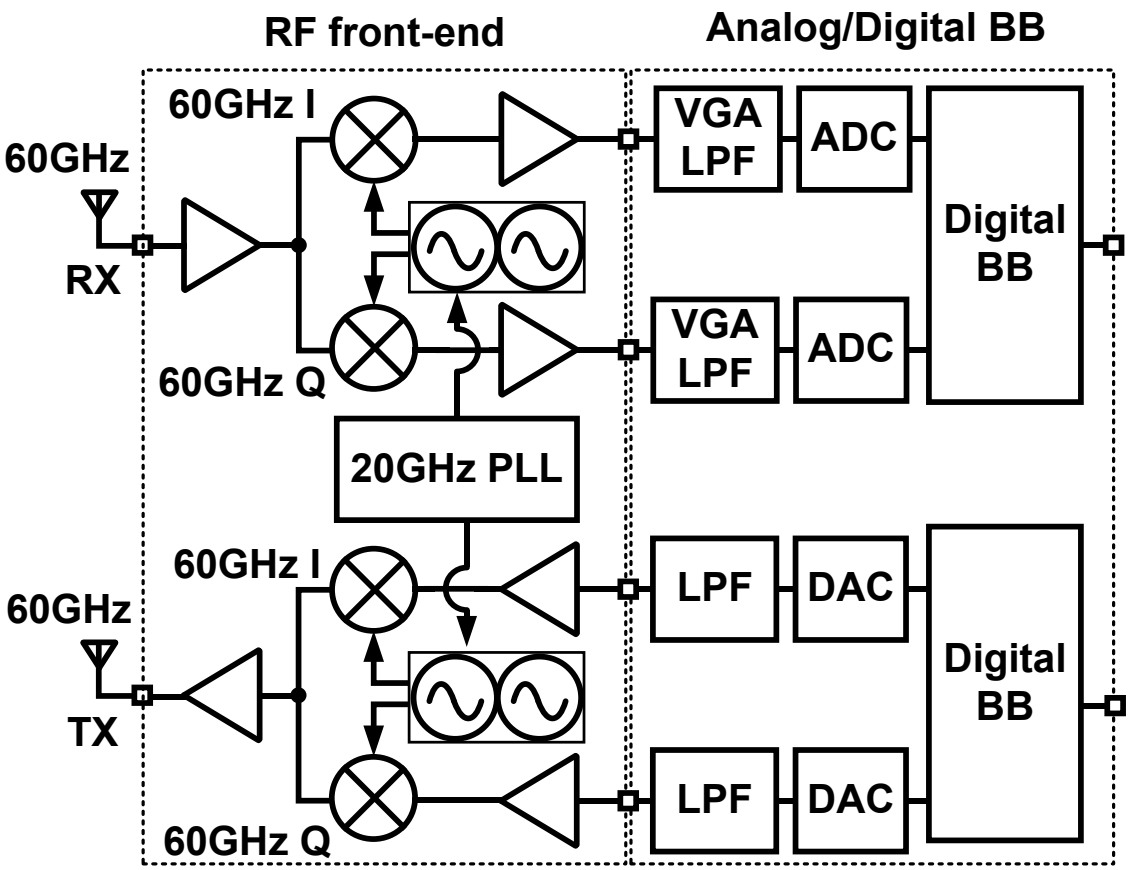
- Background
- Issues and Previous Work
- Proposed 60GHz Frequency Synthesizer
  - System Architecture
  - 20GHz-to-5GHz Dual-Step-Mixing ILFD
- Experimental Results
- Conclusions

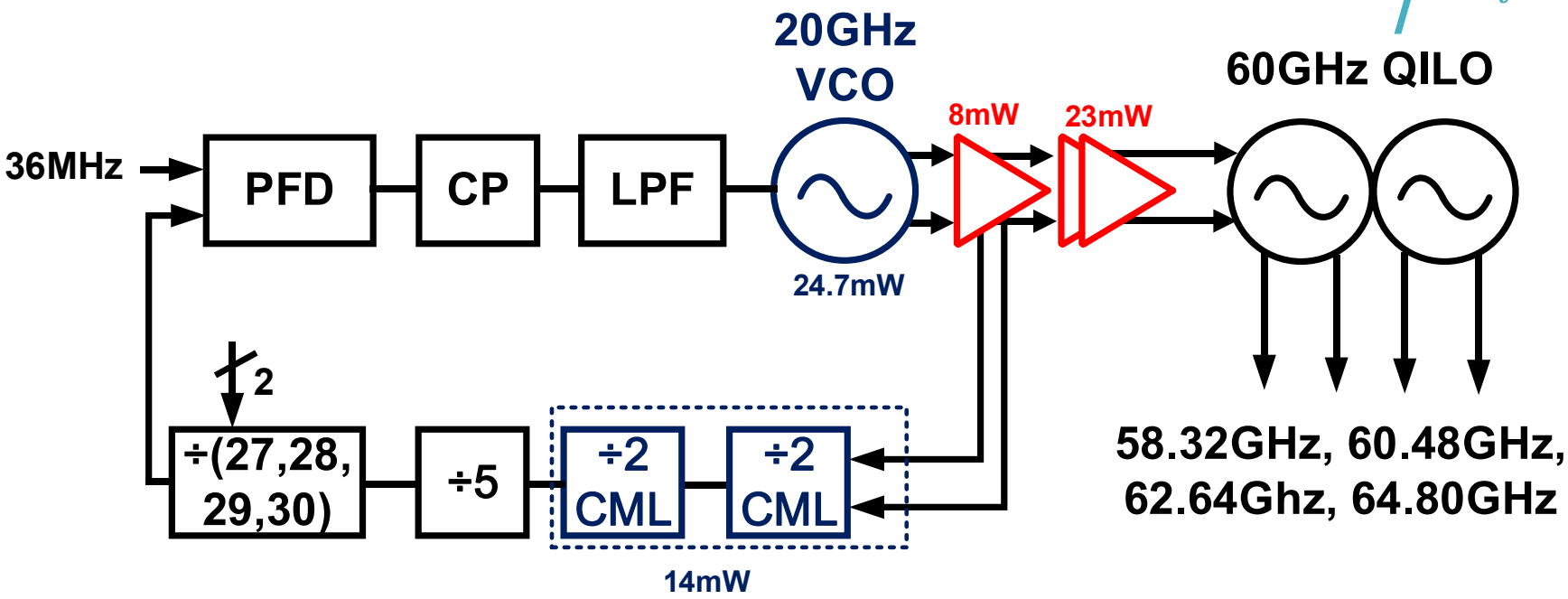
Requirements for 60GHz PLLs



- **Out-of-band phase noise<-90dBc/Hz @1MHz to support 16QAM***
- **In-band phase noise should be lowered depending on the bandwidth of carrier-recovery circuitry****

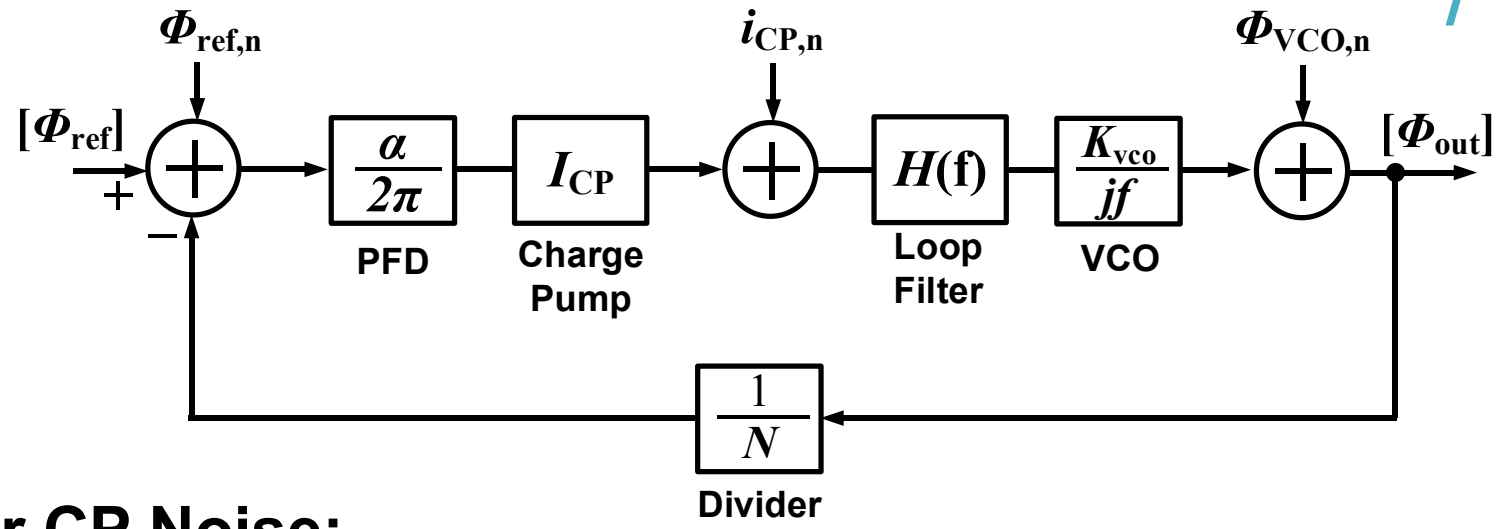
***,** K. Okada, *et al.*, JSSC 2013**

Issues of mm-wave PLLs



- Low out-of-band phase noise by Injection Locking
- -96dBc/Hz at 1MHz at 61.56GHz
- Large power consumption (64mW for 20GHz)
- Does not support channel bonding and all standards
  - Lower REF clk. required to support all standards (N↑)

PLL Noise Transfer Function



For CP Noise;

$$\frac{\Phi_{out}}{i_{CP,n}} = \frac{N}{K_d} \cdot \frac{G(s)}{1+G(s)} \longrightarrow \frac{\Phi_{out}}{i_{CP,n}} = \frac{1}{K_d} \cdot \frac{G(s)}{1+G(s)}$$

(G(s) is open-loop transfer function)

- Divide ratio N is no longer contribute to CP/PFD output noise

→ Useful in a system with large division ratio N

X.Gao, *et al.*, JSSC 2009

Proposed 60GHz Frequency Synthesizer

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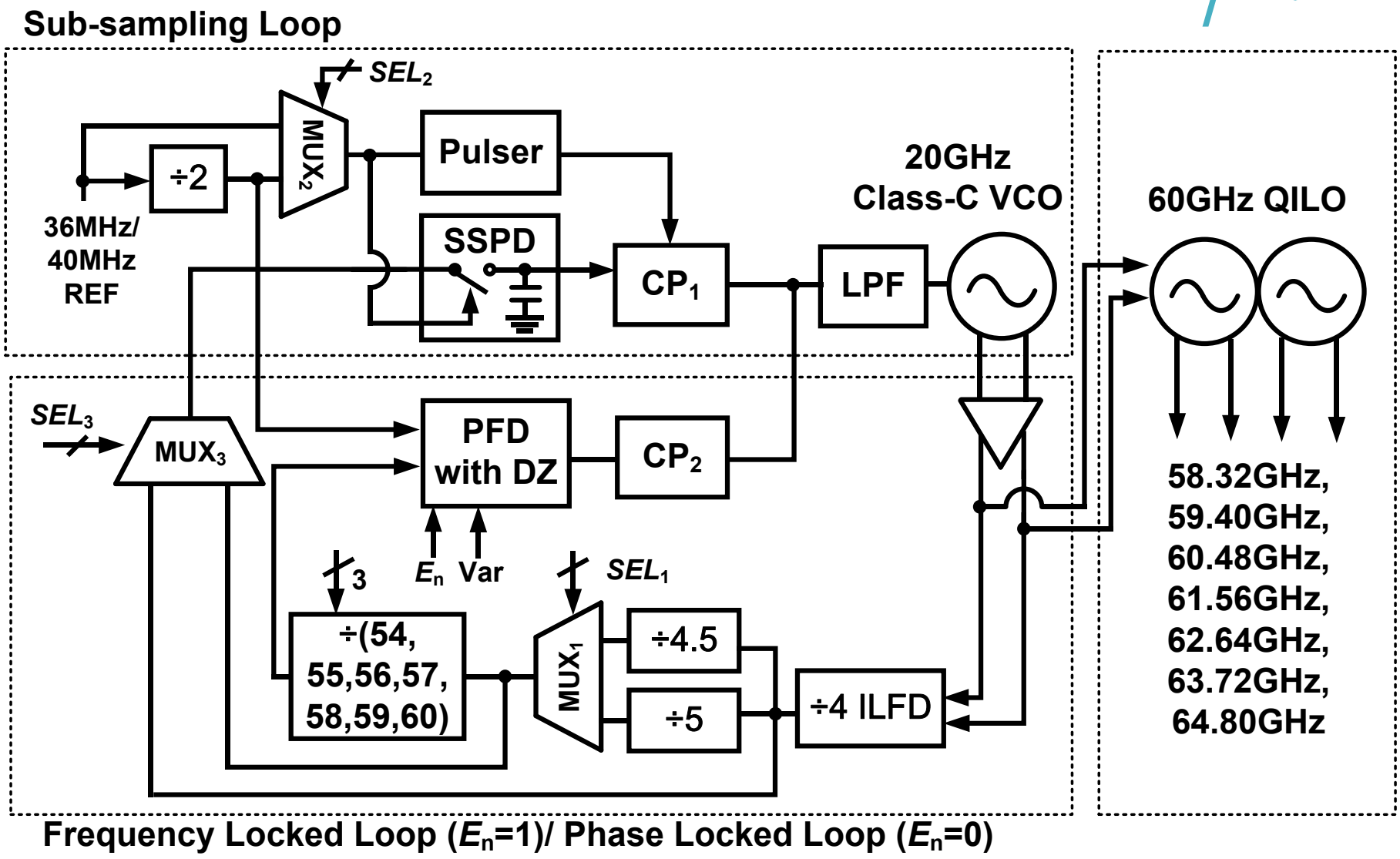
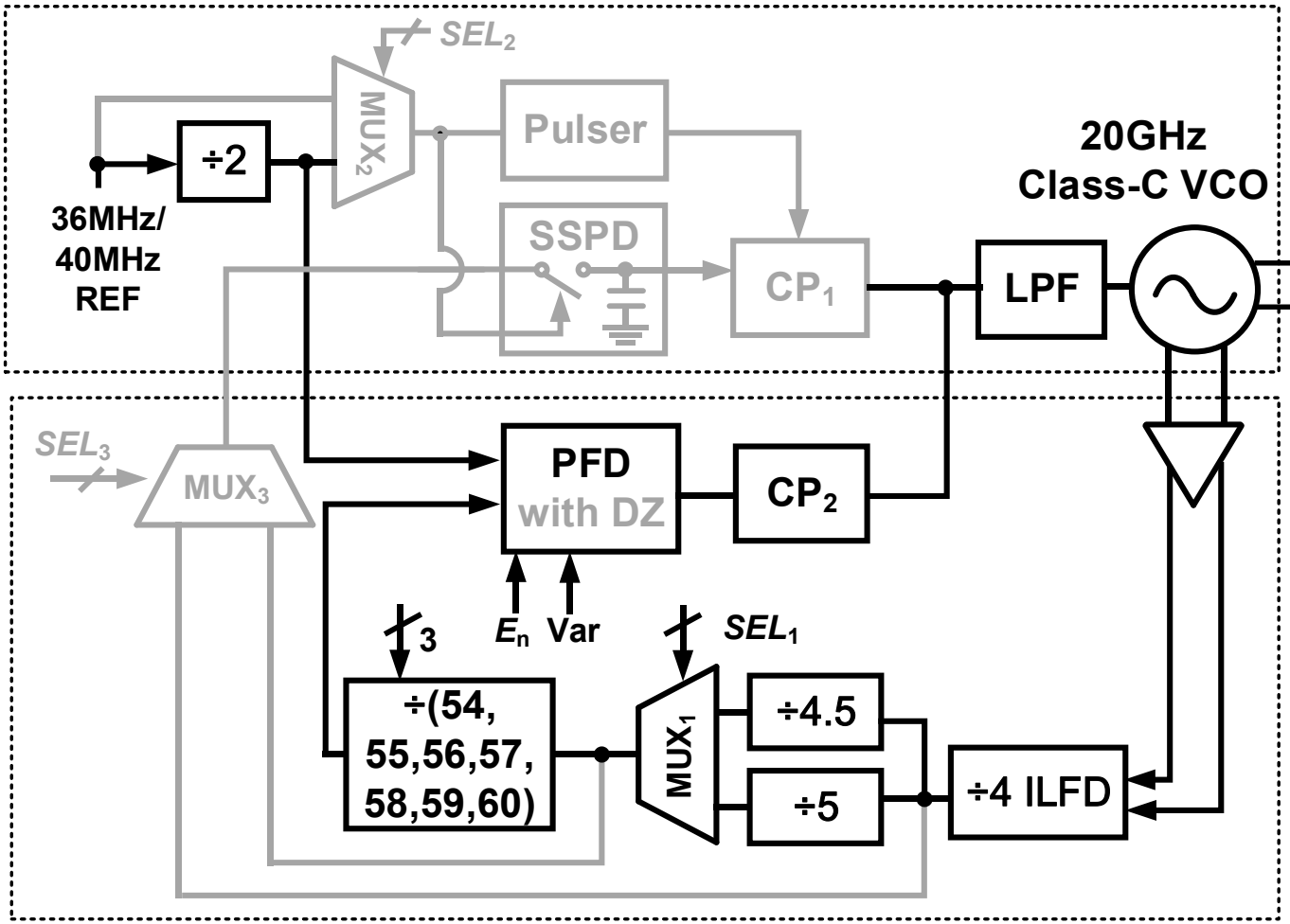


Frequency Locked Loop (E_n=1)/ Phase Locked Loop (E_n=0)

T. Siriburanon, *et. al*, RFIC 2014

Matsuzawa & Okada Lab.

20GHz PFD/CP PLL



Frequency Locked Loop (E_n=1)/ **Phase Locked Loop (E_n=0)**

- **PFD and CP_2 are enabled**

20GHz Sub-sampling PLL

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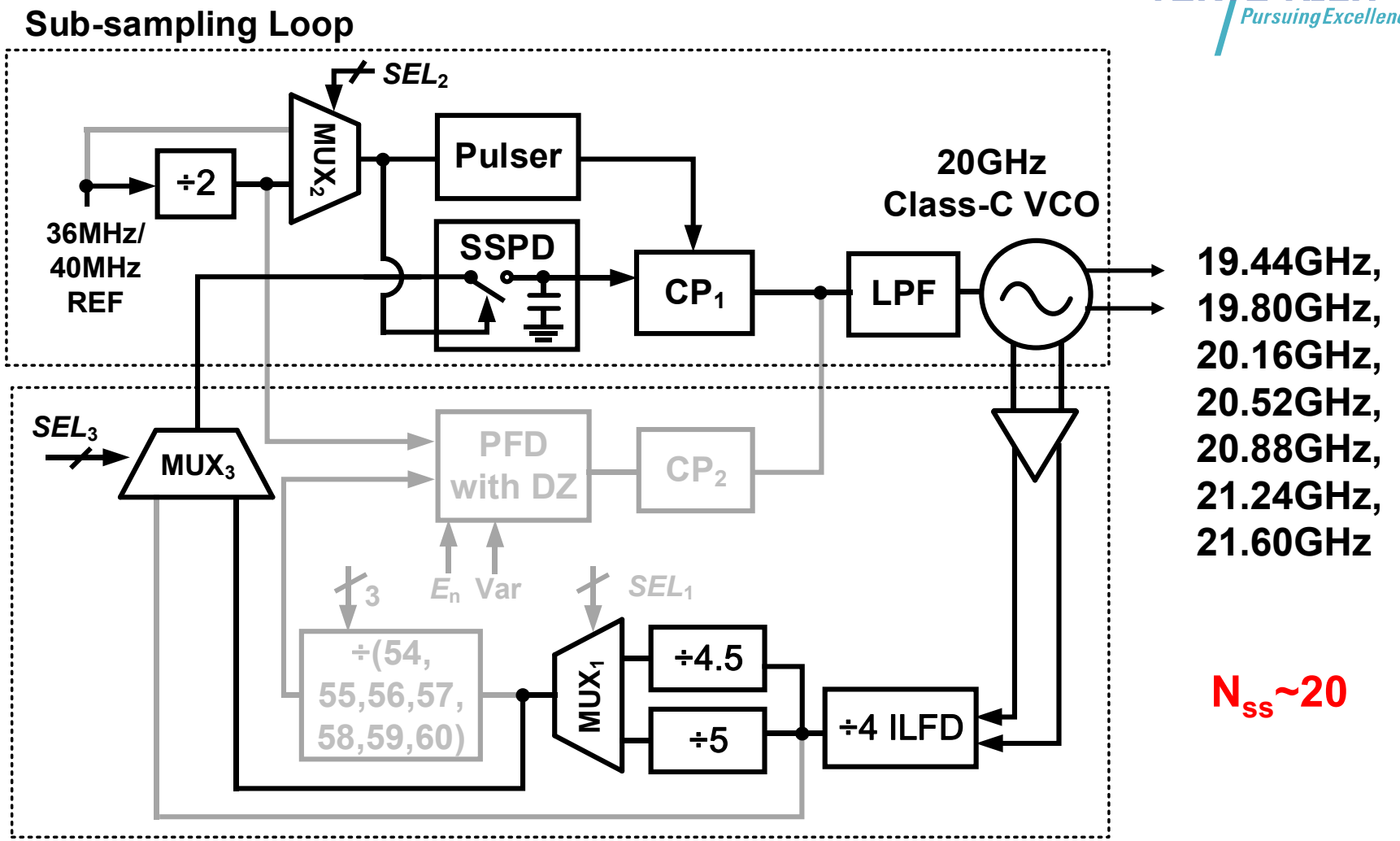

- **Dead zone in PFD, SSPD and CP_1 are enabled**

20GHz SS-PLL Noise Modelling

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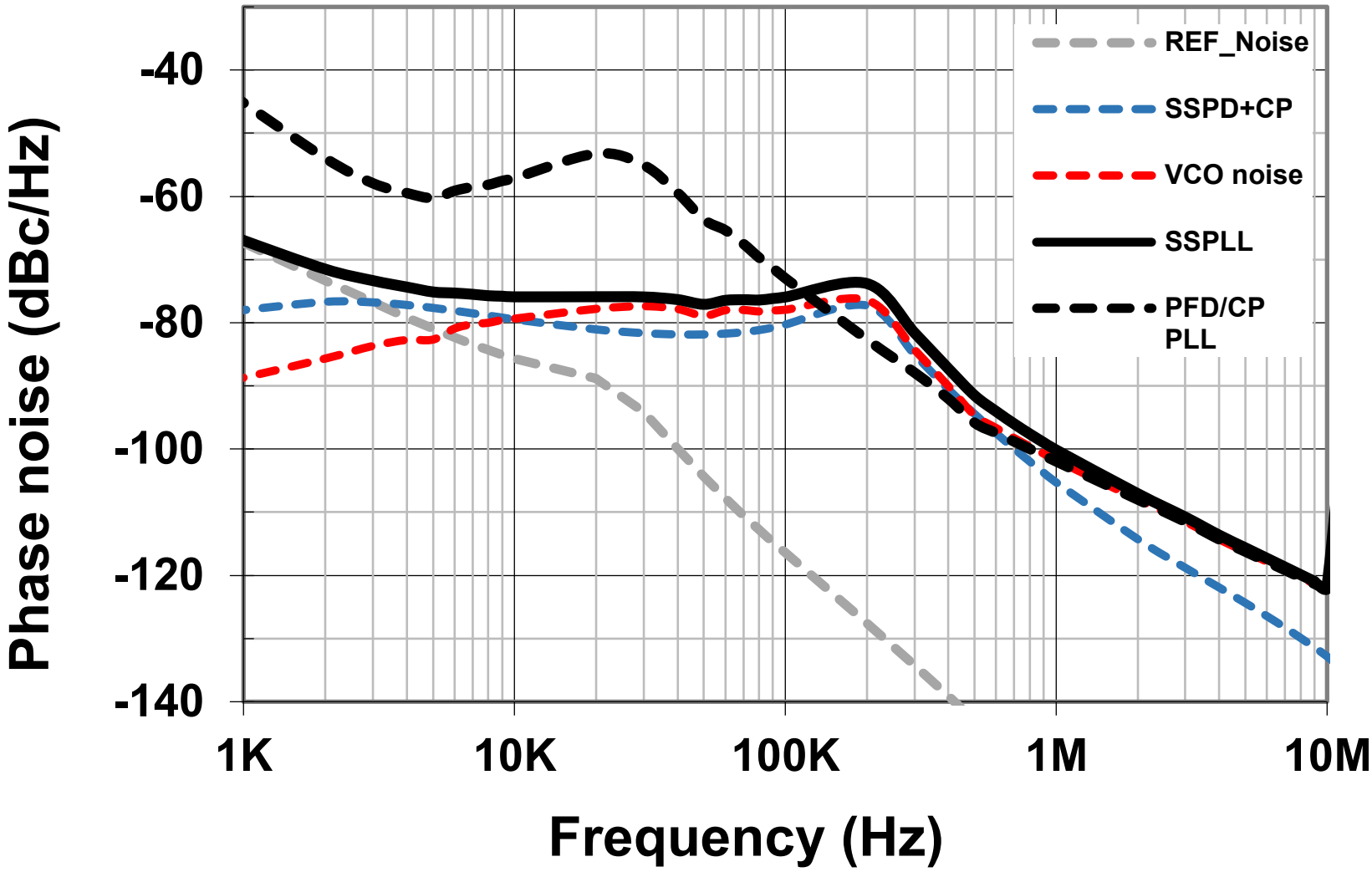

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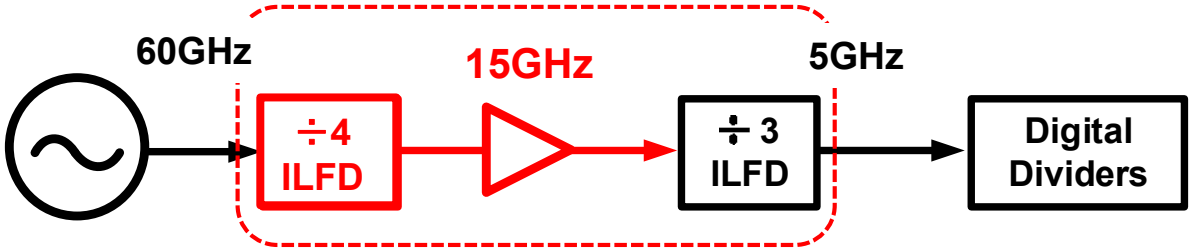
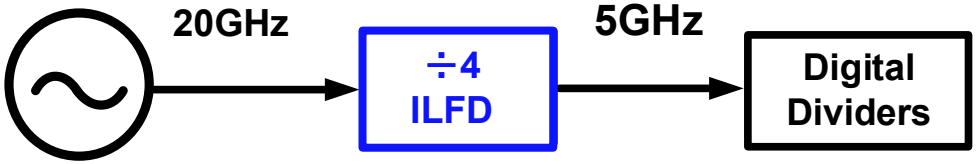
High-speed Divider Chains



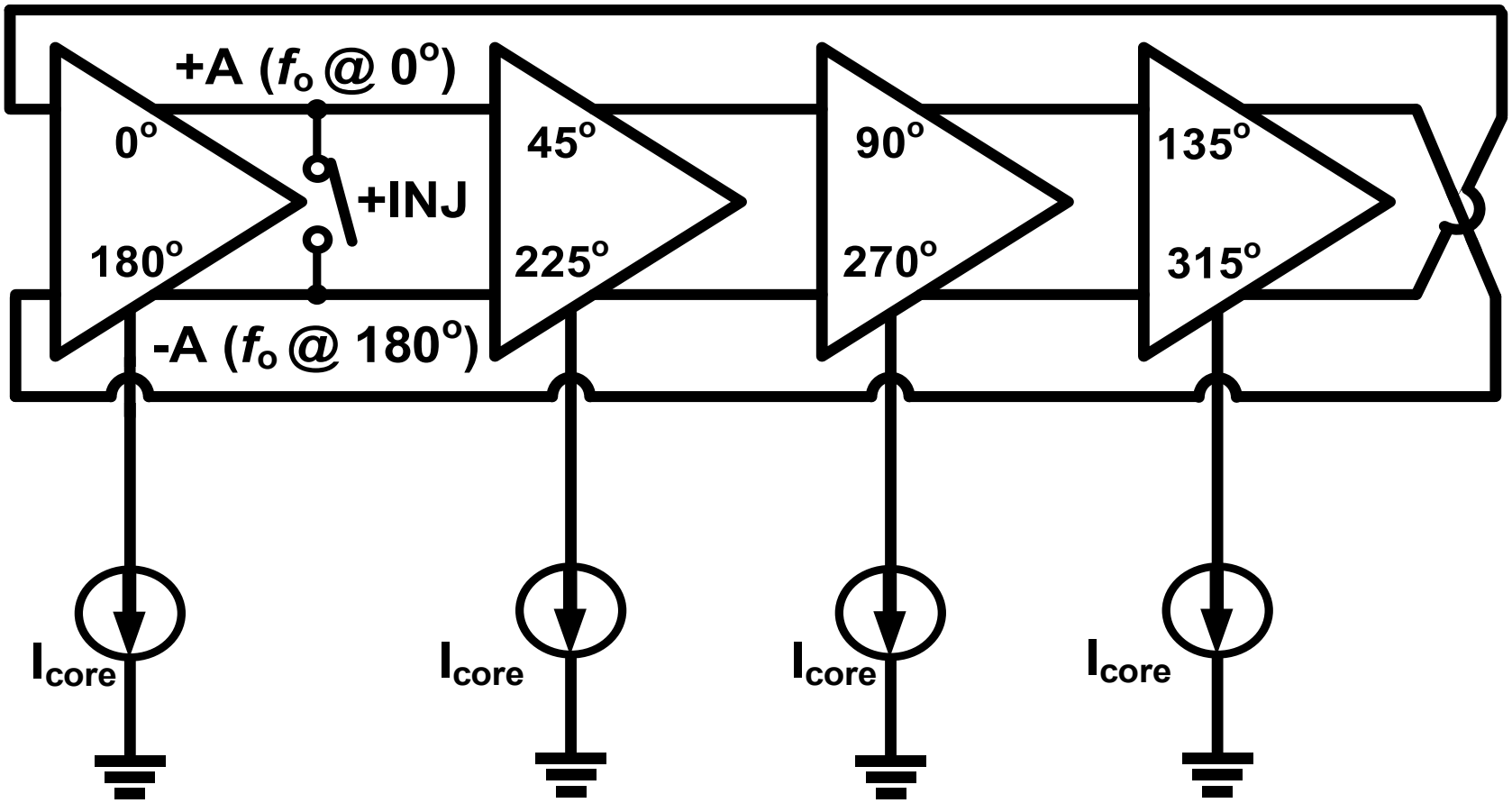
- Large power
- Locking range mismatch



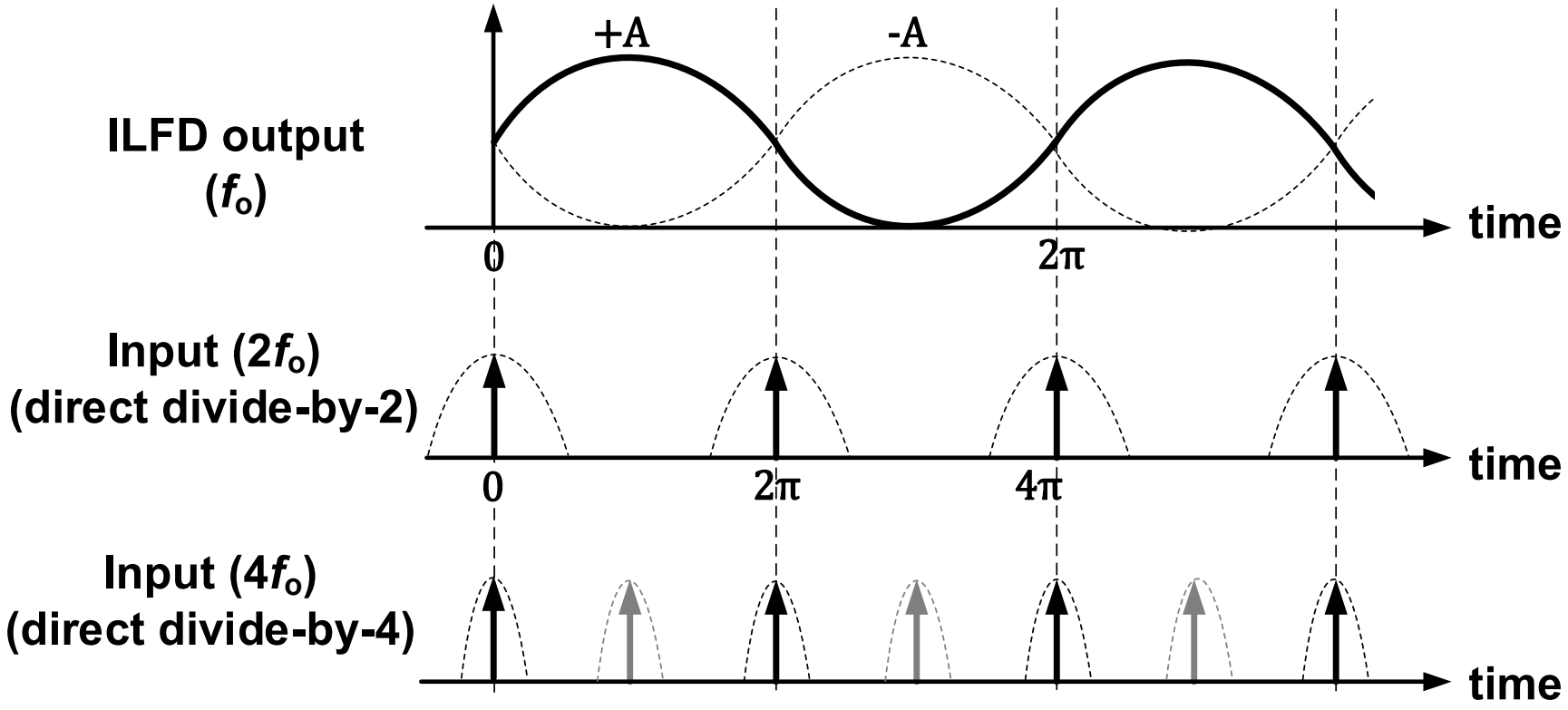
- Narrow locking range

■ A technique to increase locking range of high-order-division in ILFDs is necessary

Conv. Single-Step Injection ILFD



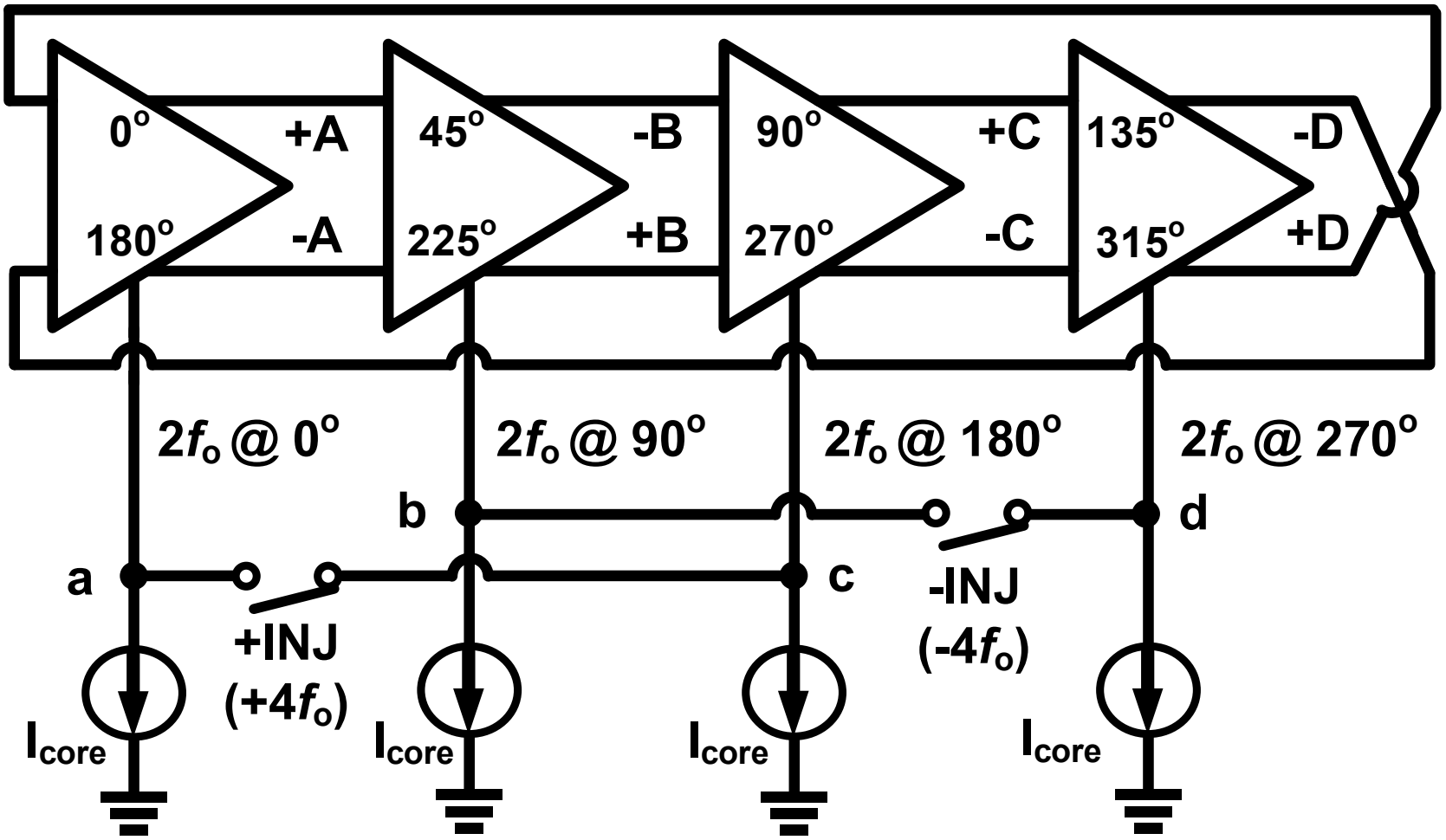
Conv. Single-Step Injection ILFD



Disturbing injection in grey

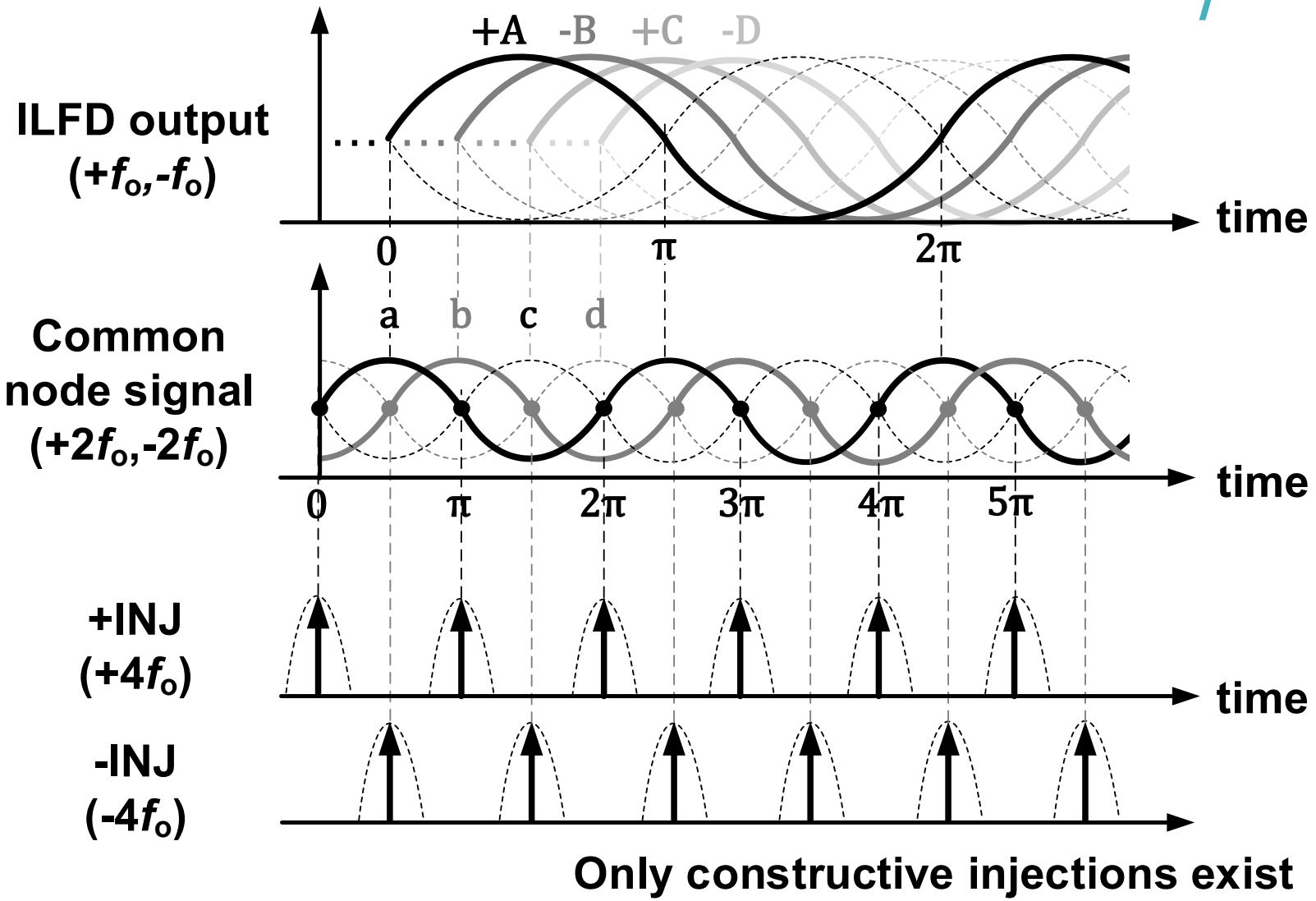
Constructive injection in black

Dual-Step Injection ILFD



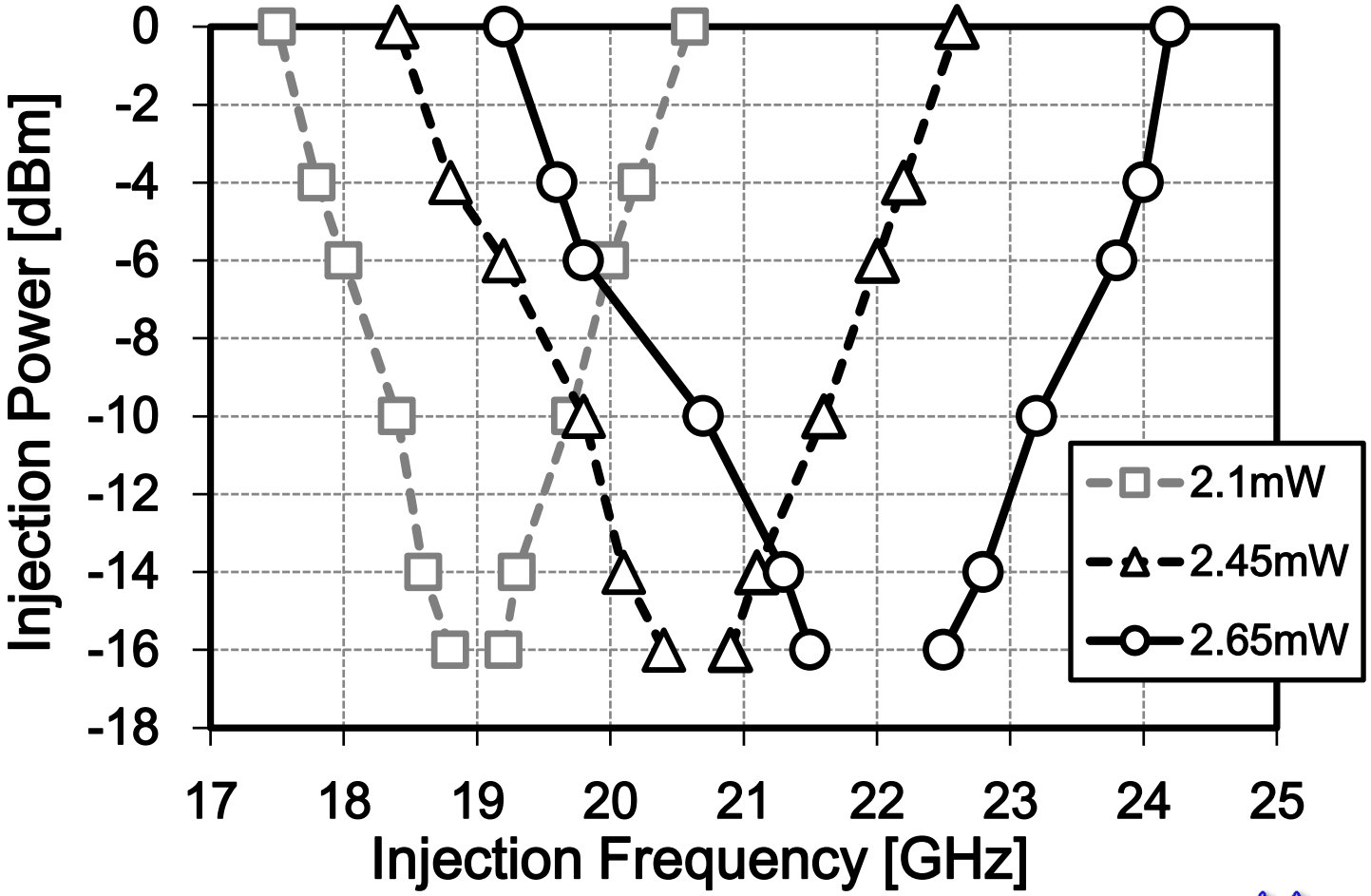
T. Siriburanon, *et. al,* ESSCIRC 2013

Dual-Step Injection ILFD



Measured Locking Range

- **Can cover required range for 60GHz Applications (19-22GHz)**



ILFD Performance Comparison

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	Features	Div. Ratio	Locking Range* (GHz)	Locking Range* (%)	Power (mW)	Area (mm^2)
[1]	Direct mixing	4	22.6-28	21	8.3	0.140
[2]	Direct mixing	4	6.0-7.6	22	6.8	0.007
[3]	Direct mixing	4	31.0-41.0	27	3.3	0.002
[4]	LC Direct mixing (3^{rd} harmonic boosting)	4	58.5-72.9	21.9	2.2	0.032
[5]	CML + LC ILFD	4	13.5-30.5	77.3	7.3	0.33
[6]	Dual-Step Mixing	4	13.4-21.3	31	3.9	0.003
This Work	Dual-Step Mixing	4	19-24.2	24	2.65 (with buffers)	0.002

[1] A-SSCC'07 [2] RFIC'04 [3] ISSCC'06 [4] CICC'12
[5] MTT'11 [6] A-SSCC'11

20GHz SS-PLL Measurement

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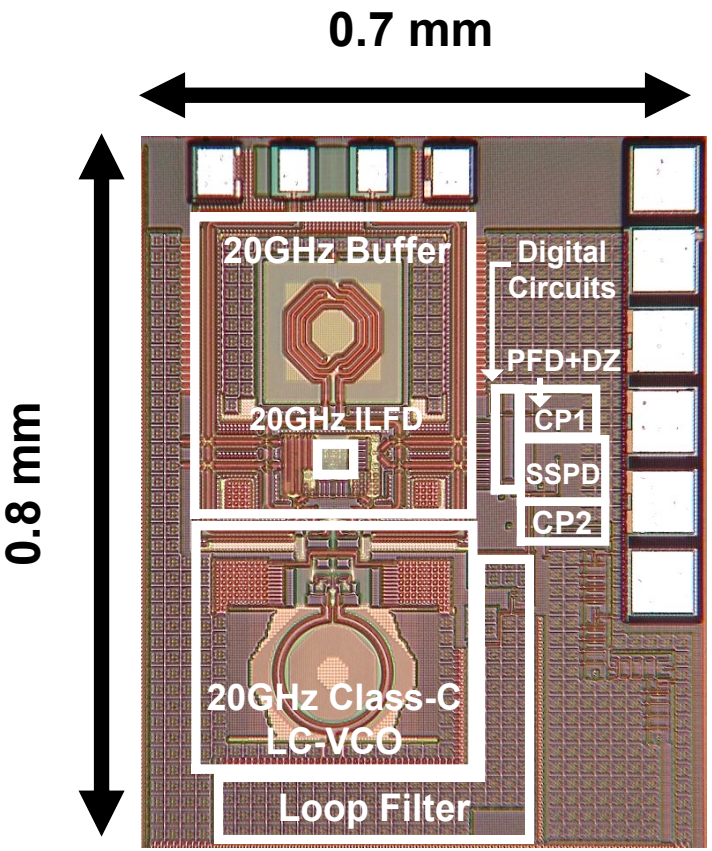
Freq. (GHz)	19.38 - 22.58(15.3%)
Frequencies (GHz)	19.44, 19.80, 20.16, 20.52, 20.88, 21.24, 21.60
Ref. Spurs (dBc)	-58 dBc @ f_{REF}
PN@1MHz(dBc/Hz)	~ -104
Ref. freq. (MHz)	36/40 (18/20)
Out Power (dBm)	0 ~ -4
Total Power (mW)	20.2
Process	65nm CMOS



20GHz SS-PLL

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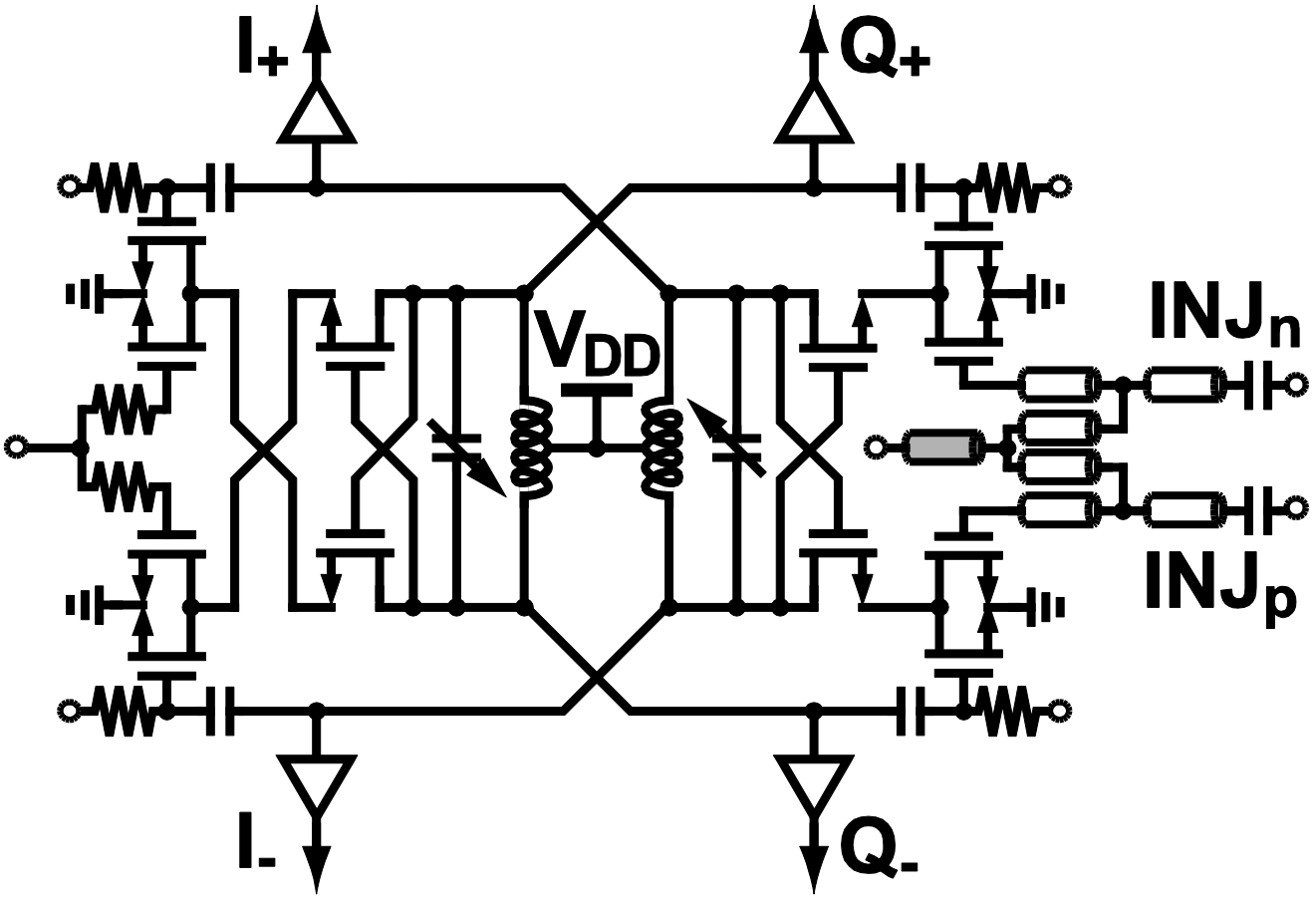
Schematic of 60GHz QILO



K. Okada, *et al.*, JSSC 2013

60GHz Quadrature Injection-Locked Oscillator

60GHz QILO Measurement Summary

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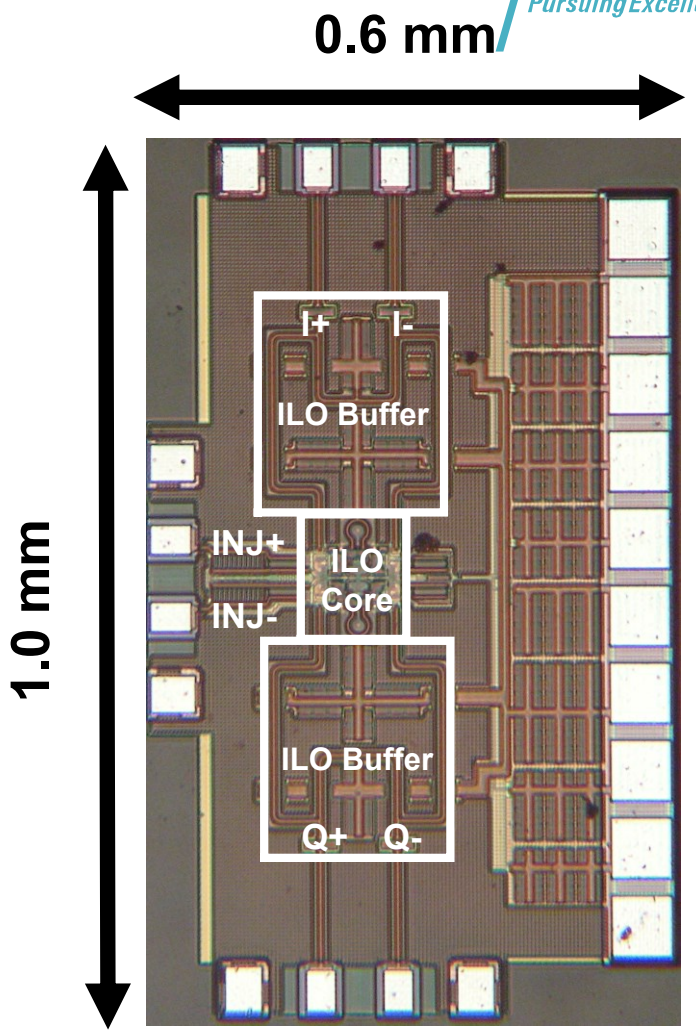
Process	65nm CMOS
Supply Voltage (V)	1.2
Tuning Range (GHz)	58.3-65.4
P_{DC} (mW)	14.0
Output Power (dBm)	-10.0



60GHz QILO

Phase Noise Characteristics

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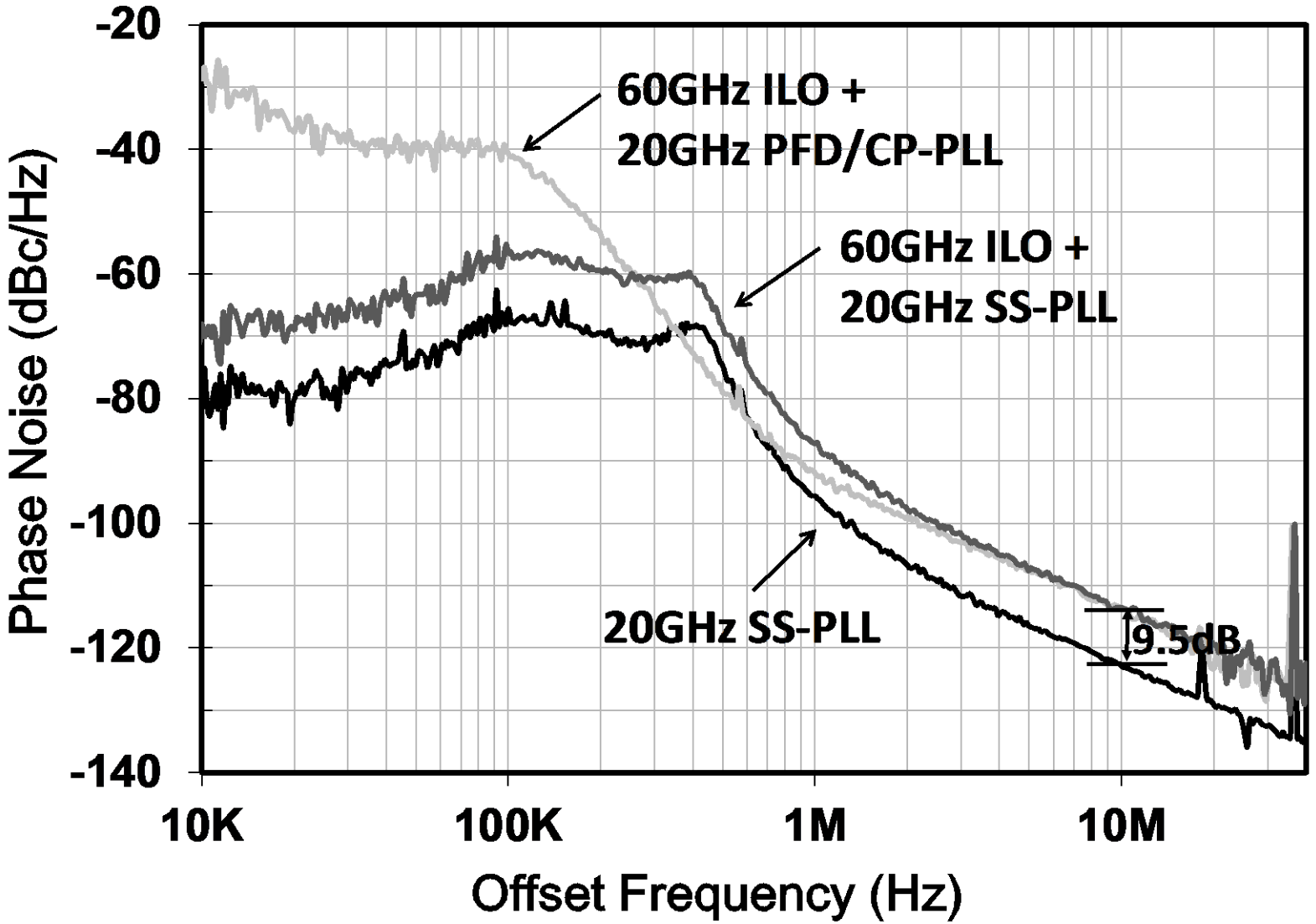
At a carrier frequency of 62.64GHz



Performance Comparison

Ref.	REF Freq. (MHz)	Frequency (GHz)	Phase Noise @10kHz offset	Phase Noise @10MHz offset	Features	Power (mW)
[1]	100	57.0-66.0	-66 dBc/Hz	-108 dBc/Hz	Direct 60GHz QPLL	78
[2]	203.2	59.6-64.0	-65 dBc/Hz	-112 dBc/Hz	30GHz PLL + Coupler	76
[3]	100	56.0-62.0	-71 dBc/Hz	-109 dBc/Hz	60GHz AD-PLL	48
[4]	40	53.8-63.3	-89 dBc/Hz	-108 dBc/Hz	60GHz SS-QPLL	42
[5]	18	58.1-65.0	-40 dBc/Hz	-117 dBc/Hz	Sub-harmonic Injection 20GHz PLL + 60GHz QILO	72
This Work (normal)	18/20	58.3-65.4	-40 dBc/Hz	-115 dBc/Hz	Sub-harmonic Injection 20GHz PLL + 60GHz QILO	32.8
This (SS)	18/20	58.3-65.4	-69 dBc/Hz	-115 dBc/Hz	Sub-harmonic Injection 20GHz SS-PLL + 60GHz QILO	34.2

[1] K. Scheir, *et al.*, ISSCC 2009 [2] C. Marcu, *et al.*, JSSC 2009 [3] W. Wu, *et al.*, ISSCC 2013
[4] V. Szortyka, *et al.*, ISSCC 2014 [5] W. Deng, *et al.*, JSSC 2013

Conclusion

- **Low in-band and out-band phase noise have been achieved through sub-sampling and sub-harmonic injection-locked techniques, respectively**

- **With an assist of a low-power Dual-Step-Mixing ILFD, the proposed 60GHz SS-PLL achieves low power consumption while maintaining good phase noise performance**