A 60-GHz Sub-Sampling PLL Using A Dual-Step-Mixing ILFD

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***Abstract* — This paper presents a 60-GHz sub-sampling PLL using a dual-step-mixing injection-locked frequency divider (ILFD). The sub-sampling operation achieves lower in-band phase noise, and the dual-step-mixing ILFD realizes a low power operation. The proposed synthesizer has been implemented in a standard 65-nm CMOS technology. It achieves a phase noise of -115dBc/Hz at 10MHz offset. The sub-sampling operation helps reducing an integrated jitter from 12ps to 2.1ps. It consumes only 34mW.**

Index Terms — CMOS, Millimeter-Wave, PLL, sub-sampling, injection-locked frequency divider, 60GHz.

I. Introduction

To meet the continuous demand for higher data rates in future wireless connections, a 9-GHz unlicensed bandwidth in 60GHz spectrum is one of the most promising solution. It has already been specified by a number of standards, *i.e.,* IEEE802.11ad/WiGig, IEEE802.15.3c, wirelessHD, ECMA-387 and ISO/IEC13156. The main requirements of the 60GHz synthesizer which is the heart of 60GHz transceivers are frequency coverage that should cover four main channels, as well as the channels in between for channel bonding capability, *i.e.,* 58.32GHz, 59.40GHz, 60.48GHz, 61.56GHz, 62.64GHz, 63.72GHz, and 64.80GHz. Secondly, it should support dual reference clock, *e.g.*, 36MHz and 40MHz while consuming low power consumption. More importantly, out-of-band phase noise performance should be lower than -90dBc/Hz for 16QAM. Moreover, the in-band phase noise should be lowered depending upon the bandwidth of baseband carrier-recovery circuitry [1].

Sub-harmonic injection-locked technique [2] has shown relatively lower out-of-band phase noise due to a better compromise between quality factor of inductor and capacitor at 60GHz comparing to PLLs with VCO running directly at 60GHz [3]-[5]. However, to support required channels with specified reference clocks, integer-N mm-wave PLLs in [2] suffer from poor in-band phase noise performance as in-band noises are multiplied by the high divider feedback ratio N since the PLL in-band phase noise contributed by PFD/CP can be approximated as $L_{\text{in-band}} \approx (S_{\text{i,n}} \cdot N^2)/(2 \cdot K_{\text{D}}^2)$ [6], where $S_{\text{i,n}}$ is power spectral density of PD/CP current noise, N is a division ratio in a PLL and K_{D} is the CP gain. In the proposed sub-sampling operation, high-divide-ratio digital dividers have been omitted in the feedback path to reduce in-band phase noise while being compatible with 36MHz and 40MHz reference clocks to generate all required channels and support channel bonding [7]. As well, instead of using two cascading CML dividers as prescaler divider, a single dual-step-mixing ILFD is utilized for power reduction in the 60GHz PLL [8].

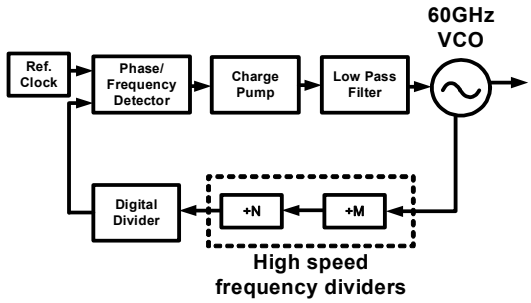


Fig.1. Simplified architecture of 60GHz PLLs [3]-[5]

II. Design of Proposed Architecture

The proposed synthesizer includes a sub-harmonic 20GHz sub-sampling PLL (SS-PLL) and a 60GHz QILO as shown in Fig.2. The 20GHz PLL can perform both classical PFD/CP mode (E_{n}=0) and sub-sampling mode (E_{n}=1). For a PFD/CP mode, E_{n} is set to 0. The sub-sampling loop is disabled as CP_1 is off and PFD in lower loop works without any dead zone. A divide-by-2 divider is placed after reference clock to support channel bonding but at an expense of lower reference clock. "SEL_1" bit of MUX_1 can control corresponding division ratio of input 36/40MHz reference clocks.

Due to the limited acquisition range of SSPD, a frequency-locked loop (FLL) is necessary. In this work, for sub-sampling mode, E_{n} is set to 1, a dead zone of PFD is created. PFD controls CP_2 until the signal is close to lock working as an FLL. Then, the SSPD samples the divider output with 18MHz reference clock converting phase error into voltage variation. Current output from CP_1 controls VCO in the locked state with significantly less N ratio. The sub-sampling mode bypasses a divide-by-60 ratio and an in-band suppression in the feedback loop is calculated to be approximately 15dB when sampled by the divided reference clock.

III. Key Circuit Building Blocks

A. 20GHz VCO and its Buffer

In this work, a class-C VCO which theoretically has higher DC-RF current conversion efficiency comparing to Class-B

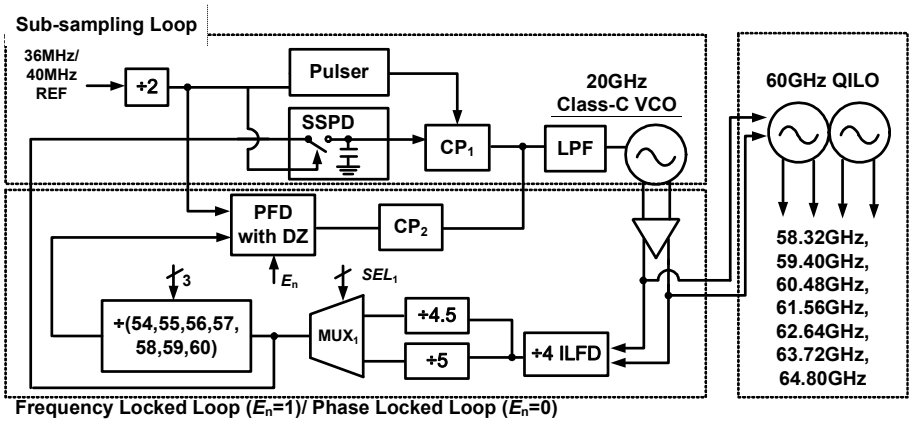


Fig.2. Proposed architecture for 60GHz sub-harmonic injection-locked sub-sampling quadrature frequency synthesizer [7]

VCO are utilized. The frequency can be tuned by a varactor and a 4-bit capacitor array. Cross-coupled capacitors are used in 20-GHz buffer to help cancel undesired parasitic gate-to-drain capacitances which improves reverse isolation [1].

B. 20GHz Dual-Step-Mixing ILFD

More importantly, to avoid power-consuming two divide-by-2 CML dividers in cascade, a single-stage divide-by-4 ILFD is employed using dual-step-mixing technique [8]. As shown in Fig.3 and Fig.4, the injected differential signals are applied at the switches across common node of corresponding delay cells which periodically gives positive amplitude peak at zero-crossing point of second harmonic signals resulting maximum phase shifts and synchronize the second harmonic signal with the injected signal. Then, second harmonic signal at common nodes of each delay cell further synchronize with the fundamental output and lock it to the injected signals. As a result, it can obtain wide locking range and low-power [8].

C. 60GHz QILO

The 60GHz QILO [1] is composed of two LC tanks which are coupled to generate quadrature signals. The frequency can be adjusted by coarse and fine tuning.

IV. EXPERIMENTAL RESULTS

The proposed 60GHz frequency synthesizer is implemented in a standard 65nm CMOS process. The microphotographs of both chips are shown in Fig.5 in which the 20GHz SS-PLL and QILO occupy an area of 700μm×800μm and 1000μm×600μm including PADs, respectively. The phase noise is evaluated using an Agilent E5052B signal source analyzer (SSA) and a 50-to-75 GHz external mixer. The 60GHz QILO consumes an average power of 14mW from 1.2V supply. It can generate free-running frequencies from 58.3-65.4GHz.

To validate the performance of the divide-by-4 dual-step mixing ILFD, the measured locking range of the ILFD are shown in Fig.6. It achieves the widest locking range of 6.6GHz (28%) for divide-by-4 operations while consuming 4.2mW which covers the required frequency range for 60GHz wireless standards [8]. Fig.8. shows the measured phase noise characteristics of 20GHz SS-PLL at carrier frequency of 20.88GHz, 60GHz QILO locked to 20GHz PFD/CP PLL, and 60GHz QILO locked to 20GHz SS-PLL both at a carrier frequency of 62.64GHz. In the sub-sampling mode, the out-of-band phase noise of 60GHz QILO locked to 20GHz SS-PLL is maintained at -115dBc/Hz at 10MHz offset, where its in-band phase noise shows a 15dB reduction at 100 kHz offset comparing to the case where 60GHz QILO locked to

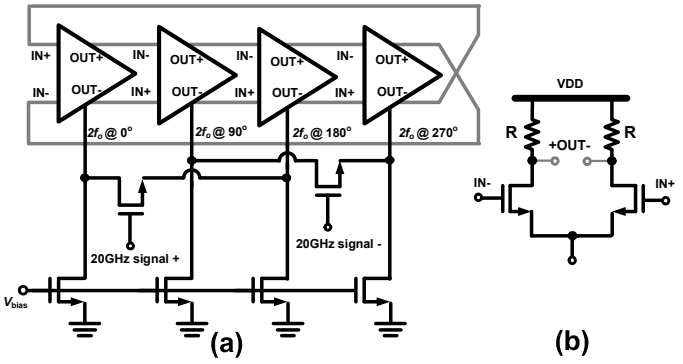


Fig.3. The schematic of (a) 20GHz-to-5GHz dual step mixing ILFD [7] and (b) its delay cell

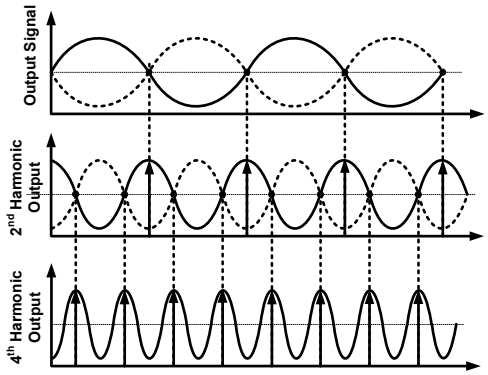
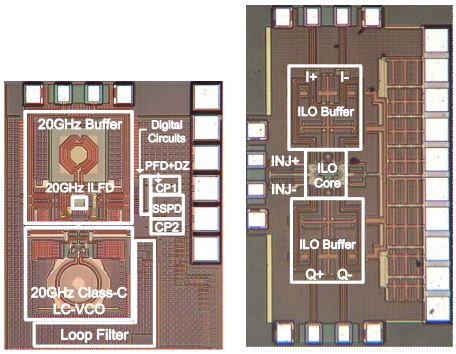


Fig.4 Time diagram at ideal locked case of divide-by-4 operation



(a) (b)

Fig.5. Chip micrographs (a) 20GHz SS-PLL (b) 60GHz QILO [7]

conventional 20GHz PFD/CP PLL. The calibrated output power of 20GHz PLL is approximately -4 dBm. The power consumption of the 20GHz SS-PLL is 20.2mW from 10.6mW of the 20GHz VCO and its buffer, 4.8mW of the ILFD and 4.8mW of digital circuits from 1.2V supply. This is about 3 times power reduction compared to [2]. Table I summarizes the comparison of the proposed work with the state-of-the-art 60GHz PLLs. Sub-harmonic injection method shows the lowest out-of-band phase noise at 10MHz offset comparing to [3]-[5]. However, due to the use of relatively lower REF clock, the work in [2], as well as, PFD/CP mode of the proposed work have higher in-band phase noise [5]-[6]. The sub-sampling loop of the proposed work successfully reduces the division ratio and suppresses the in-band phase noise to -69dBc at 10kHz offset [7].

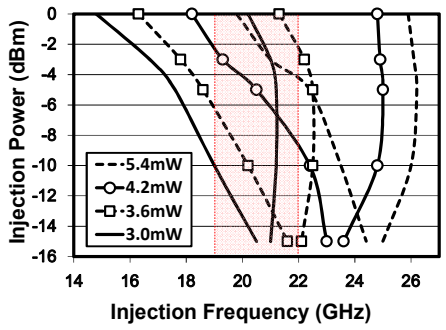


Fig. 6 Measured locking range of divide-by-4 ILFD [8]

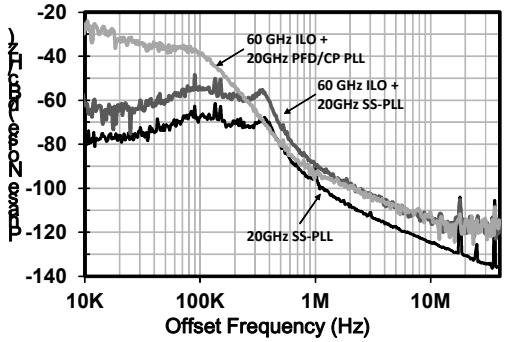


Fig. 7 Phase noise characteristics at 62.64GHz [7]

TABLE I: PERFORMANCE COMPARISON WITH RECENT 60GHZ PLLS [7]

	REF (MHz)	Freq. (GHz)	PN(dBc/Hz)*	Features	Power (mW)
[3]	234	58.0-60.4	-50 /-100	60GHz Diff. PLL	80
[4]	100	56.0-62.0	-71 /-109	60GHz AD-PLL	48
[5]	40	53.8-63.3	-89 /-107	60GHz SS-QPLL	42
[1]	18/20	58.1-65.0	-40 /-117	20GHz PLL + 60GHz QILO	72
[7] (CP)	18/20	58.3-65.4	-40 /-115	20GHz PLL + 60GHz QILO	32.8
[7] (SS)	**18/20**	58.3-65.4	**-69 /-115**	**20GHz SS-PLL** + 60GHz QILO	**34.2**

**Phase noise (PN) comparison at 10 kHz and 10 MHz offset*

V. CONCLUSION

The proposed 60GHz frequency synthesizer using 20GHz SS-PLL and 60GHz QILO is presented. It achieves a suppression of in-band phase noise in sub-sampling mode and also achieves low out-of-band phase noise. It can support various 60GHz standards.

ACKNOWLEDGEMENT

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