A 0.5-to-1 V 9-bit 15-to-90 MS/s Digitally Interpolated Pipelined-SAR ADC Using Dynamic Amplifier

James Lin, Zule Xu, Masaya Miyahara, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

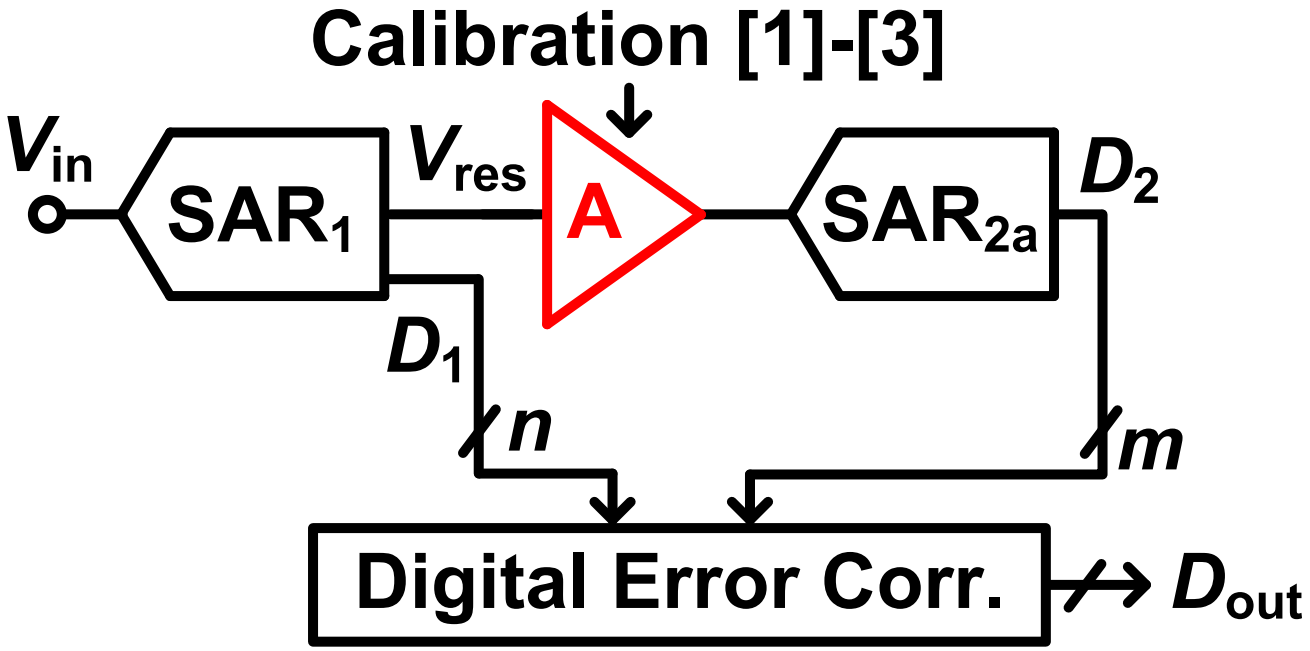
Matsuzawa & Okada Lab

Outline

- Motivation
- Digital Interpolation
- Circuit Design
- Measurement Results
- Conclusion

Conventional Pipelined-SAR ADC

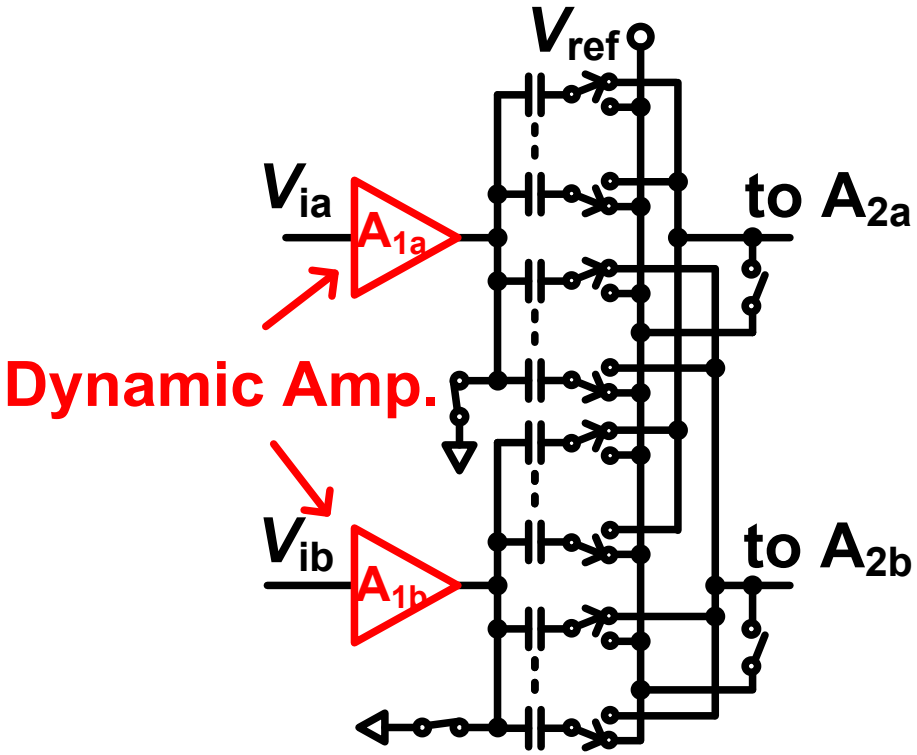
- **Pipelined-SAR ADCs are sensitive to inter-stage gain variation similar to pipelined ADCs**

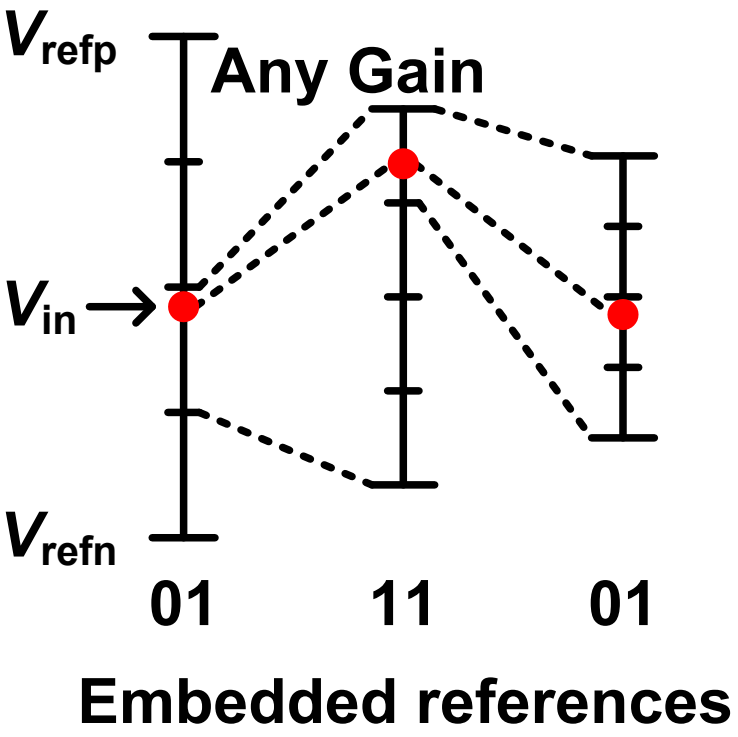


[1] J. Zhong, *et al.*, A-SSCC 2012.
[2] B. Verbruggen, *et al.*, VLSI Circuits 2013.
[3] F. van der Goes, *et al.*, ISSCC 2014.

Analog Interpolation

- For pipelined ADCs, interpolation can be used to alleviate absolute gain requirement [4]





[4] J. Lin, *et al.*, CICC 2013.

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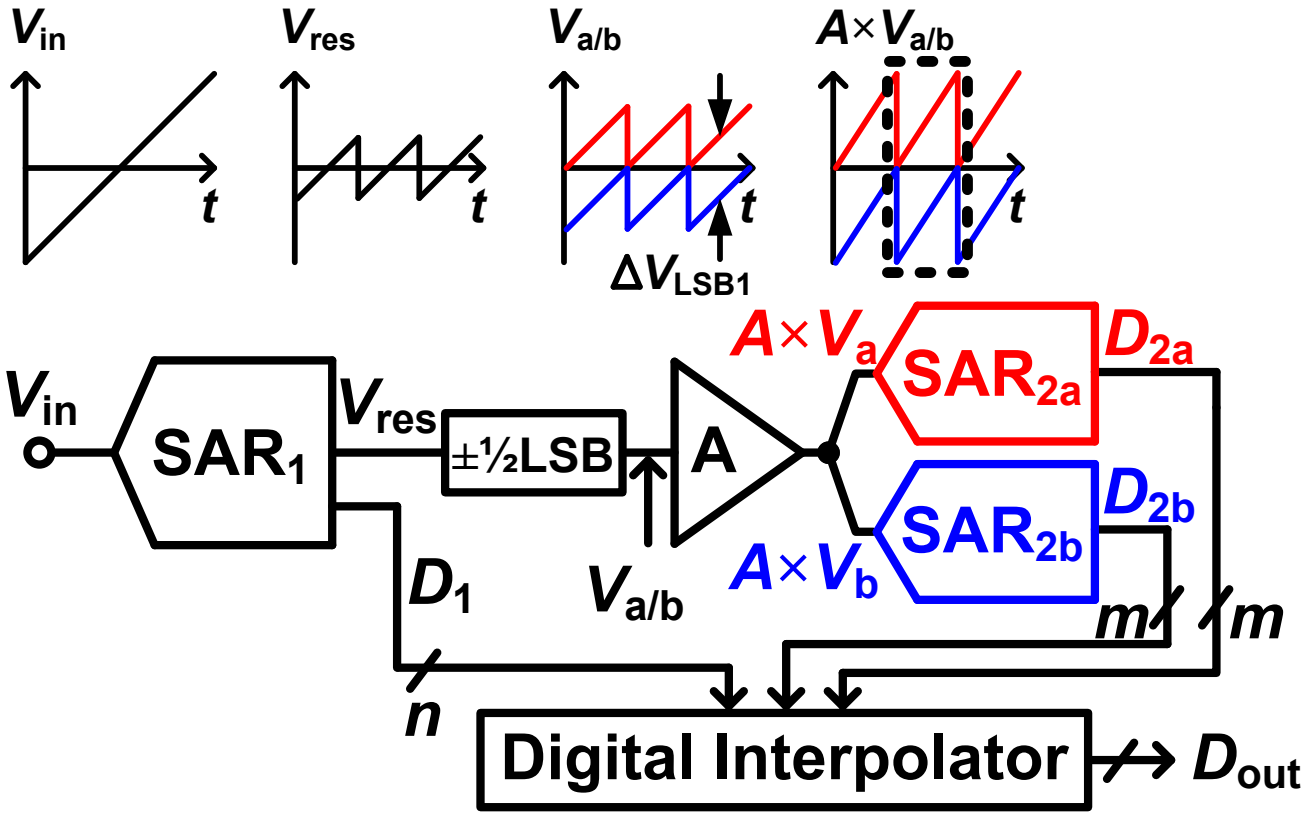
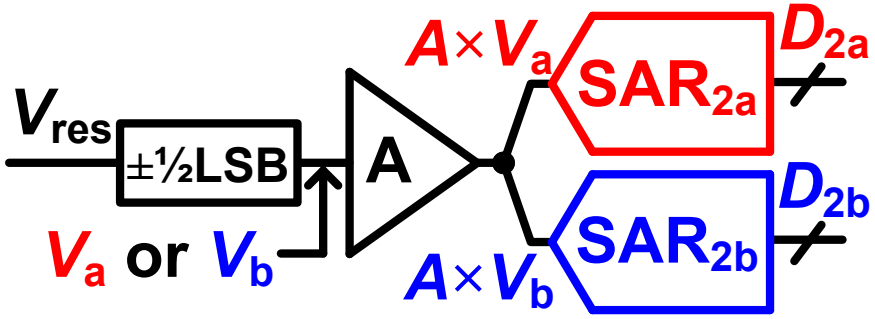
Digitally Interpolated Pipelined-SAR

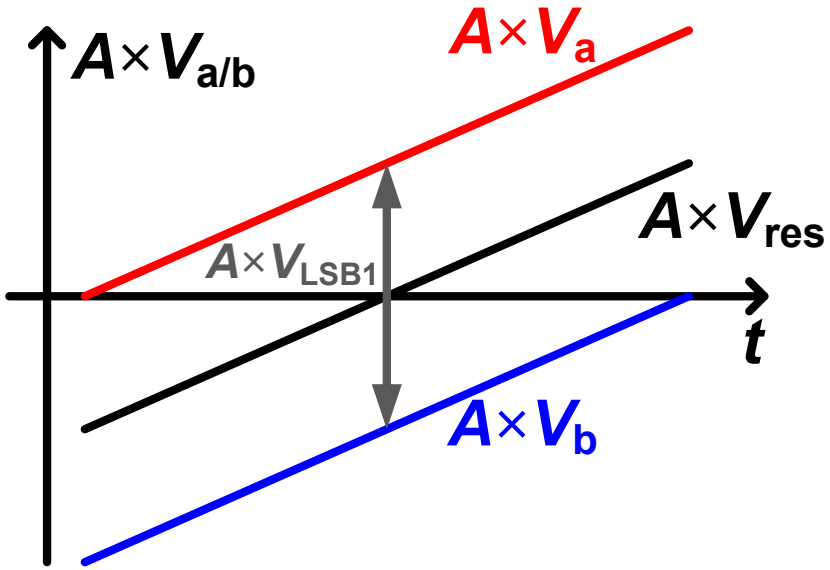
- **Digital interpolation is proposed for its simplicity and robustness**



Insensitive to Inter-Stage Gain

- **Outputs of the second stage is a fractional representation of the original residue**





$$D_{2a} = D\{A\times(V_{res}+\tfrac{1}{2}V_{LSB1})\}$$
$$D_{2b} = D\{A\times(V_{res}-\tfrac{1}{2}V_{LSB1})\}$$

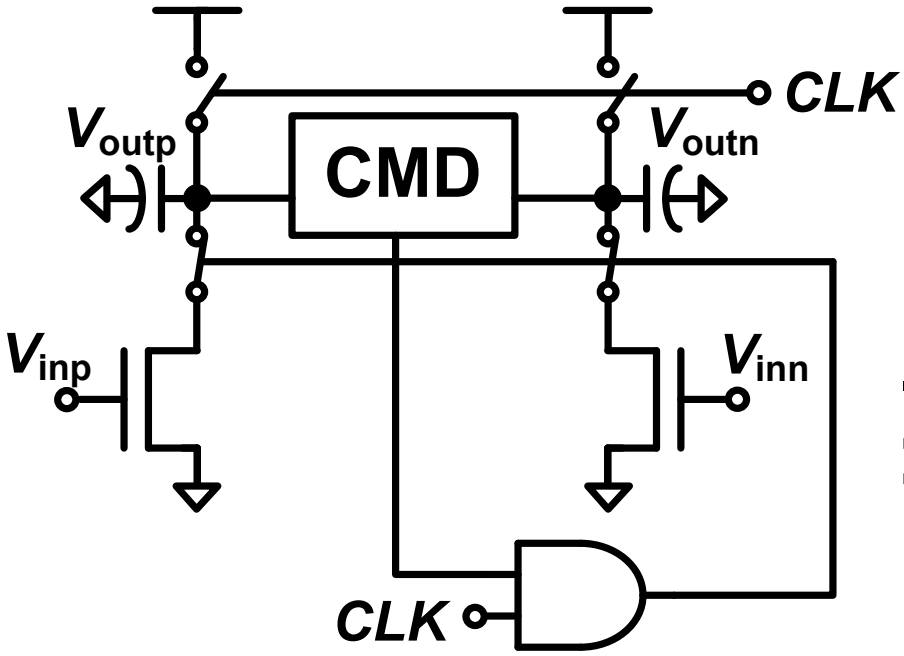
$$D_{2a}+D_{2b} = 2A\times V_{res}$$
$$D_{2a}-D_{2b} = A\times V_{LSB1}$$

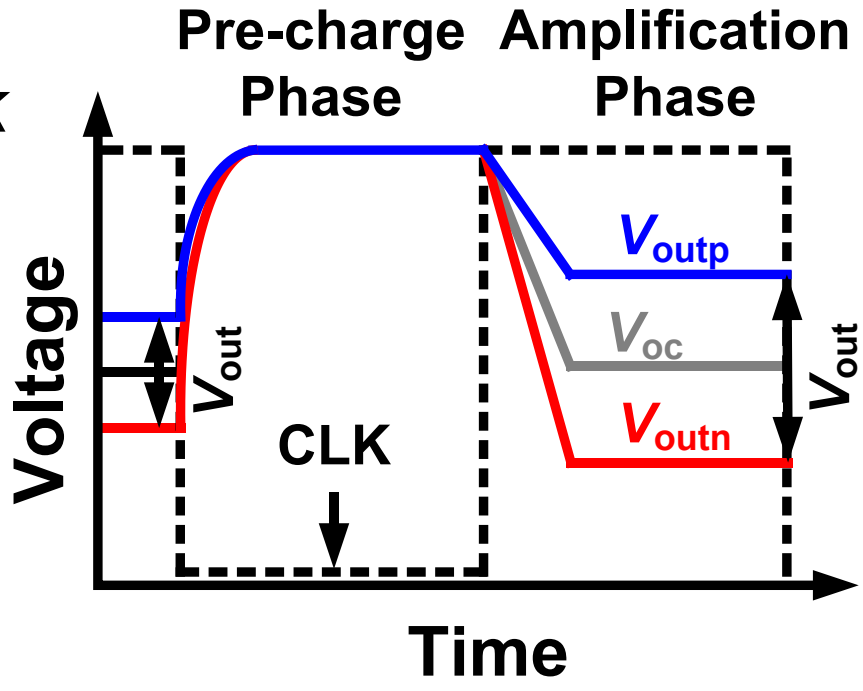
$$\frac{(D_{2a}+D_{2b})/2}{D_{2a}-D_{2b}} = \frac{V_{res}}{V_{LSB1}}$$

$$D_{out} = \left(D_1+\frac{(D_{2a}+D_{2b})/2}{D_{2a}-D_{2b}}\right)\times 2^{m-\alpha}$$

Dynamic Amplifier

- **High speed at low supply voltage and clock-scalable power consumption [5]**





CMD: Common-mode voltage detector

$P_d = fCV_{DD}^2$

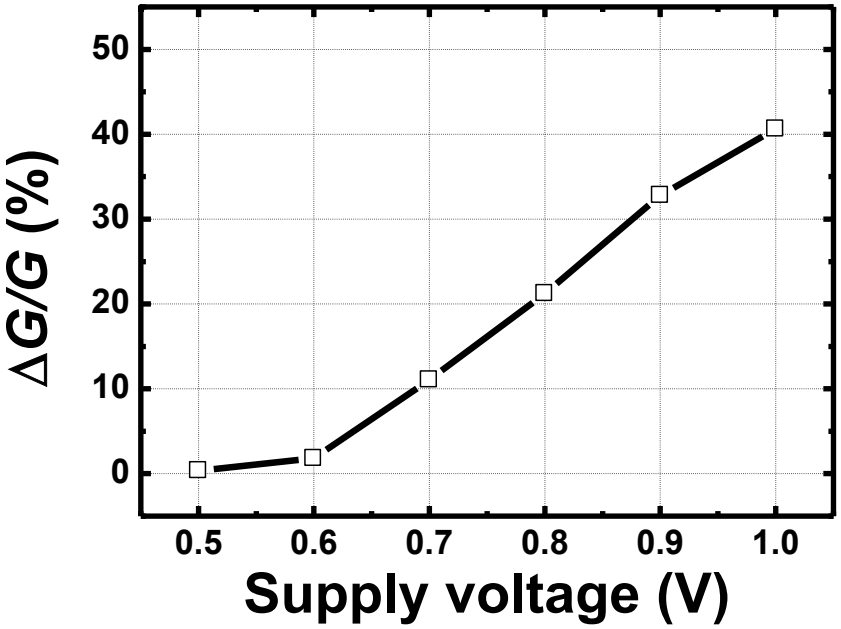
[5] J. Lin, *et al.*, ISCAS 2011.

Inter-Stage Gain Variation

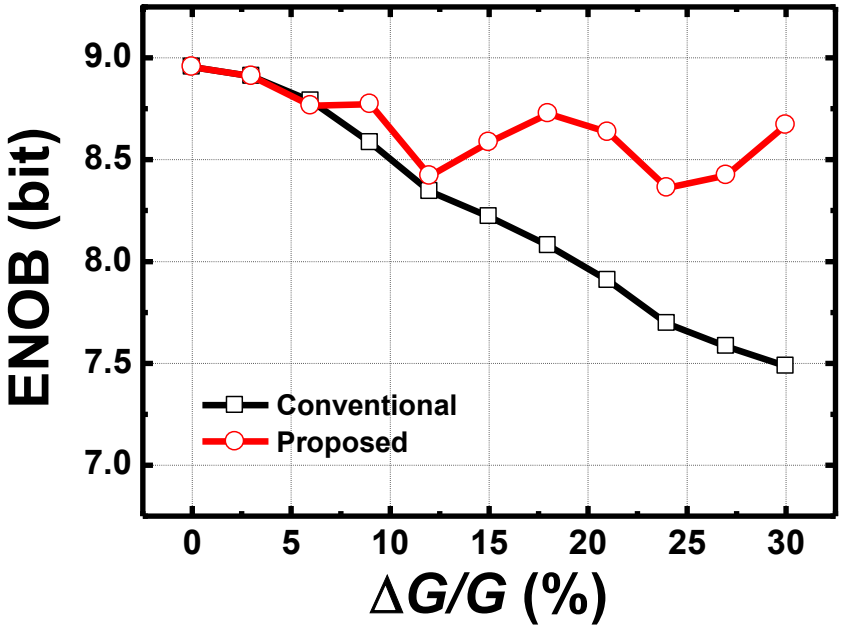
- Dynamic amplifier's gain varies with supply voltage
  → digital interpolation suppresses the ENOB degradation

$$G_{amp} = \alpha(V_{DD}-V_{oc})/V_{eff}\ ,\ 1<\alpha<2$$

$\Delta G/G$ vs. Supply

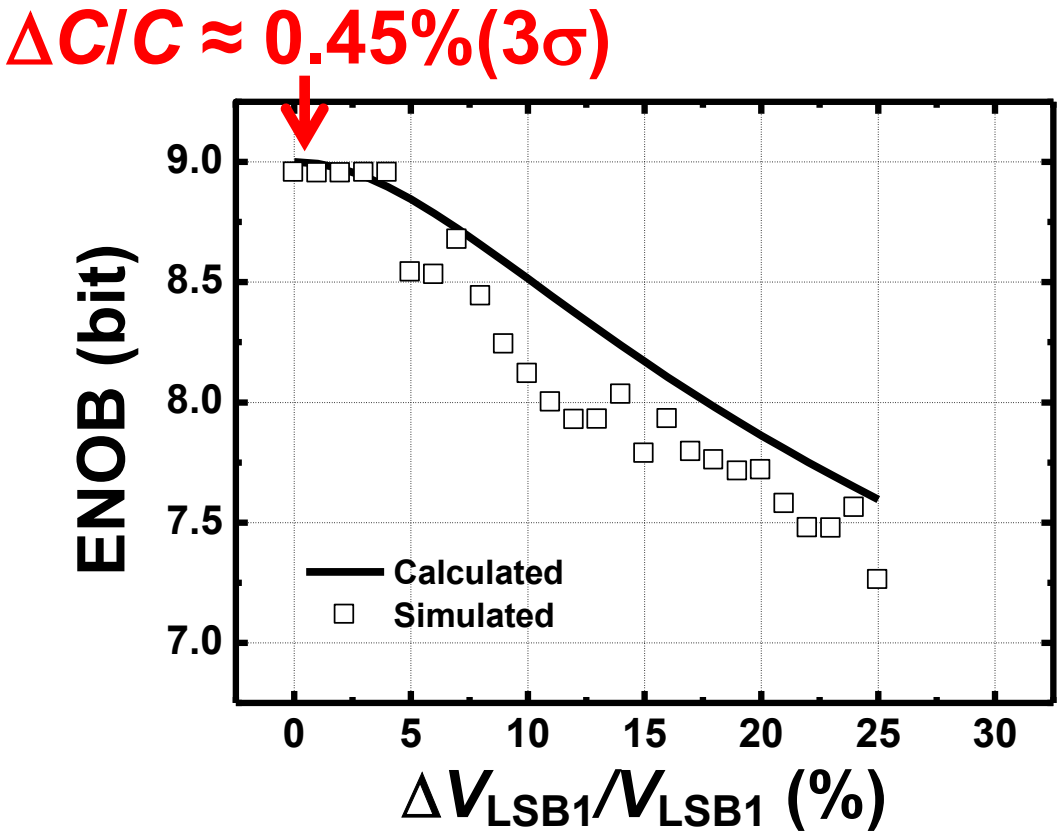


ENOB vs. $\Delta G/G$



Up/Down Shift Error

- **Interpolation requires an accurate shift instead of the conventional accurate gain**



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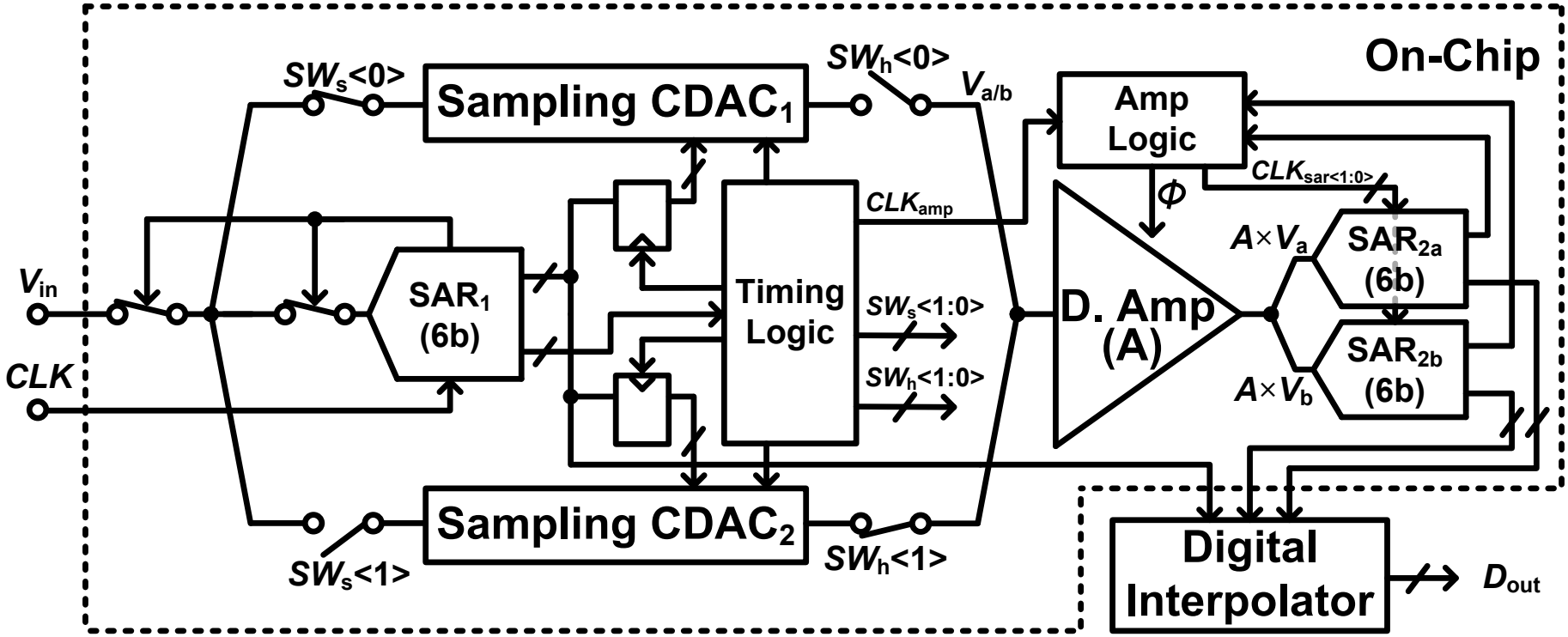
Circuit Design Overview

- ADC architecture
- Self-clocking scheme
- Shared dynamic amplifier
- Ultra-low-voltage SAR ADCs

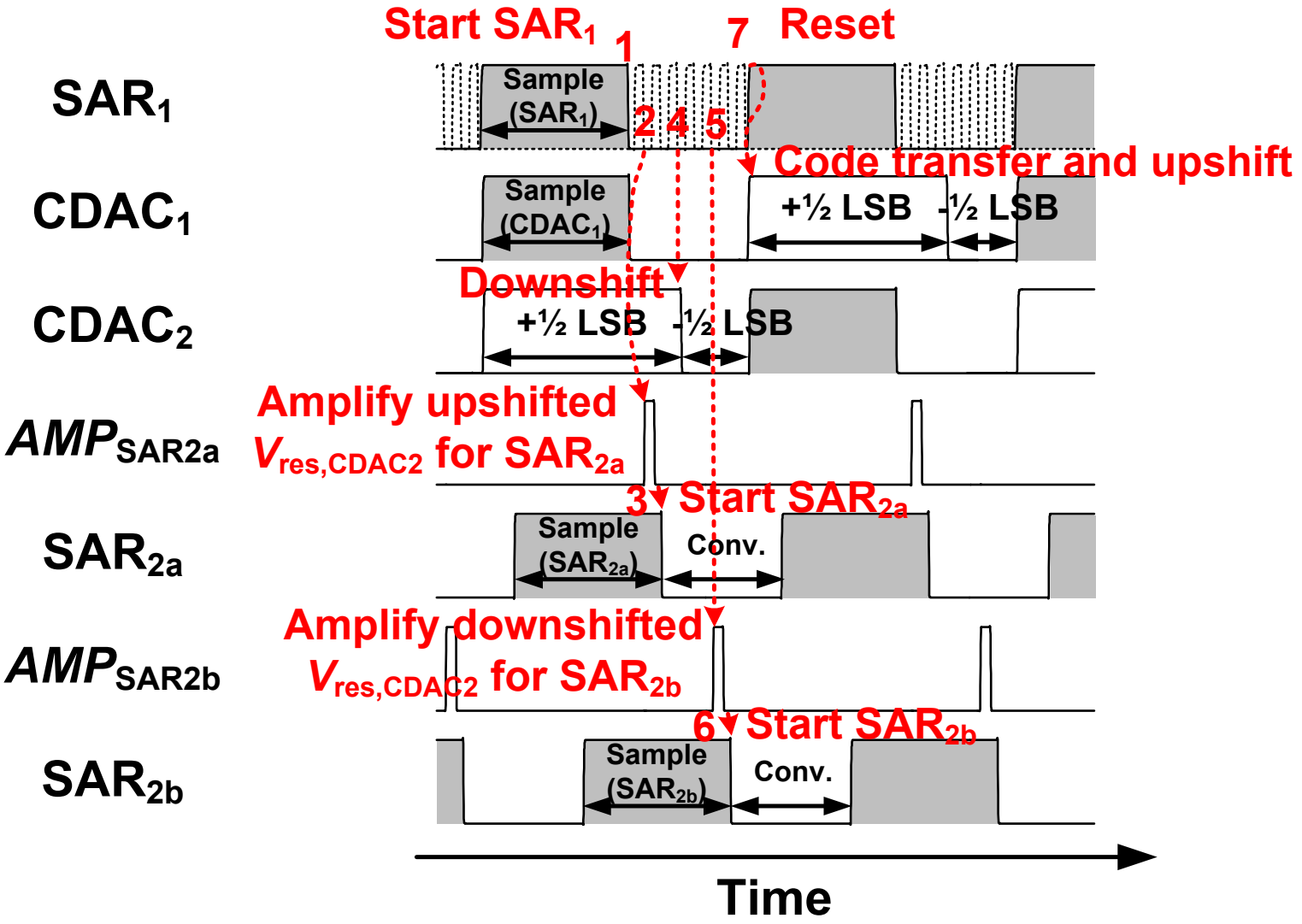
ADC Architecture

- **Proposed ADC consists of two stages**
  - → 6b SAR ADC, 2×sampling CDACs, logic
  - → Dynamic amplifier, 2×6b SAR ADCs, logic



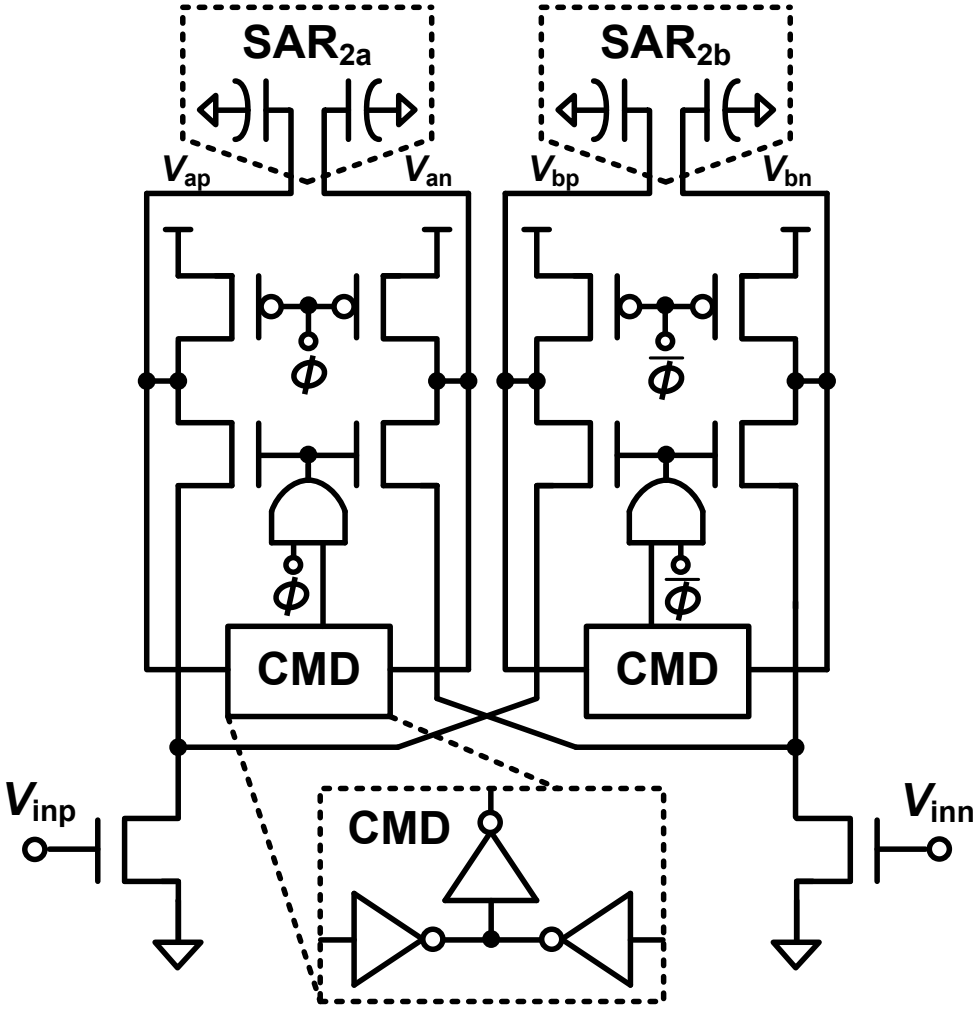
Self-Clocking

- Simulated timing diagram to show the key steps



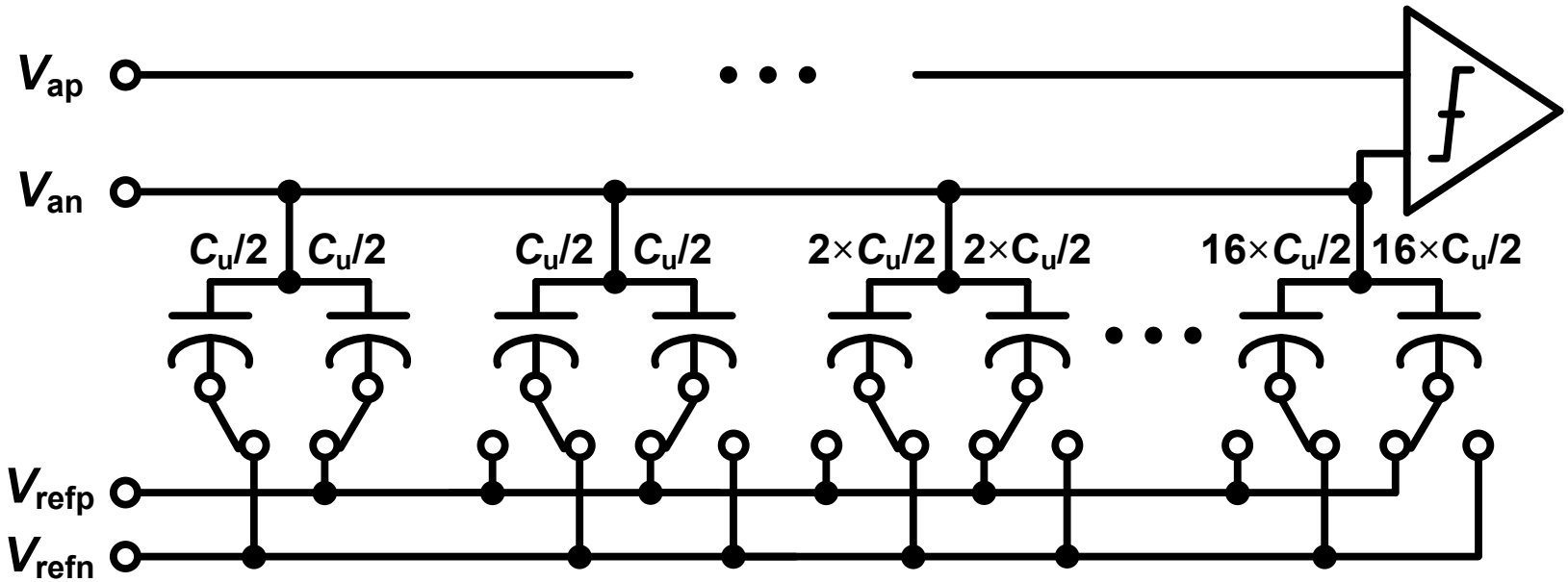
Shared Dynamic Amplifier

- **Same pair of amplifying transistors are shared between the two second-stage SAR ADCs**



Ultra-Low-Voltage SAR ADCs

- Virtual V_{cm} realized using capacitive interpolation achieves high speed



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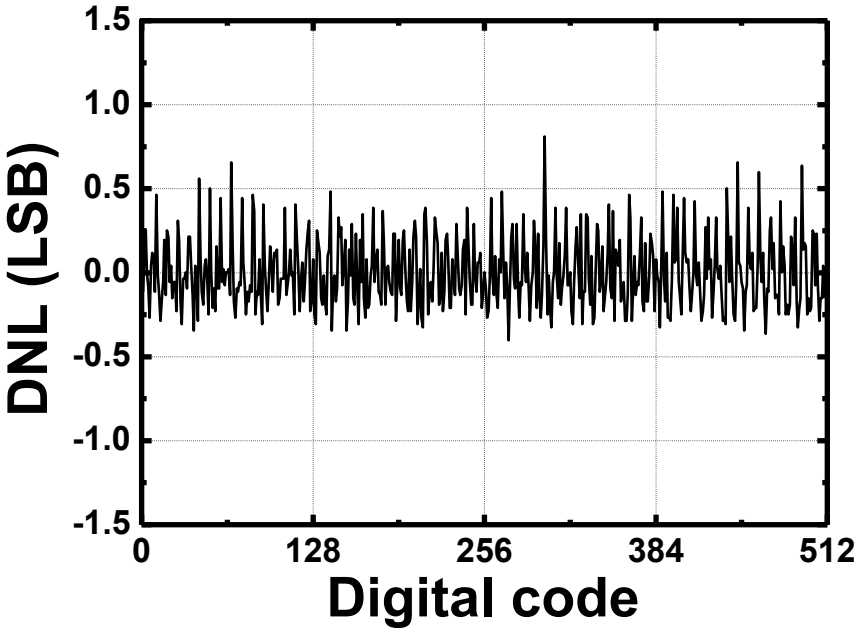
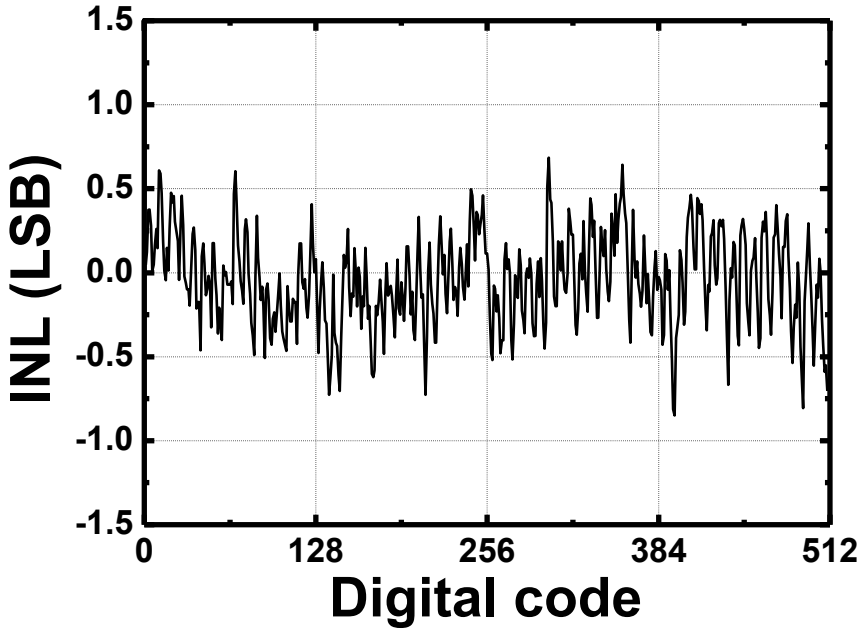
Measured DNL and INL (0.6 V)

- DNL: +0.81/-0.40 LSB
- INL: +0.69/-0.85 LSB

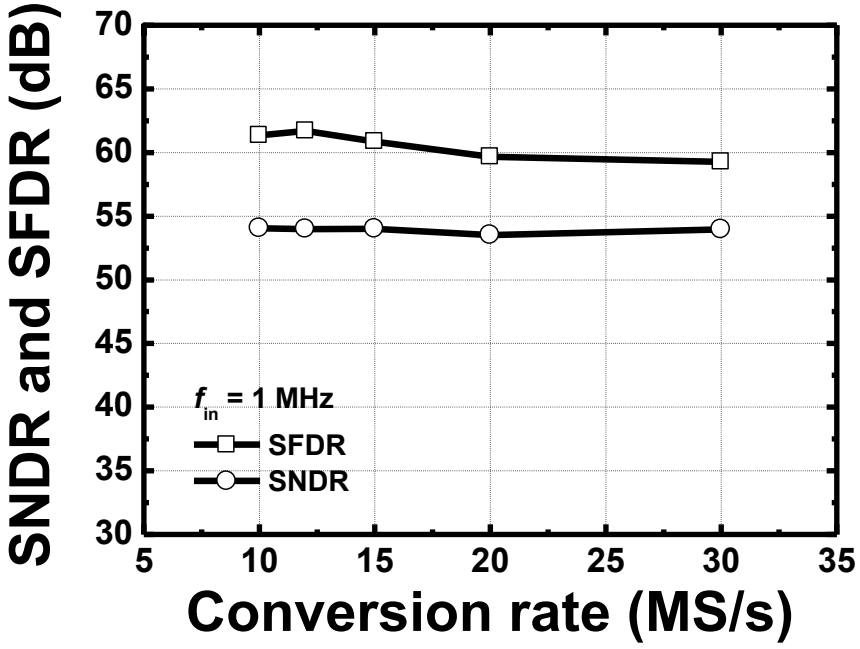




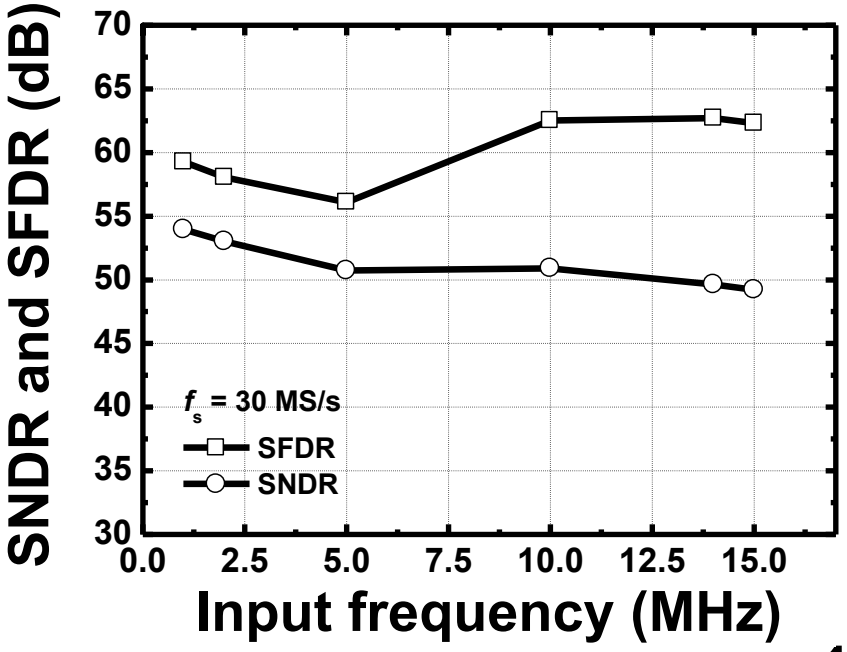
Measured SNDR and SFDR (0.6 V)

- **>49 dB of SNDR is measured up to 30 MS/s with an ERBW >15 MHz**
- **Consumes 481.6 μW (23% analog, 65% digital, 12% reference) at 30 MS/s → FoM=68 fJ/conversion-step**

SNDR & SFDR vs. f_s

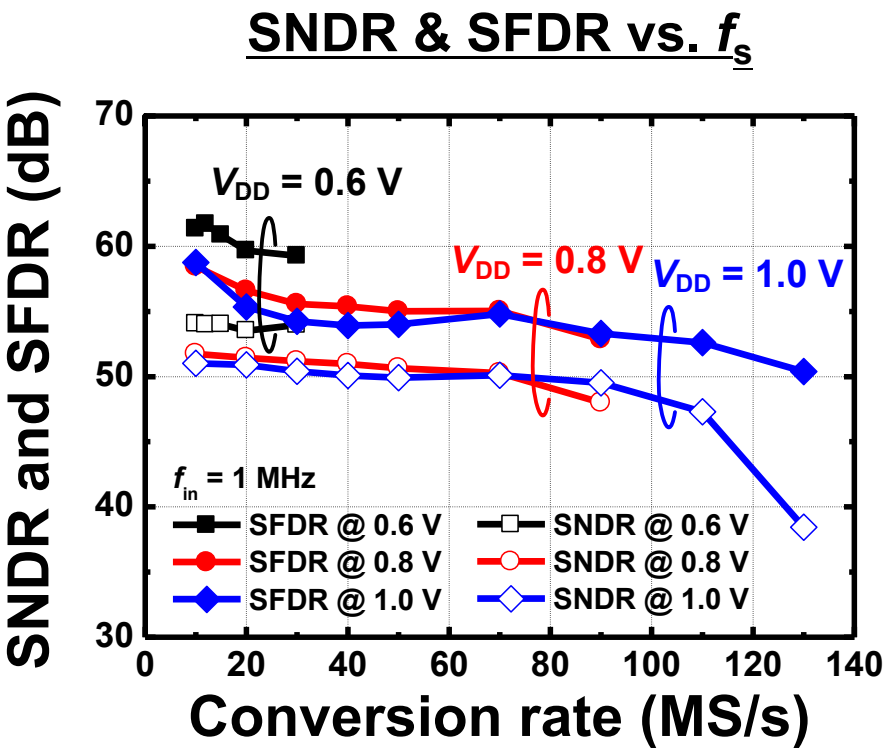


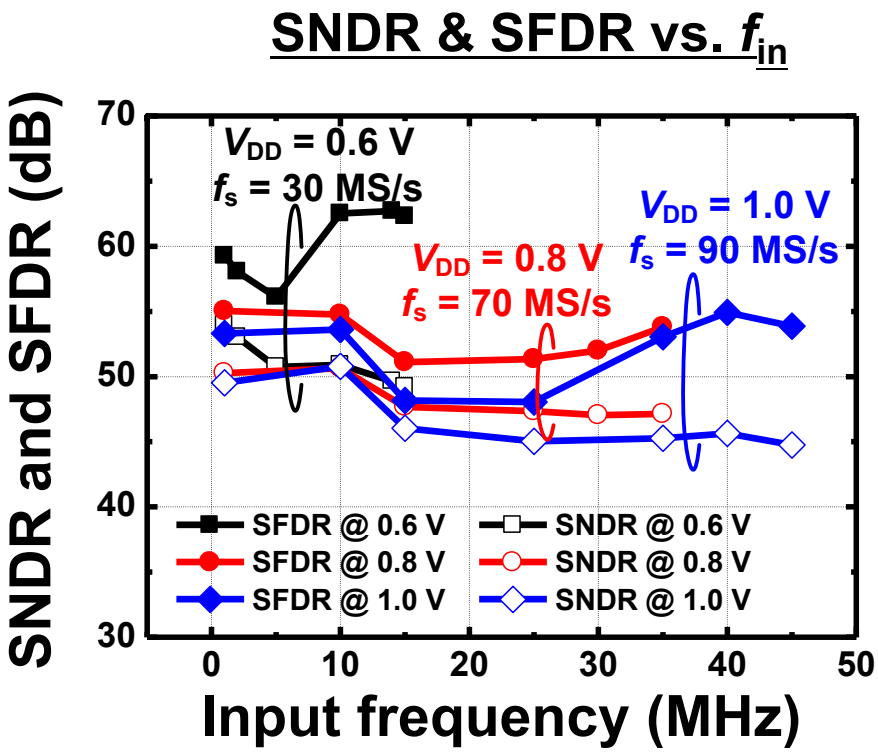
SNDR & SFDR vs. f_{in}



Measured SNDR and SFDR (0.6-1.0 V)

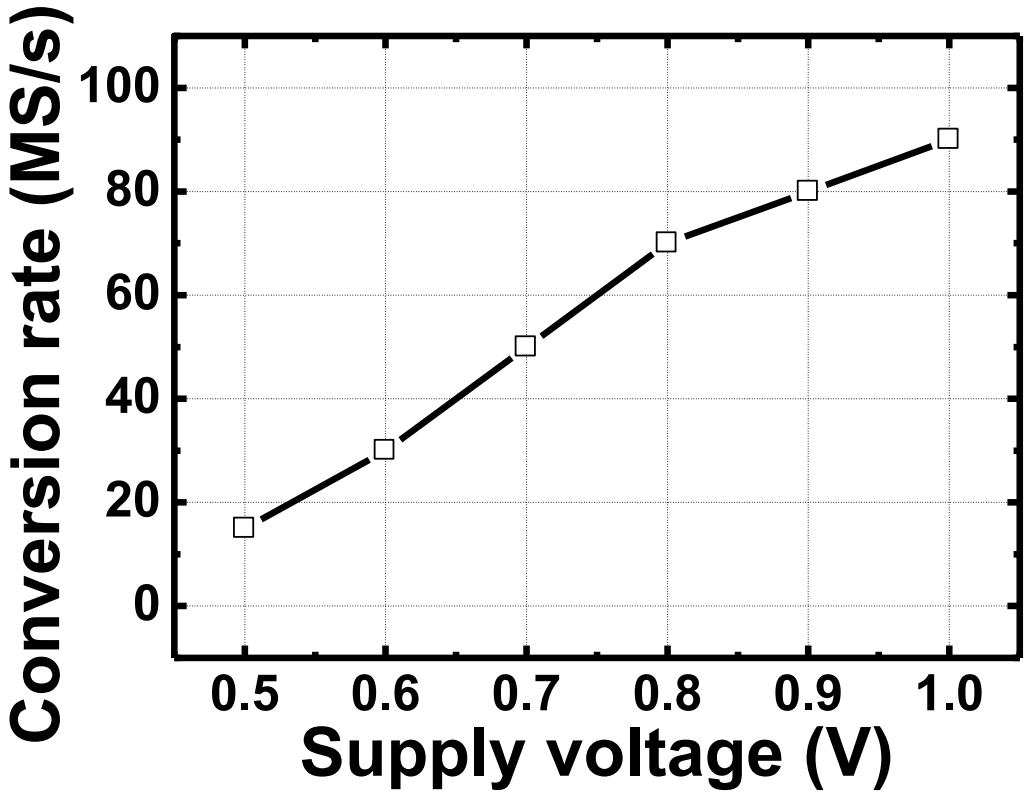
- 0.6 V → 30 MS/s, 68 fJ/conversion-step
- 0.8 V → 70 MS/s, 148 fJ/conversion-step
- 1.0 V → 90 MS/s, 247 fJ/conversion-step





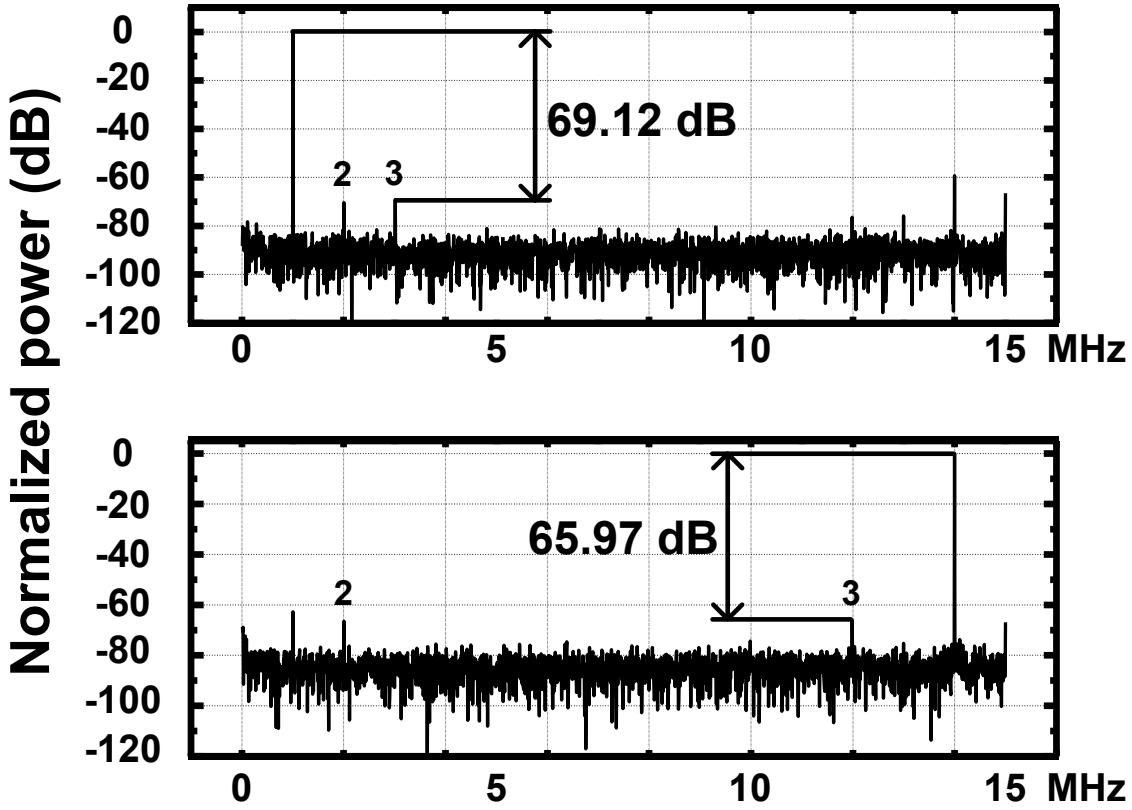
Voltage-Scalable Conversion Rate

- **Conversion rate scales with the supply voltage**



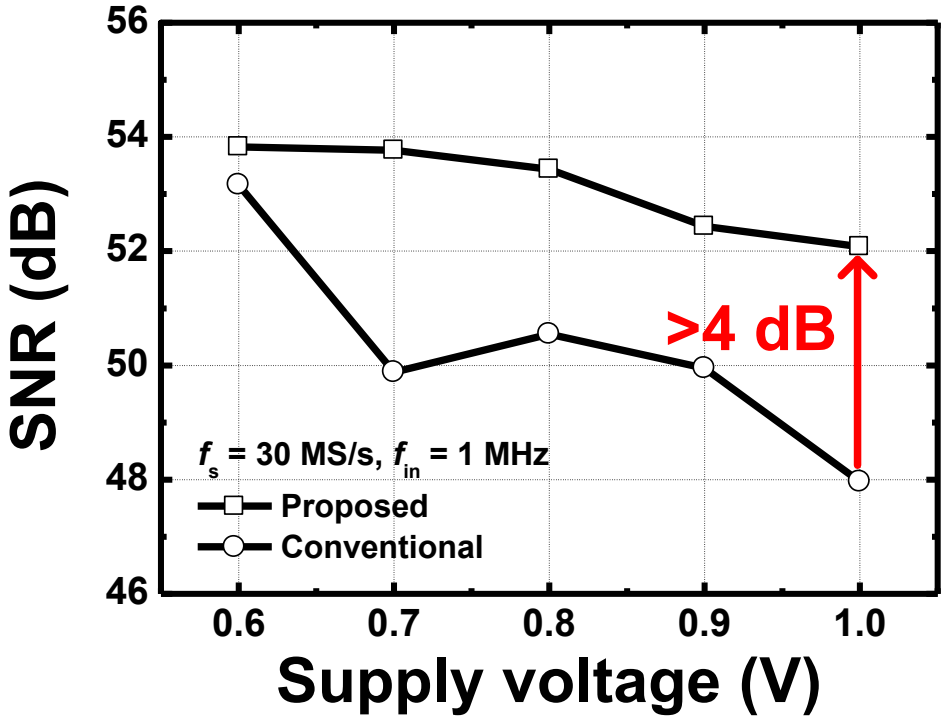
Third-Order Harmonic Distortion

- **ENOB degradation of the prototype ADC is due to noise and a spur caused by interleaved CDACs**
- **3rd-order harmonic spur is <-65 dB**



Inter-Stage Gain Variation

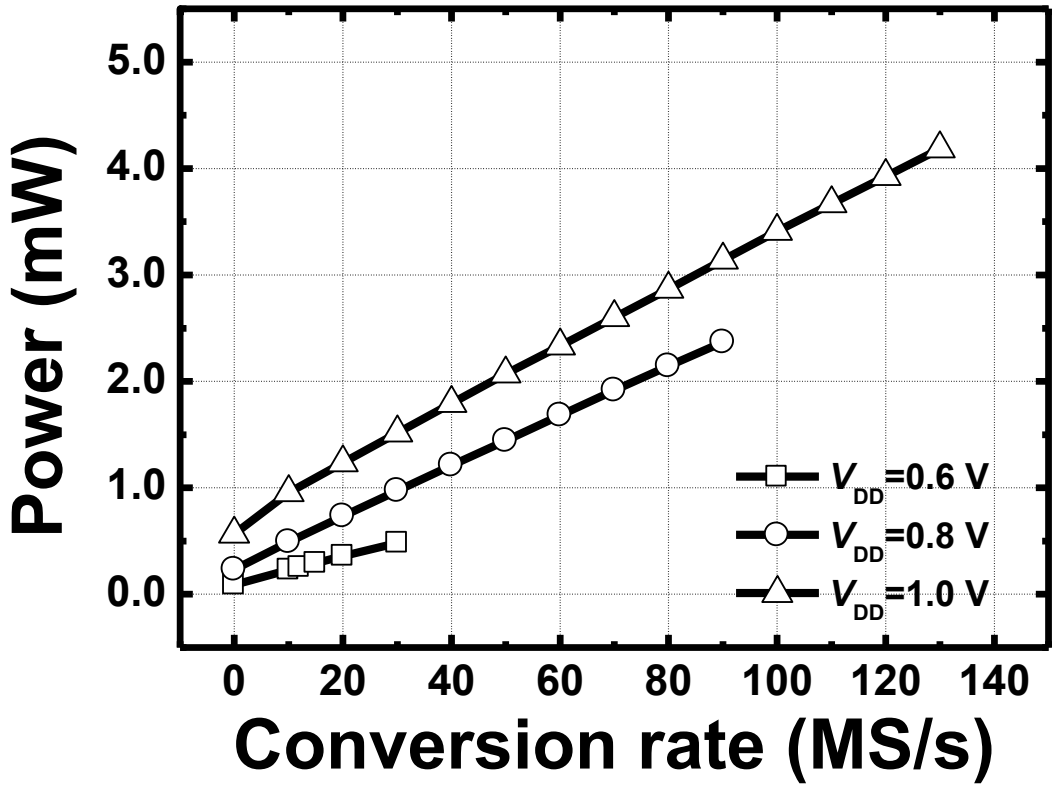
- **Prototype ADC can operation in two modes:**
  - → **Digital interpolation (proposed)**
  - → **External gain adjustment (conventional)**



Clock-Scalable Power Consumption

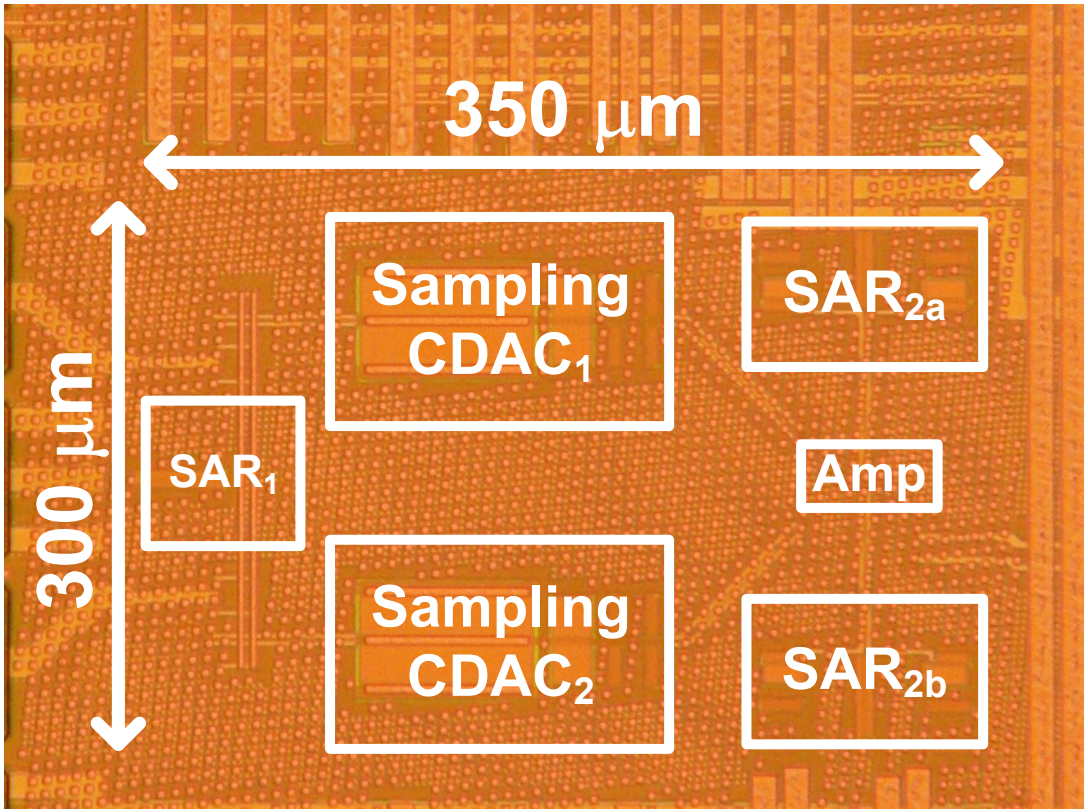
- **Dynamic nature of the entire ADC**

  → Power scales with the clock



Chip Photo

- Prototype ADC is fabricated in 65 nm CMOS with the low threshold and deep N-well options
- The occupied area is <0.11 mm^2



Performance Comparison

- **Digital interpolation and dynamic amplifier realize a flexible ADC**

	[6]	[7]		[8]				This work			
Architecture	Pipe	Pipe		Pipe				Pipelined-SAR			
Resolution (bit)	8	10		12				9			
Supply voltage (V)	0.5	0.5	0.8	0.5	0.6	0.8	1.0	0.5	0.6	0.8	1.0
Conv. rate (MS/s)	10	10	60	5	10	30	50	15	30	70	90
Power (mW)	2.4	3.0	19.2	0.24	0.56	1.61	4.07	0.20	0.48	1.92	3.14
ENOB (bit)	7.7	8.5	8.2	10.7	10.8	10.8	11.0	7.63	7.88	7.54	7.14
FoM (fJ/c.-s.)	1150	825	1118	28.0	30.9	31.1	41	67	68	148	247
Technology (nm)	90	130		65				65			
Active area (mm^2)	1.44	0.98		0.36				0.11			

[6] J. Shen, *et al.*, JSSC 2008.
[7] Y. J. Kim, *et al.*, CICC 2007.
[8] S. Lee, *et al.*, JSSC 2012.

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Conclusion

- **Digital interpolation is validated through a 0.5-to-1 V, 9b, 15-to-90 MS/s pipelined-SAR ADC**

- **Proposed digitally interpolated pipelined-SAR ADC achieves**
  - **→ Robustness to gain variation**
  - **→ Voltage-scalable**
  - **→ Clock-scalable**

Acknowledgement

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Thank you for your interest!

James Lin,
james@ssc.pe.titech.ac.jp