A 0.5-to-1 V 9-bit 15-to-90 MS/s Digitally Interpolated Pipelined-SAR ADC Using Dynamic Amplifier

James Lin, Zule Xu, Masaya Miyahara, and Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552, Japan
E-mail: james@ssc.pe.titech.ac.jp

***Abstract*— This paper presents a 0.5-to-1 V, 9-bit, 15-to-90 MS/s digitally interpolated pipelined-SAR ADC. The proposed digital interpolation alleviates the inter-stage gain requirement of a pipelined-SAR ADC making this ADC insensitive to gain variation. With a relaxed gain requirement, an open-loop dynamic amplifier is employed as the residue amplifier making the proposed design high-speed, clock-scalable, and robust to supply voltage scaling. The prototype ADC fabricated in 65 nm CMOS demonstrates an ENOB of 7.88 bits up to 30 MS/s with an input close to the Nyquist frequency at 0.6 V. At this conversion rate, it consumes 0.48 mW resulting in a FoM of 68 fJ/conv.-step.**

I. Introduction

As CMOS technology continues to scale, the maximum supply voltage is expected to decrease to around 0.5-to-0.6 V in the next decade [1]. With such a low supply voltage, mixed-signal system-on-a-chip (SoC) design becomes more challenging, especially for the analog interface circuits.

For analog circuits, the key challenges include the limited voltage headroom, the reduced SNR, the increased effects of transistor variation, and the speed reduction. Although there are several methods to realize ultra-low voltage (ULV) operation including SAR-based operation [2], [3], very few of them deal with the speed issue [4].

In order to achieve high-speed data conversion at ULV, the work in [4] proposed to use dynamic amplifiers in a pipeline ADC with capacitive interpolation. However, the nonlinearity of the amplifiers limits the resolution. Furthermore, this architecture is susceptible to amplifier mismatch. Although digital calibration can be used to compensate for these errors [5], digital linearity compensation often requires over tens of thousands of data samples, thus increasing the test cost of the digital back-end.

Alternatively, a pipelined-SAR architecture can be adopted to reduce the dynamic amplifier's input signal range. To alleviate the gain requirement of a pipelined-SAR ADC, an interpolation technique in the digital domain is proposed. In this paper, we present an ULV digitally interpolated pipelined-SAR ADC using a dynamic amplifier.

II. Circuit Design

A. Digitally Interpolated Pipelined-SAR Architecture

Conventionally, the pipelined-SAR architecture is capable of achieving high speed and moderate resolution conversion. However, the accuracy of the inter-stage gain is very critical. As a result, several calibration techniques have been proposed to compensate for the gain error [6]-[8]. Instead of adjusting the inter-stage gain, we propose a digitally interpolated pipelined-SAR ADC, which is insensitive to the inter-stage gain error. A conceptual diagram of the proposed digital interpolation is depicted in Fig. 1. After the first stage SAR ADC, SAR_1, completes its trials, the residue voltage, V_{res}, is shifted by ±½LSB of SAR_1 and amplified by a factor of A. These residues are then quantized by the two second stage SAR ADCs, SAR_{2a} and SAR_{2b}. The average output of D_{2a} and D_{2b} is the amplified residue while the difference between the two outputs is the amplified LSB of SAR_1, $A\times V_{LSB1}$. The ratio between the average output and the difference output is a fractional representation of the original residue. Since the amplifier's gain is present in both the average output and the difference output, this technique is insensitive to the amplifier's gain. The final digital output code can be obtained through the

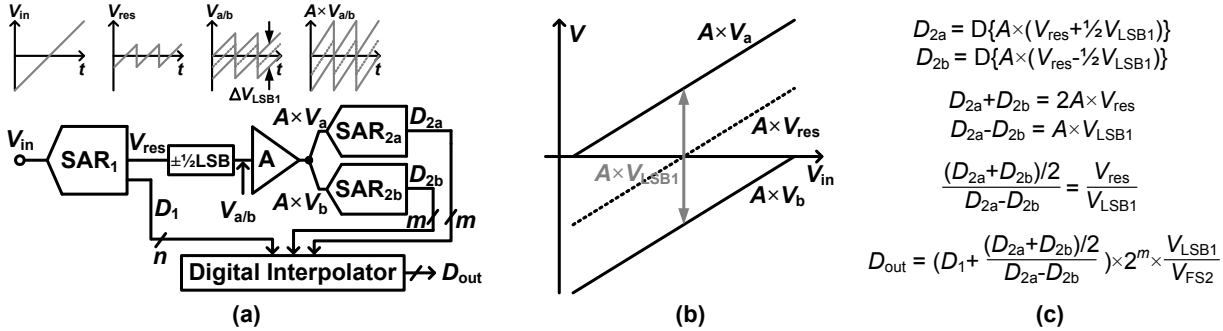

Fig. 1. Conceptual diagram of (a) the proposed digitally interpolated pipelined-SAR ADC, (b) its voltage diagram, and (c) its equations showing its insensitivity to inter-stage gain.

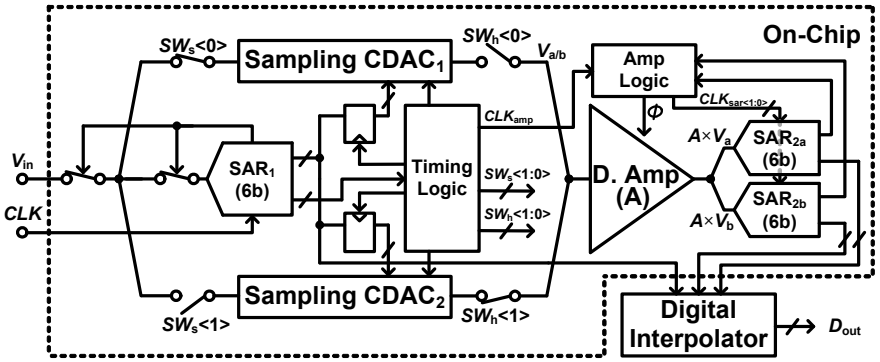

Fig. 2. Block diagram of the proposed digitally interpolated pipelined-SAR ADC using a dynamic amplifier.

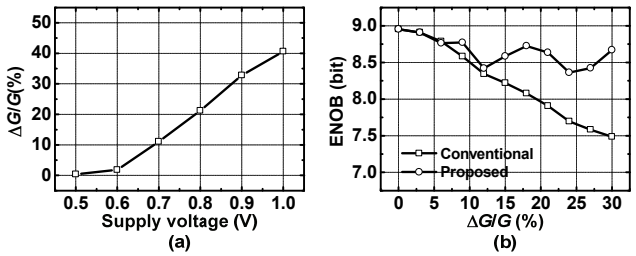

Fig. 3. Simulation results show (a) the gain variation of a dynamic amplifier over a wide range of supply voltages and (b) the robustness of proposed digital interpolation to gain variation. The fluctuation of data points for the proposed interpolation in (b) is due to rounding error of the interpolator.

following equation,

$$D_{\text{out}} = \left(D_1 + \frac{\left(D_{2\text{a}} + D_{2\text{b}}\right)/2}{D_{2\text{a}} - D_{2\text{b}}} \right) \times 2^m \times \frac{V_{\text{LSB1}}}{V_{\text{FS2}}}, \qquad (1)$$

where D_1 is the output of the first stage SAR ADC, m is the resolution of the second stage SAR ADCs, V_{FS2} is the full-scale range of the second stage SAR ADCs.

Fig. 2 shows the block diagram of the proposed ADC. A fully differential scheme is implemented; however, a single-ended figure is used in this paper for simplicity. The ADC consists of a 6-bit first stage and a 6-bit second stage with 1-bit reserved for the shifting of digital interpolation. The first stage includes a 6-bit SAR ADC, a timing logic, and two 6-bit interleaved sampling capacitive-DACs (CDACs). The sampling CDACs are designed to satisfy the noise requirement of this ADC. In order to achieve high speed, a much smaller SAR ADC is used to quantize the first 6 bits. This digital data is then transferred to one of the sampling CDACs. Using this data, the sampling CDAC generates a pair of shifted residue signals differ by V_{LSB1} for the dynamic amplifier.

In the second stage, the shifted residue signals, V_{a} and V_{b}, are amplified by the dynamic amplifier and quantized using $\text{SAR}_{2\text{a}}$ and $\text{SAR}_{2\text{b}}$, respectively. The digital interpolator combines the output data from all three SAR ADCs using (1) and cancels the channel offset to produce the final digital output. Due to the interpolation, this ADC is insensitive to the inter-stage gain error.

Fig. 3 shows the simulated gain variation of a dynamic amplifier and the robustness of the proposed digital interpolation to gain variation. For conventional pipelined-SAR ADC, 30% gain variation results in more than 2.5 bits ENOB degradation. In contrast, the proposed digitally interpolated pipelined-SAR ADC suppresses the degradation to less than 0.65 bit.

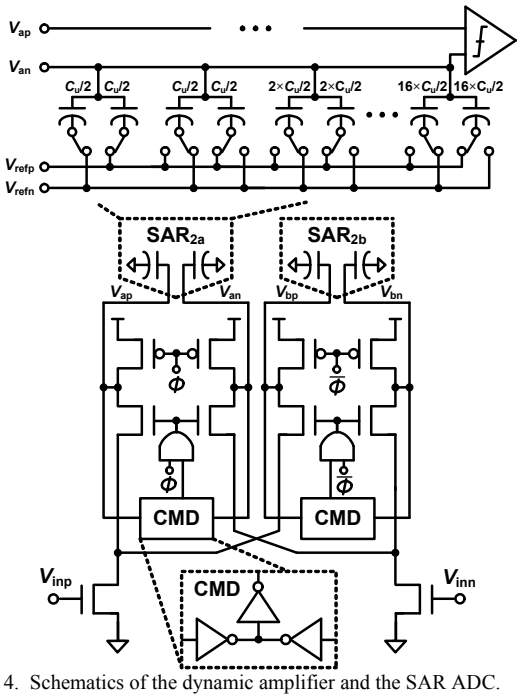

Fig. 4. Schematics of the dynamic amplifier and the SAR ADC.

B. Shared Dynamic Amplifier and SAR ADCs

With a relaxed gain requirement, an open-loop dynamic amplifier with two inverter-based common-mode detectors (CMDs) [4] is employed as the residue amplifier in this ADC to achieve high speed. The schematic of the amplifier is illustrated in Fig. 4. The amplifier is directly loaded with the second stage SAR ADCs. The gain of the amplifier is designed to approximately 4.5 times with a 0.6 V supply voltage. To ensure the gain accuracy between $D_{2\text{a}}$ and $D_{2\text{b}}$, the same pair of amplifying transistors is used to amplify the shifted residue signals, V_{a} and V_{b}.

As dynamic amplifiers are typically minimally-stacked and operate by steering charge, it is an excellent candidate for a wide range of supply voltages. Furthermore, the use of dynamic amplifier enables the proposed ADC to be fully dynamic, which makes the power consumption of this ADC clock-scalable.

As for the SAR ADCs and the sampling CDACs, they are all designed to work for nominal and ultra-low supply voltage. All CDACs are implemented using top-plate sampling for the speed advantage. Fig. 4 also shows a 6-bit SAR ADC with a 5-bit ULV CDAC. One of the main issues of a conventional CDAC with a scaled supply voltage is the high ON-resistance of the switch connecting to the common-mode voltage, V_{cm}. Although it is possible to reduce the ON-resistance using bootstrapped switches, this would significantly increase the switching power and the area. To address this issue, a capacitive interpolation technique is employed to generate a virtual V_{cm} by connecting half of the capacitance to V_{refp} and the other half to V_{refn}. Using this technique, high-speed operation can be realized even at ULV. This type of CDAC is used in the SAR ADCs and the sampling CDACs.

The comparators in the SAR ADCs are dynamic comparators [9] that are suitable for ULV high-speed operation.

III. Experimental Results

The prototype ADC is fabricated in 65 nm CMOS technology with the low threshold and the deep N-well options. The circuit functions over a range of supply voltages from 0.5 V to 1 V. The optimal supply voltage for this design is 0.6 V.

At 0.6 V, the maximum sampling frequency is 30 MS/s with a total power consumption of 481.6 μW. The breakdown of the power consumption is as follows: 108.8 μW for the analog circuits, 313.8 μW for the digital circuits including the clock buffers, and 59.0 μW for the SAR ADCs' reference. Although the digital interpolator's power is not included, layout parameter extraction (LPE) simulation shows that the expected power consumption varies from 2.1-44 μW from 0.5 V to 1 V at maximum conversion rate. At 0.6 V, the expected power is 5.3 μW at 30 MHz and the area is 17 μm×126 μm.

Fig. 5 shows the measured DNL and INL of a 1 kHz ramp input sampled at 30 MS/s at 0.6 V. The DNL and INL are +0.81/-0.40 LSB and +0.69/-0.85 LSB, respectively.

Fig. 6 illustrates the measured dynamic performance from 0.6 V to 1 V. The optimal result is measured at 0.6 V. The measured SNDR remains higher than 53.5 dB up to 30 MS/s with a 1 MHz sinusoid input. The effective resolution bandwidth (ERBW) is up to 15 MHz with a SNDR higher than 49.2 dB. This results in a FoM of 68 fJ/conv.-step at 0.6 V.

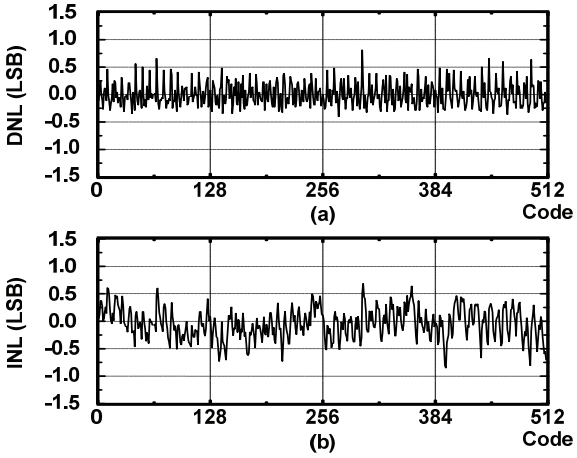

Fig. 5. Measured (a) DNL and (b) INL with a supply voltage of 0.6 V.

Fig. 7 shows the effectiveness of the digital interpolation. The prototype ADC is designed to operate in two modes: with the proposed digital interpolation or with an external gain adjustment. Both modes are optimized at 0.6 V. By increasing the supply voltage up to 1 V, the proposed method has a SNR around 4 dB higher than that of the conventional pipelined-SAR ADC due to its insensitivity to inter-stage gain variation.

The FFT of the measured results are presented in Fig. 8. The main causes of the ENOB degradation for this ADC are the noise in the second stage SAR ADCs and a tone caused by interleaving. In contrast, the spur caused by the third-order harmonic is around 69.1 dB with a 1 MHz input and 65.9 dB with a 14 MHz input signal. This demonstrates that the proposed digitally interpolated pipelined-SAR ADC using a dynamic amplifier is a promising candidate to achieve moderate-resolution high-speed data conversion in an ULV environment.

Fig. 9 shows the chip photo of the prototype ADC occupying a total area around 0.11 mm^2. The performance comparison with other state-of-the-art ULV ADCs are listed in Table I and presented in Fig. 10. Several published pipelined-SAR ADCs are not included in the comparison as this work targets on ULV ADC design.

V. Conclusion

In conclusion, this paper presents an ULV moderate-resolution high-speed pipelined-SAR ADC using a dynamic amplifier and digital interpolation. The proposed interpolation allows the pipelined-SAR architecture to become insensitive to the inter-stage gain while the dynamic amplifier makes the design clock-scalable and robust to supply voltage scaling. These techniques together enable a fully dynamic 0.5-to-1 V, 9-bit, 15-to-90 MS/s ADC.

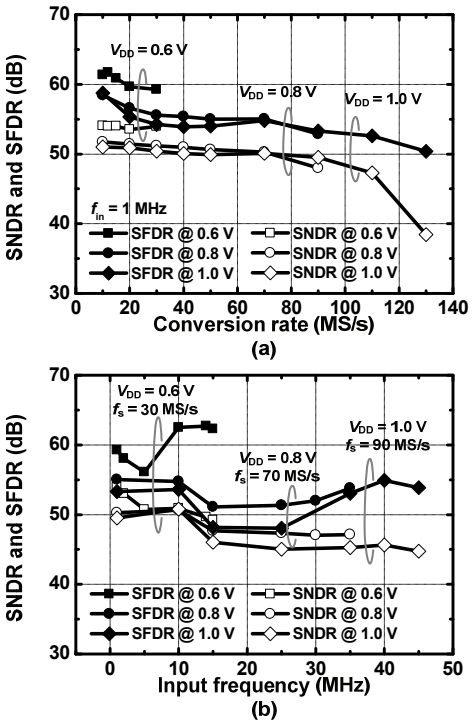

Fig. 6. Measured SNDR and SFDR vs. (a) conversion rate and (b) input frequency from 0.6 V to 1.0 V.

TABLE I: PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART ULTRA-LOW-VOLTAGE MODERATE-RESOLUTION HIGH-SPEED ADCS

	[2]	[3]	[4]	[10]				This work			
Architecture	SAR	SAR	Pipe.	Pipeline				Pipelined-SAR			
Resolution (bit)	10	10	7	12				9			
Supply voltage (V)	0.6	0.45	0.55	0.5	0.6	0.8	1.0	0.5	0.6	0.8	1.0
Conversion rate (MS/s)	2.5	0.2	160	5	10	30	50	**15**	**30**	**70**	**90**
Power consumption (mW)	0.005	0.000084	2.43	0.24	0.56	1.61	4.07	0.20	0.48	1.92	3.14
ENOB (bit)	9.04	8.95	6.0	10.7	10.8	10.8	11.0	7.63	7.88	7.54	7.14
FoM (fJ/c.-s.)	3.8	0.85	240	28.0	30.9	31.1	41	67	68	148	247
Technology (nm)	90	40	90	65				65			
Active area (mm^2)	0.042	0.0065	0.25	0.36				0.11			

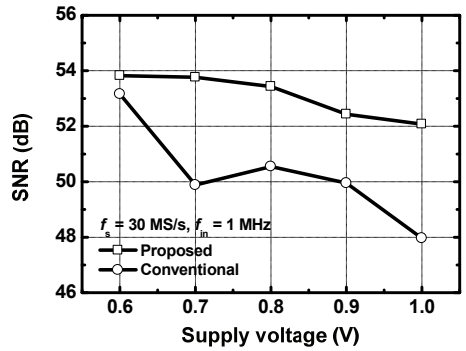

Fig. 7. Measured SNR vs. supply voltage of the proposed digital interpolation and the conventional pipelined-SAR ADC with an external inter-stage gain adjustment.

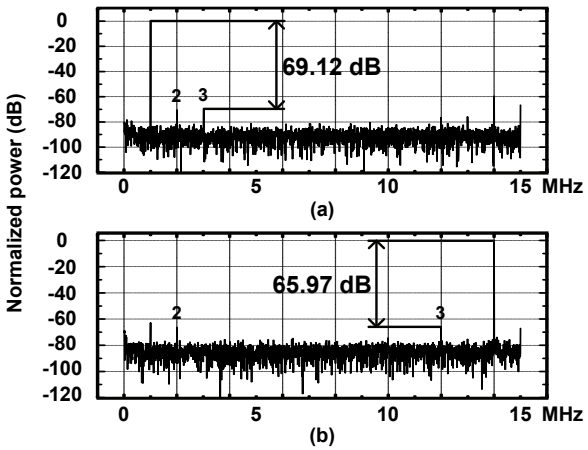

Fig. 8. FFT of the measured results with (a) 1 MHz and (b) 14 MHz input sampled at 30 MS/s (4096 data points).

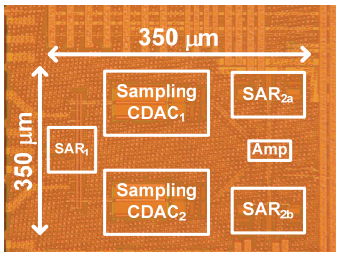

Fig. 9. Chip photo of the prototype ADC.

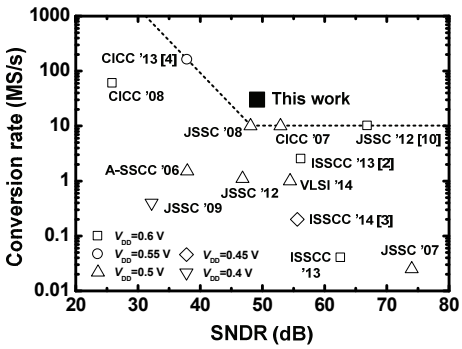

Fig. 10. Performance comparison chart showing the state-of-the-art ULV ADCs.

ACKNOWLEDGMENT

This work was partially supported by NEDO, MIC, CREST in JST, STARC, Huawei, Berkeley Design Automation for the use of the Analog FastSPICE(AFS) Platform, and VDEC in collaboration with Cadence Design Systems, Inc.

REFERENCE

[1] International Technology Roadmap for Semiconductors. 2013. [Online]. Available: http://www.itrs.net/

[2] C.-Y. Liou, *et al.*, "A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90nm CMOS," in *IEEE ISSCC*, pp. 280-281, Feb. 2013.

[3] H.-Y. Tai, *et al.*, "A 0.85fJ/conversion-step 10b 200kS/s subranging SAR ADC in 40nm CMOS," in *IEEE ISSCC*, pp. 196-197, Feb. 2014.

[4] J. Lin, *et al.*, "A 0.55 V 7-bit 160 MS/s interpolated pipeline ADC using dynamic amplifiers," in *IEEE CICC*, pp. 1-4, Sep. 2013.

[5] S.-H. W. Chiang, et al., "A 10-Bit 800-MHz 19-mW CMOS ADC," *IEEE J. of Solid-State Circuits,* vol. 49, no. 4, pp. 935-949, Apr. 2014.

[6] J. Zhong, *et al.*, "Inter-stage gain error self-calibration of a 31.5fJ 10b 470MS/S pipelined-SAR ADC," in *IEEE A-SSCC*, pp. 153-156, Nov. 2012.

[7] B. Verbruggen, *et al.*, "A 2.1 mW 11b 410 MS/s dynamic pipelined SAR ADC with background calibration in 28nm digital CMOS," in *Symp. on VLSI Circuits*, pp. C268-C269, Jun. 2013.

[8] F. van der Goes, *et al.*, "A 1.5mW 68dB SNDR 80MS/s 2×interleaved SAR-assisted pipelined ADC in 28nm CMOS," in *IEEE ISSCC*, pp. 200-201, Feb. 2014.

[9] M. Miyahara, *et al.*, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *IEEE A-SSCC*, pp. 269-272, Nov. 2008.

[10] S. Lee, *et al.*, "A 12 b 5-to-50 MS/s 0.5-to-1 V voltage scalable zero-crossing based pipelined ADC," *IEEE J. of Solid-State Circuits*, vol. 47, no. 7, pp. 1603-1614, Jul. 2012.