A 0.011mm^2 PVT-Robust Fully-Synthesizable CDR with a Data Rate of 10.05 Gb/s in 28nm FD SOI

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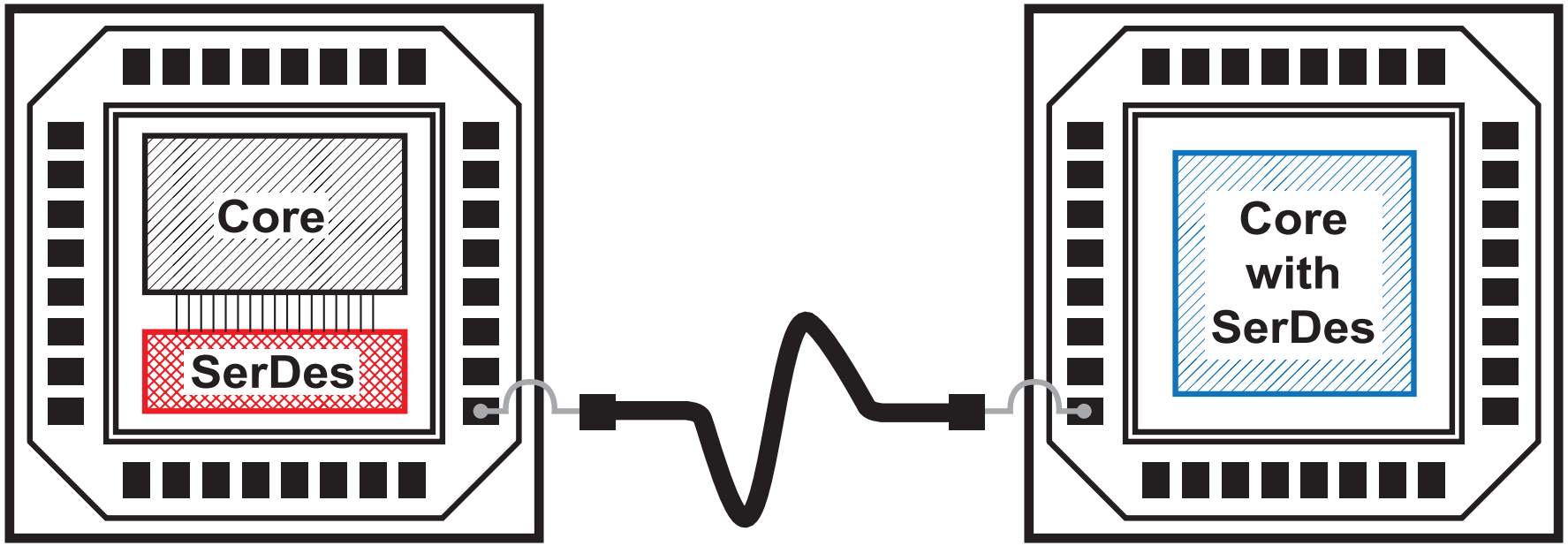
Outline

- Motivation
- Architecture for Synthesis
  - Edge Injection
  - Interpolative Phase-Coupled DCO
  - Standard Cell I-DAC
  - PVT Calibration
- Measurement Results
- Summary

Motivation

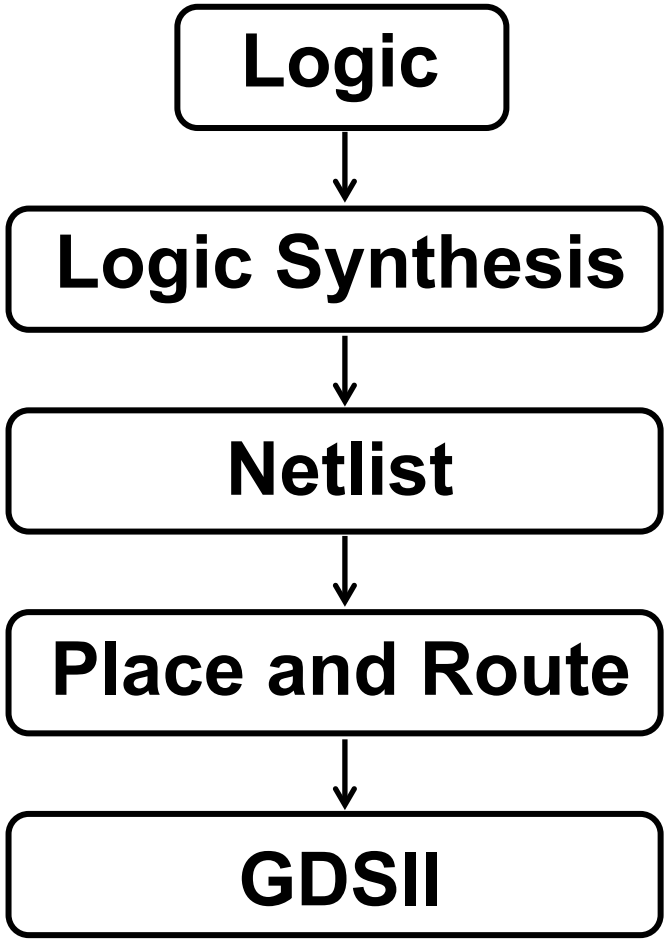


Chip-to-chip serial data link

Synthesizable CDR

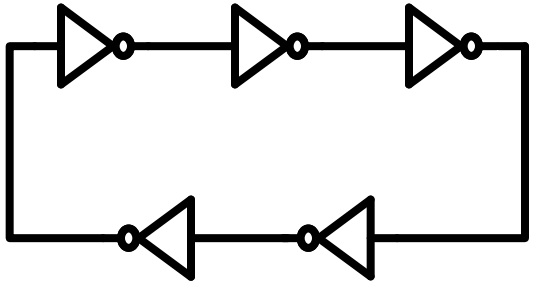
- **Co-Synthesizable with digital core.**
- **Scalable.**
- **Portable.**

Advantages of Synthesis

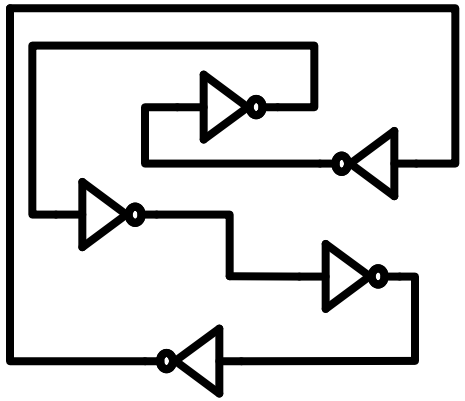


High level of automation saves precious resources

Issue: Layout Uncertainty



Ideal placement

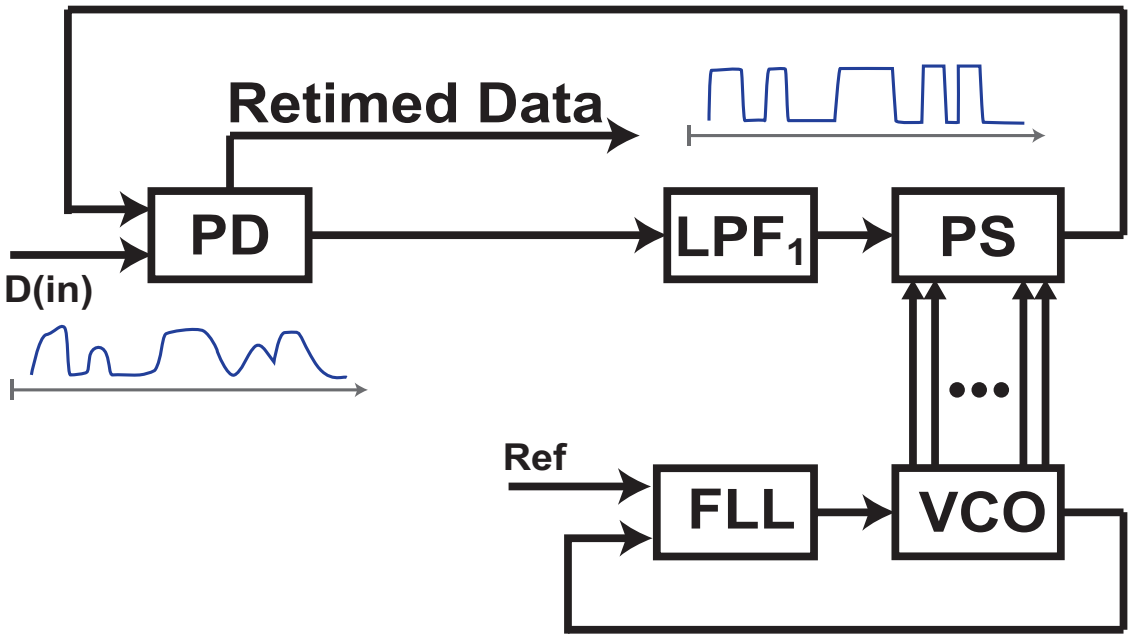


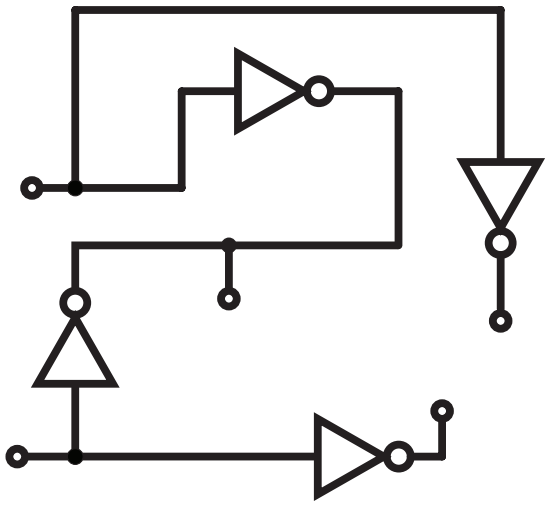
Actual placement

➔No layout symmetry

- Unbalanced layout degrades system performance.

Conventional Architectures





Unbalanced P&R

A new analog-circuit architecture is required, which tolerates layout impairment/uncertainty.

[M. Loh, *et. al.*, VLSI 2010]
[H. Pan, *et. al.*, ISSCC 2011]

Conventional Architectures

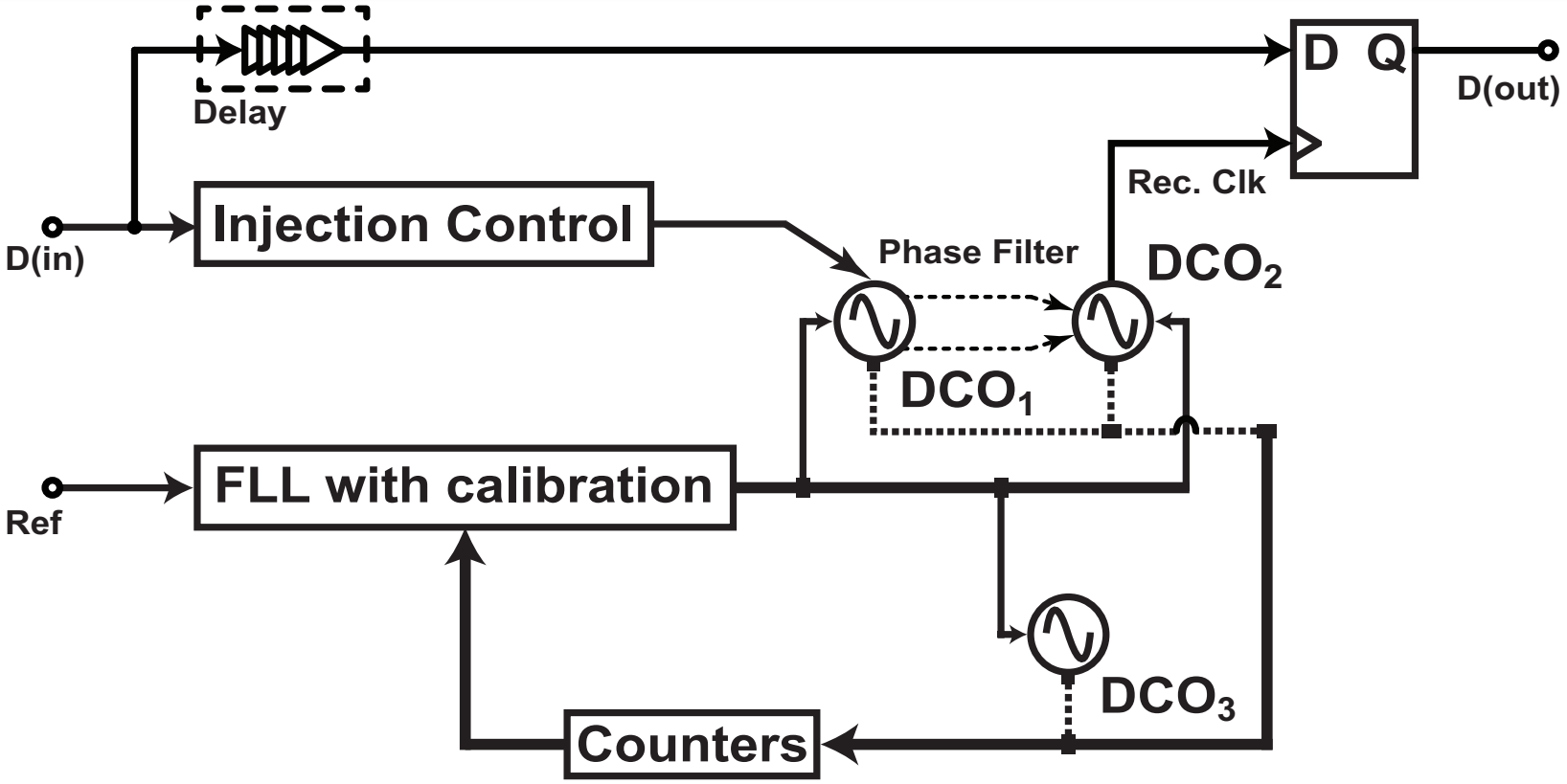
- **Architecture for synthesis must be minimally affected by layout variations.**

Topology	PLL-CDR	DLL-CDR	PI-CDR	IL-CDR
Jitter Peaking	Yes	Yes*	No	No
Locking Time	Slow	Moderate	Moderate	Fast
Frequency Range	Wide	Wide	Limited	Wide
Capture Range	Wide	Limited	Limited	Wide
Synthesizability	No*	No*	No*	**Yes**

IL-CDR is a viable candidate for synthesis

*[Edward Lee, *et. al.*, JSSC 2003]

Architecture for Synthesis



- Injection control ➡ Edge Injection
- DCO ➡ Interpolative phase coupled
- Coarse tuning ➡ I-DAC

[J. Lee, *et. al.*, JSSC 2008

Outline

- Motivation
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  - **Edge Injection**
  - Interpolative Phase-Coupled DCO
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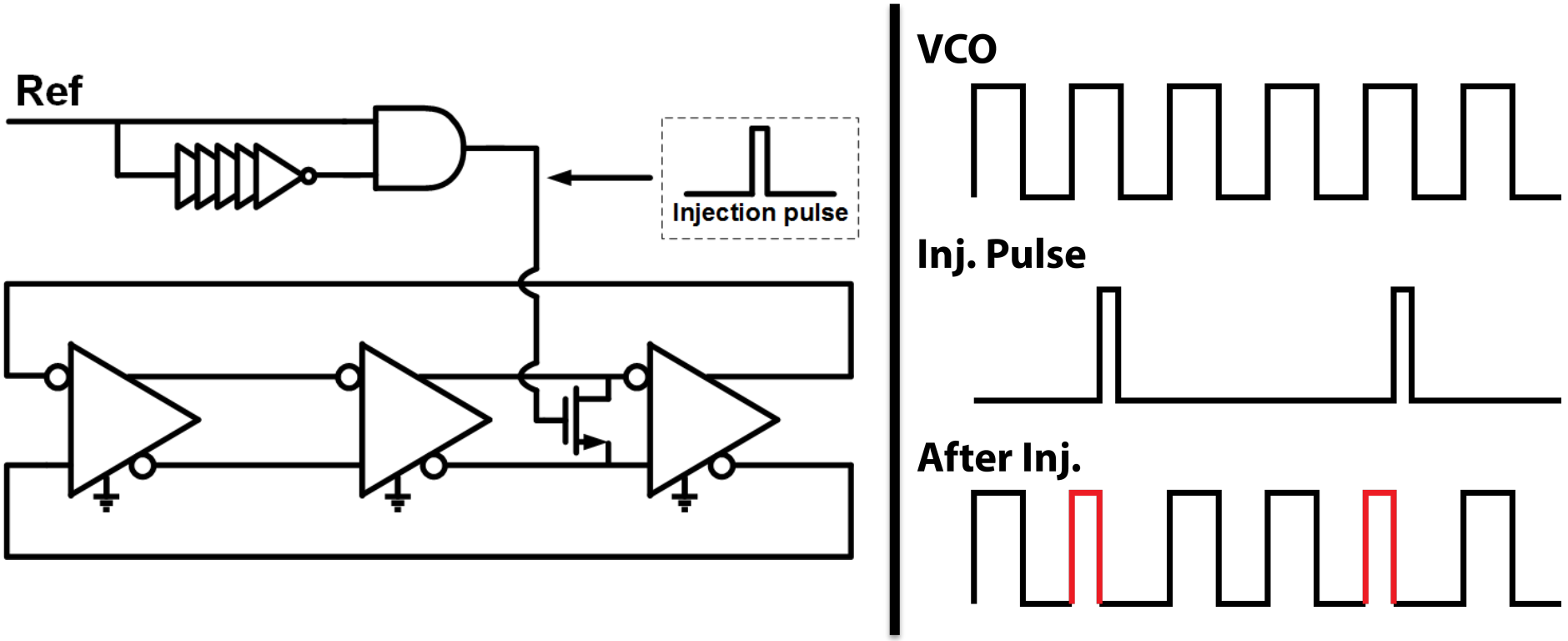
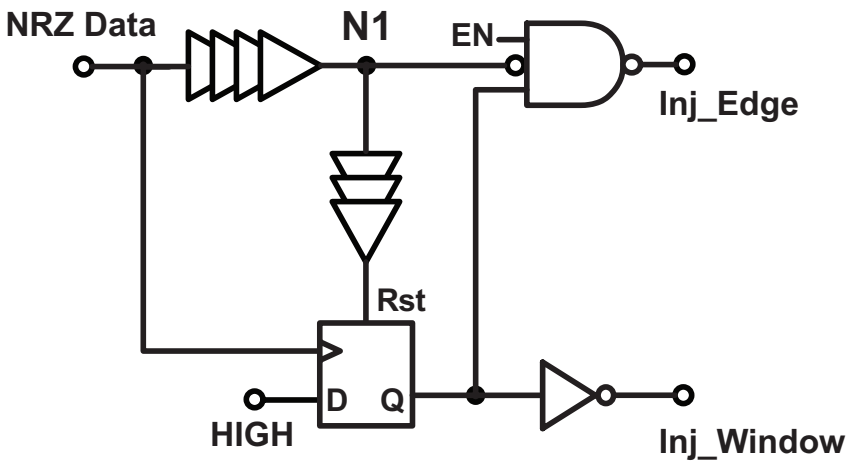
Conventional Pulse Injection

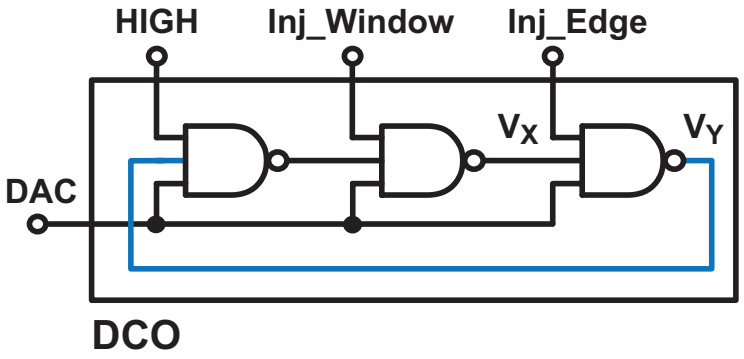


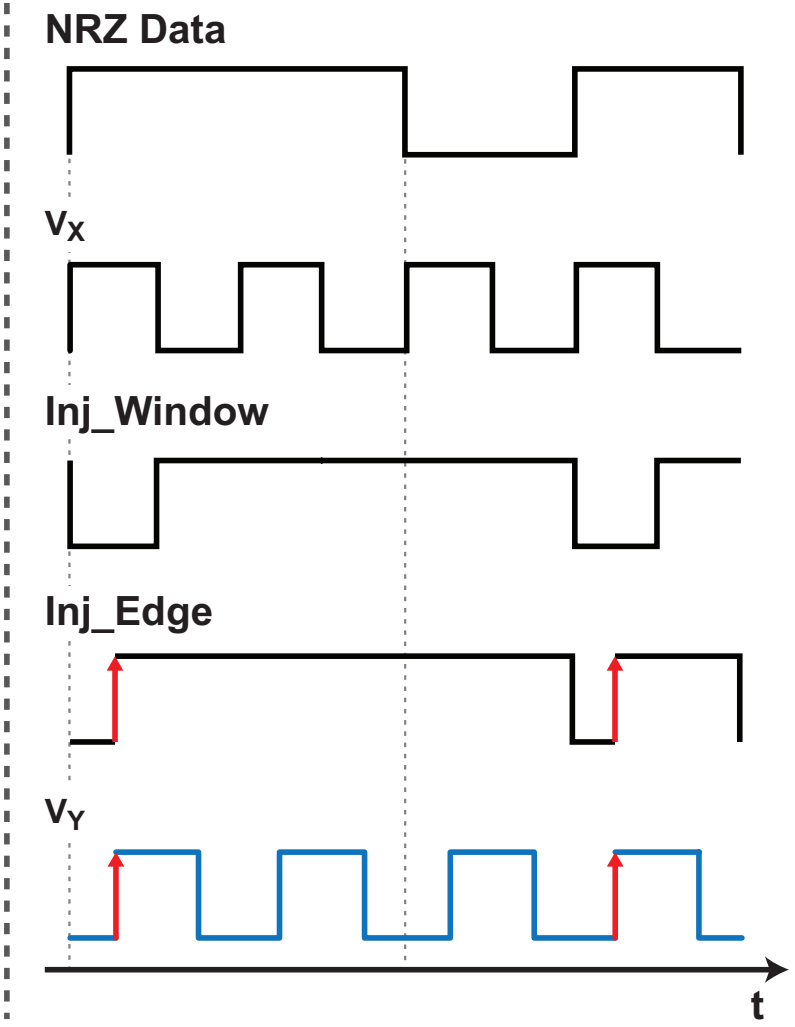
- Stringent timing constraints on inj. pulse width.
- Reduced pulse width stress down-stream circuitry.

[Hiok, *et. al.*, JSSC 2013]

Edge Injection



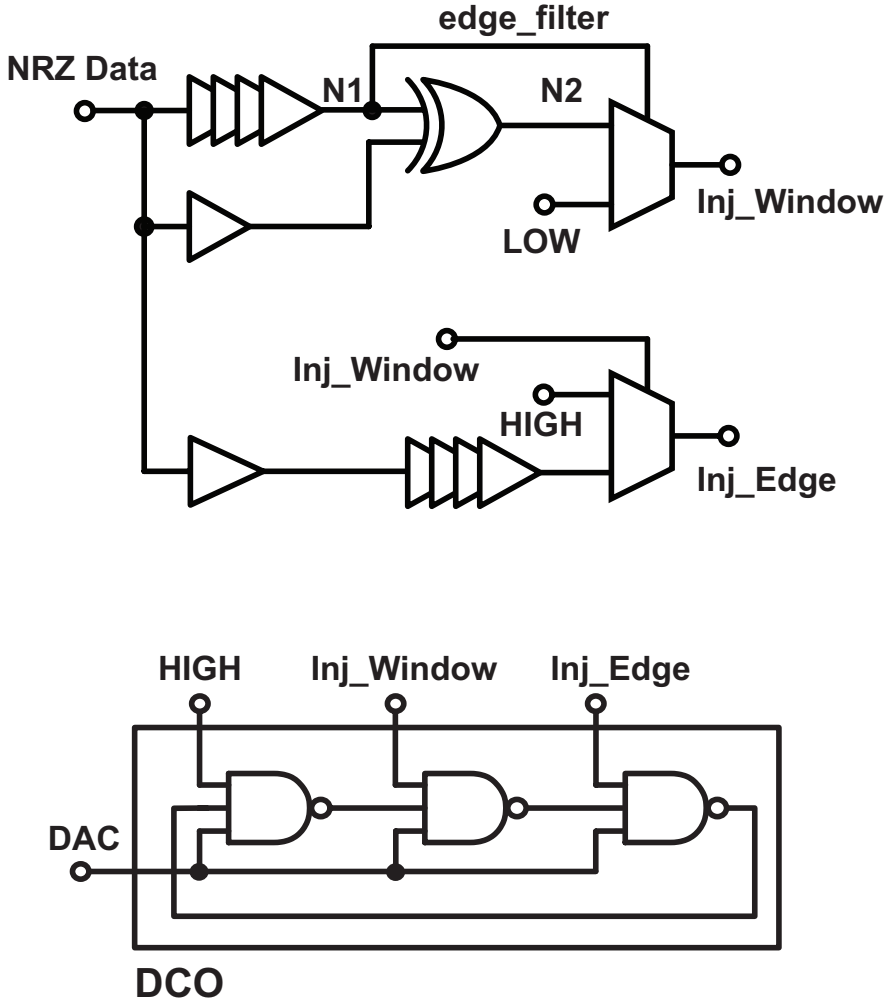


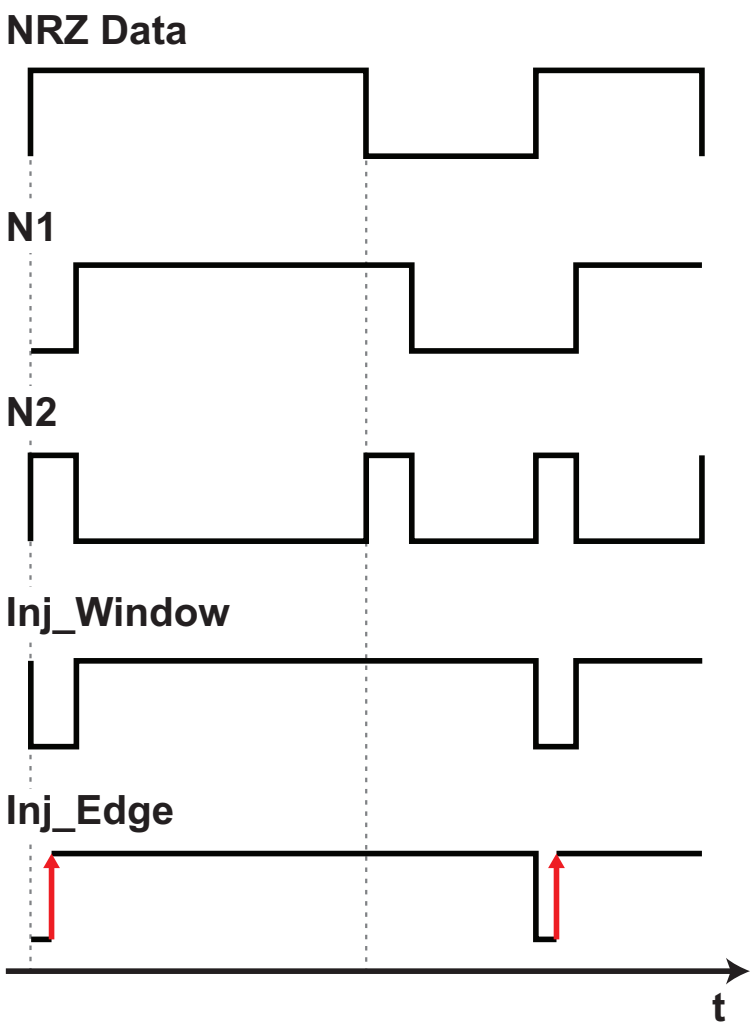


➢ **Waveform distortion is eliminated.**

[Deng, *et. al.*, JSSC 2014]

Edge Injection *Contd.*





- **Improved circuitry for enhanced operation speed.**

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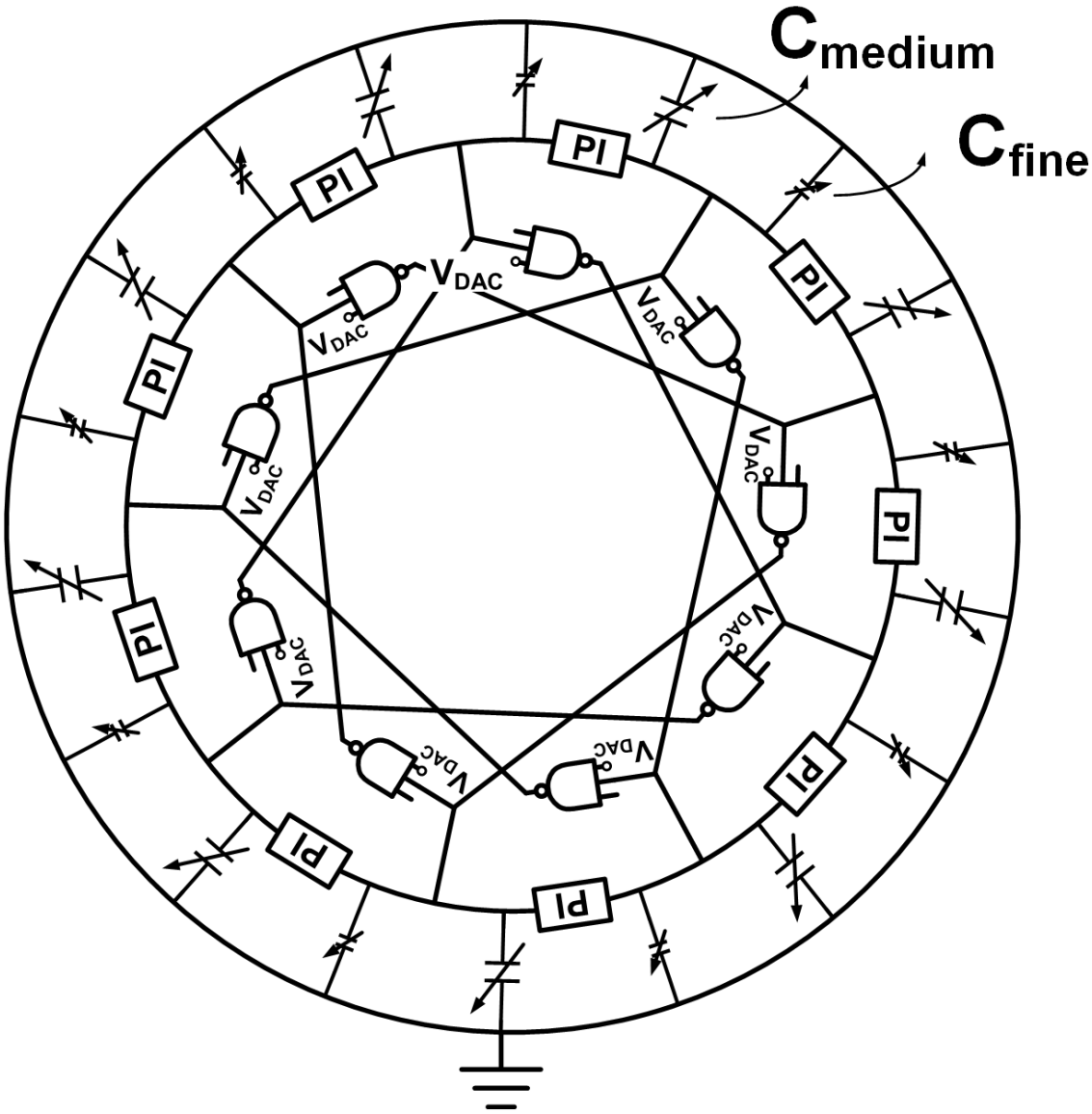
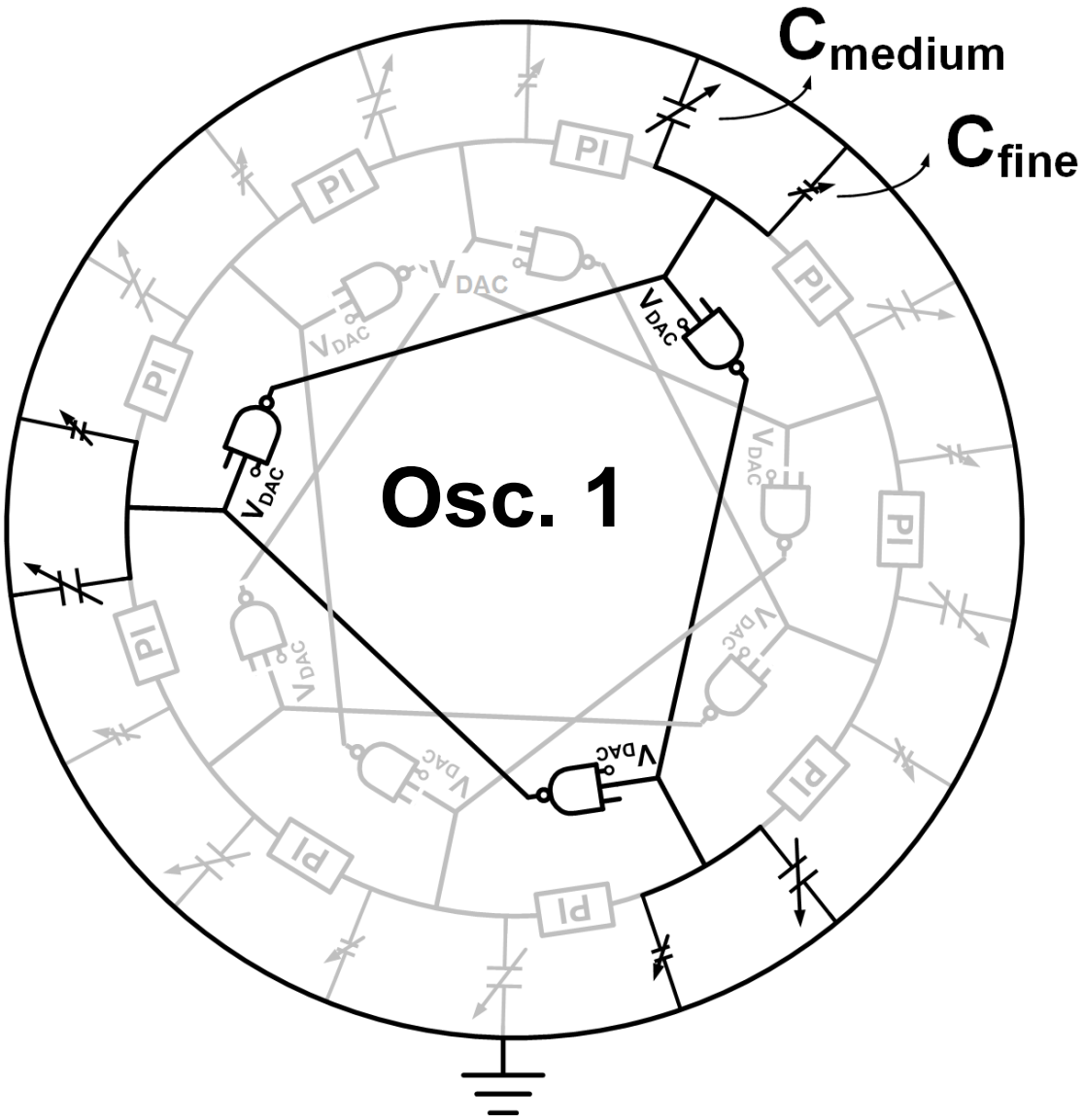
Block Diagram of DCO

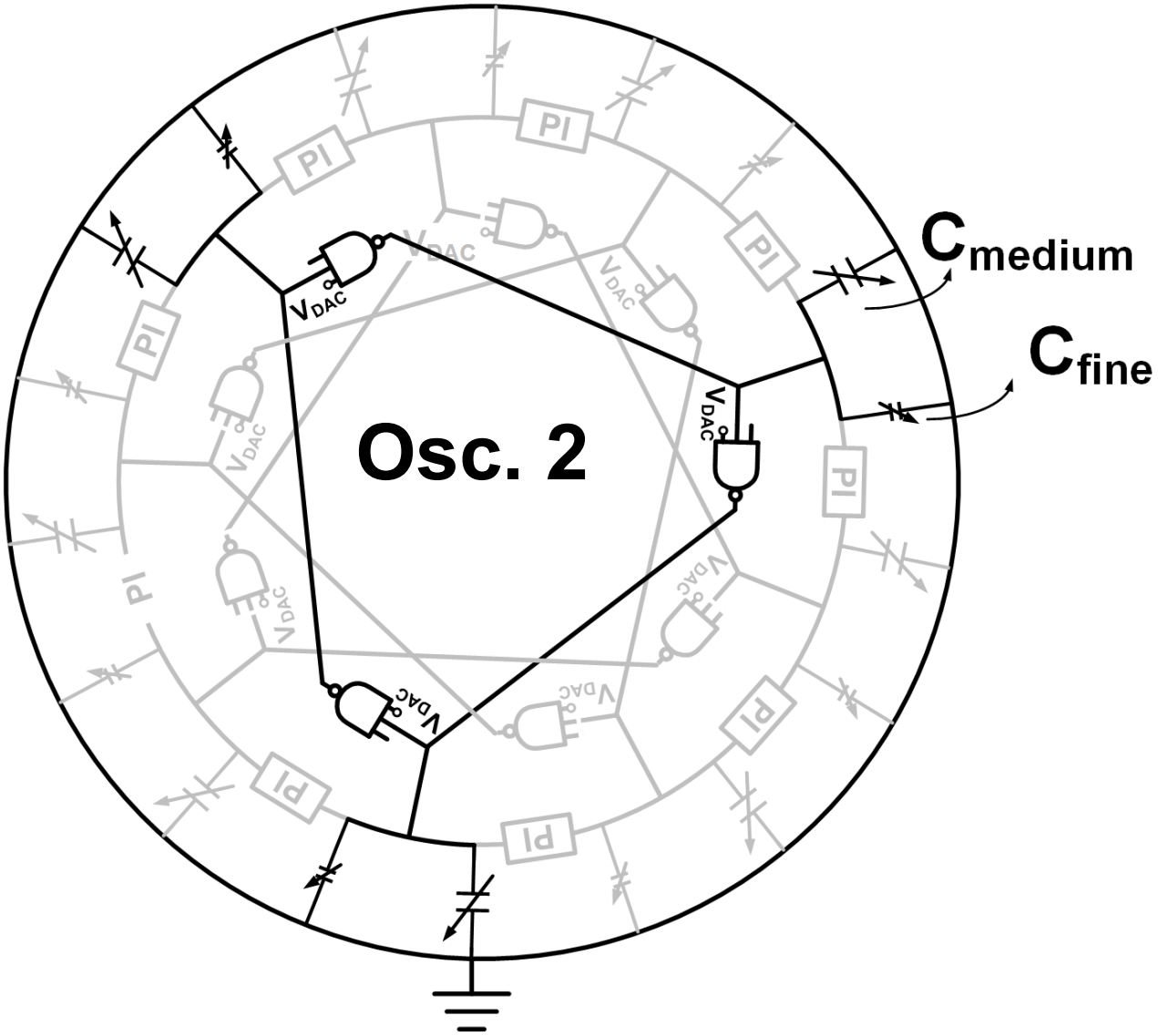


[A. Matsumoto, *et al.*, JSSC 2008]

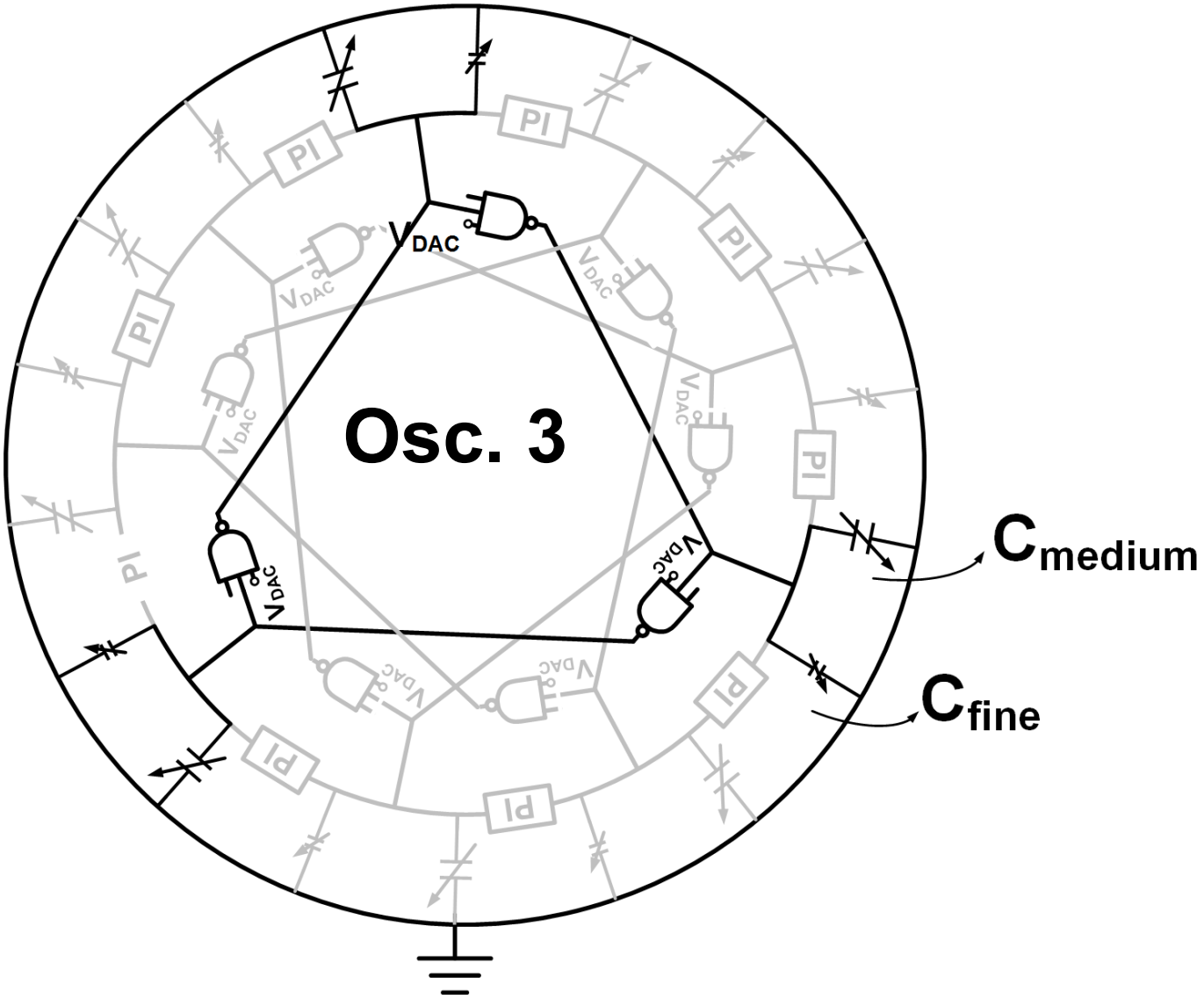
Block Diagram of Oscillator 1



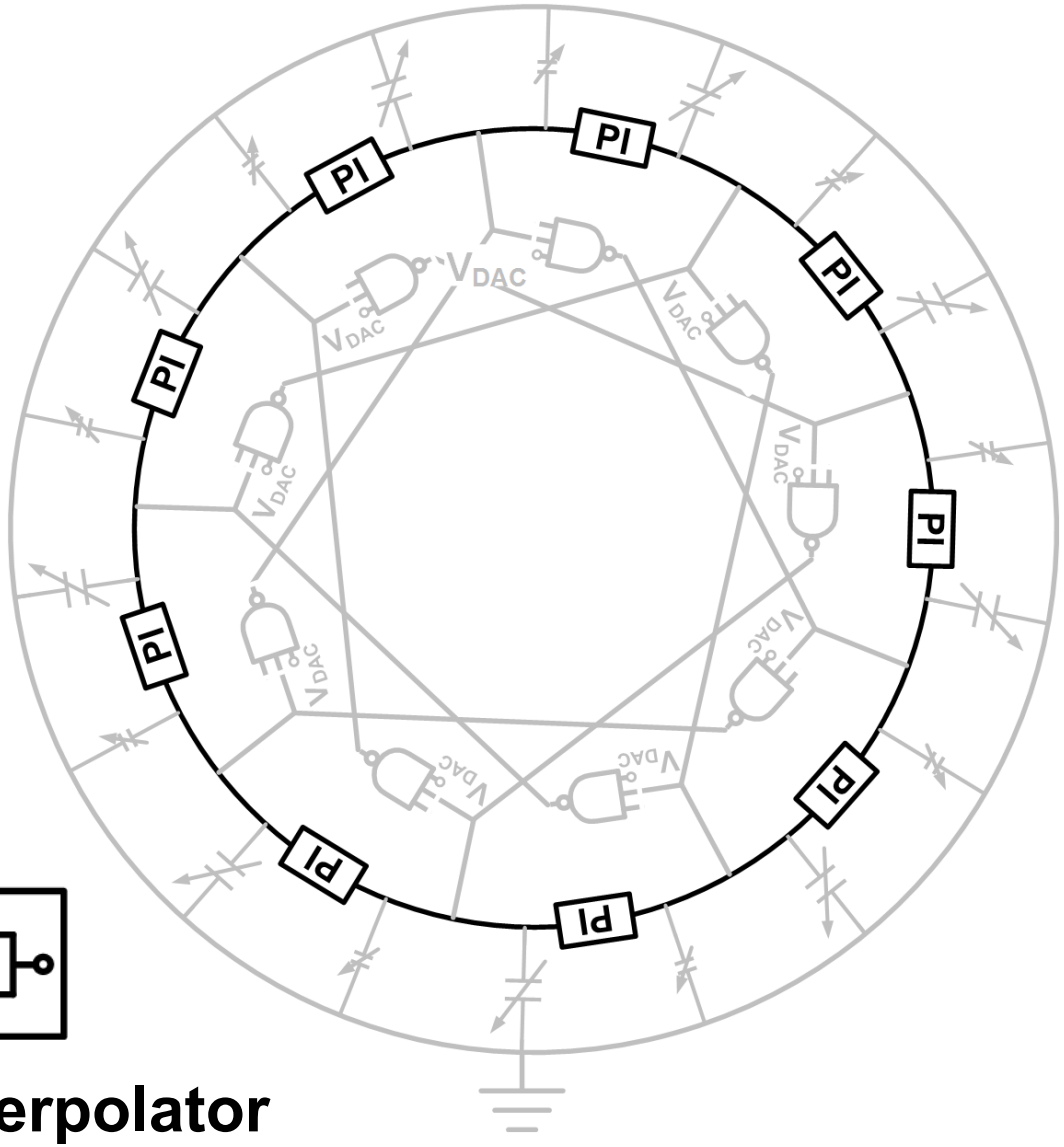
Block Diagram of Oscillator 2

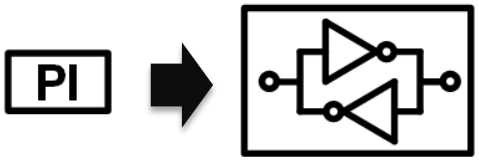


Block Diagram of Oscillator 3



Interpolative Phase-coupled Ring





PI: Phase Interpolator

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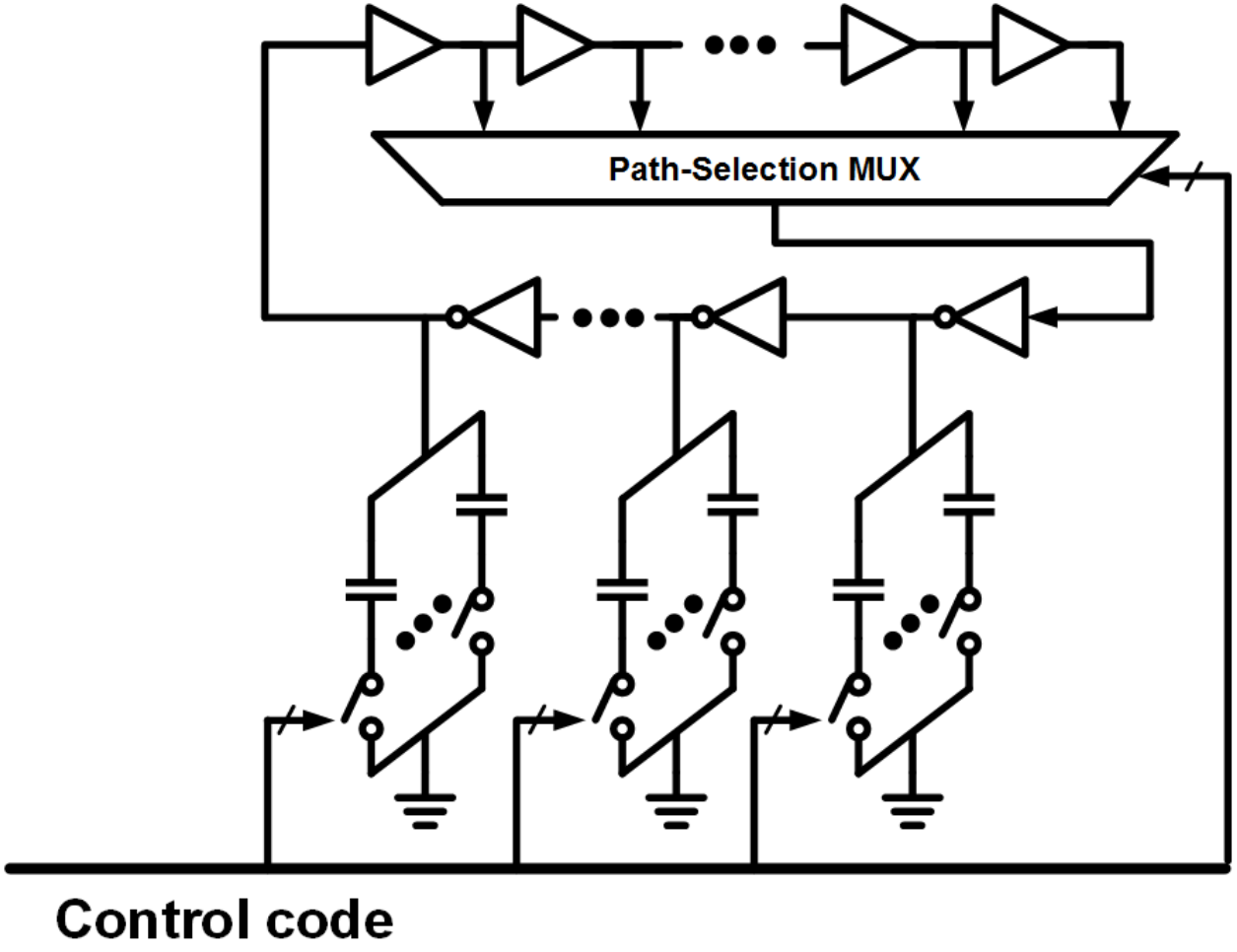
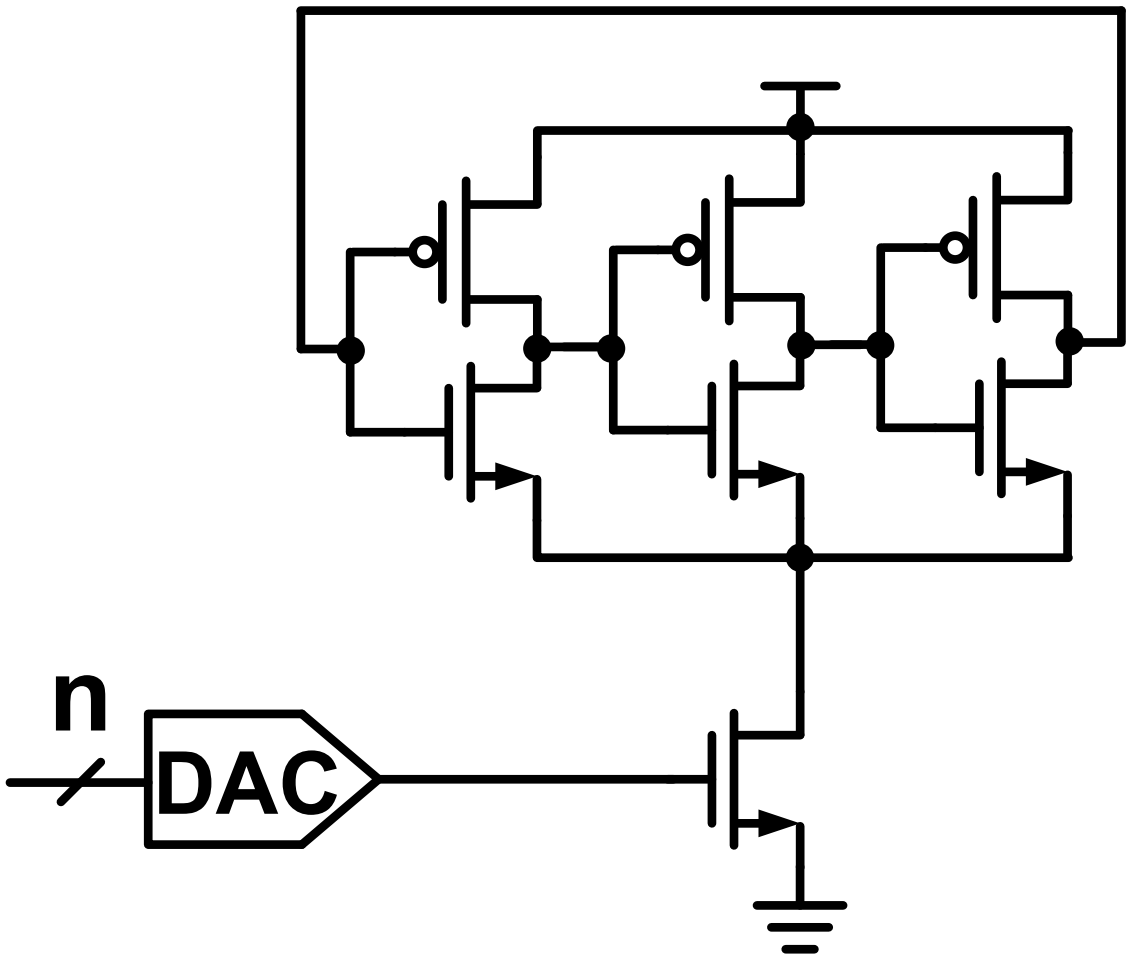
Conventional Coarse Tuning



- Unequally loaded stages.

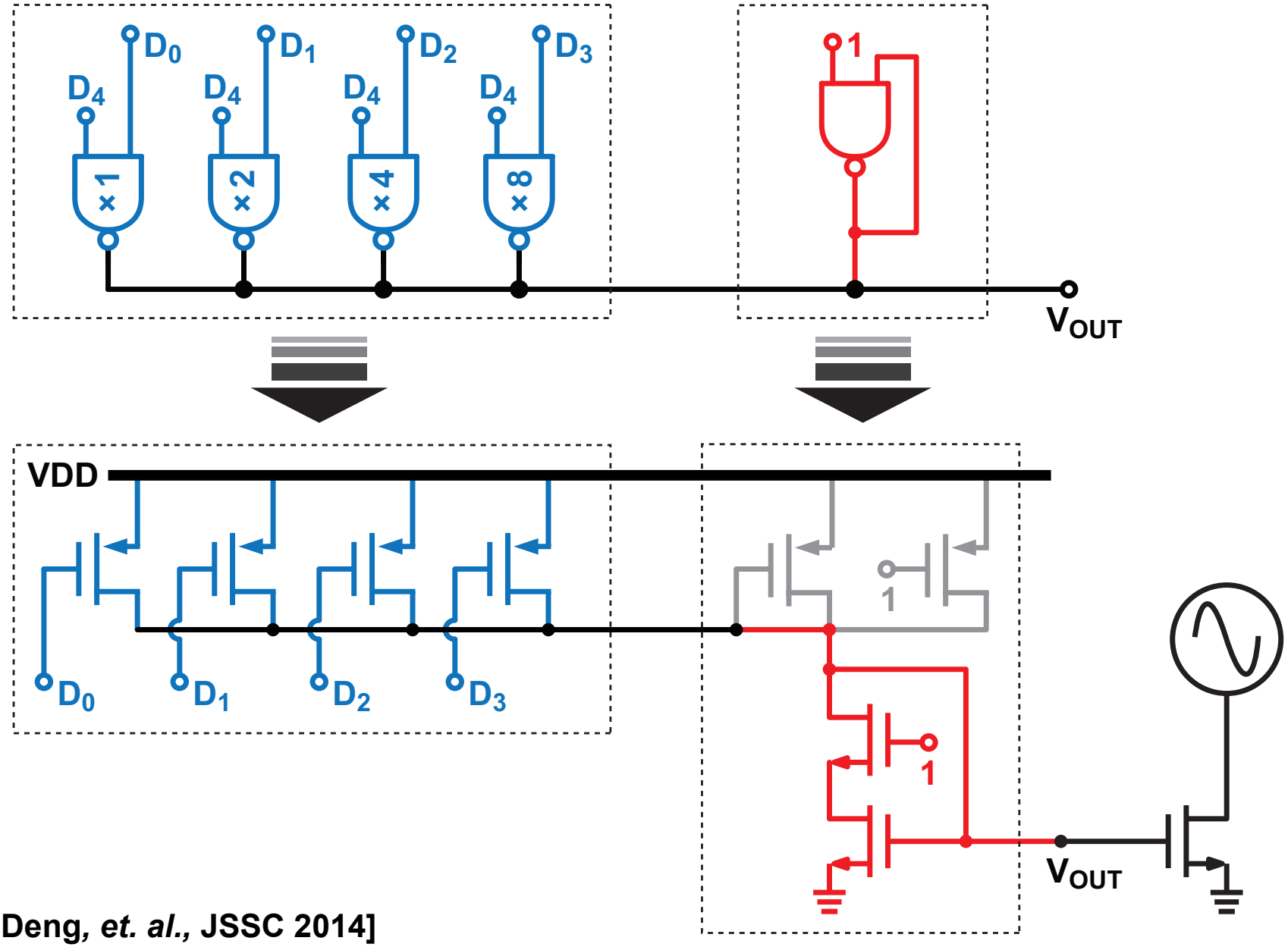
[D. Sheng, *et al.*, TCAS II 2007]

Coarse Tuning Using DAC



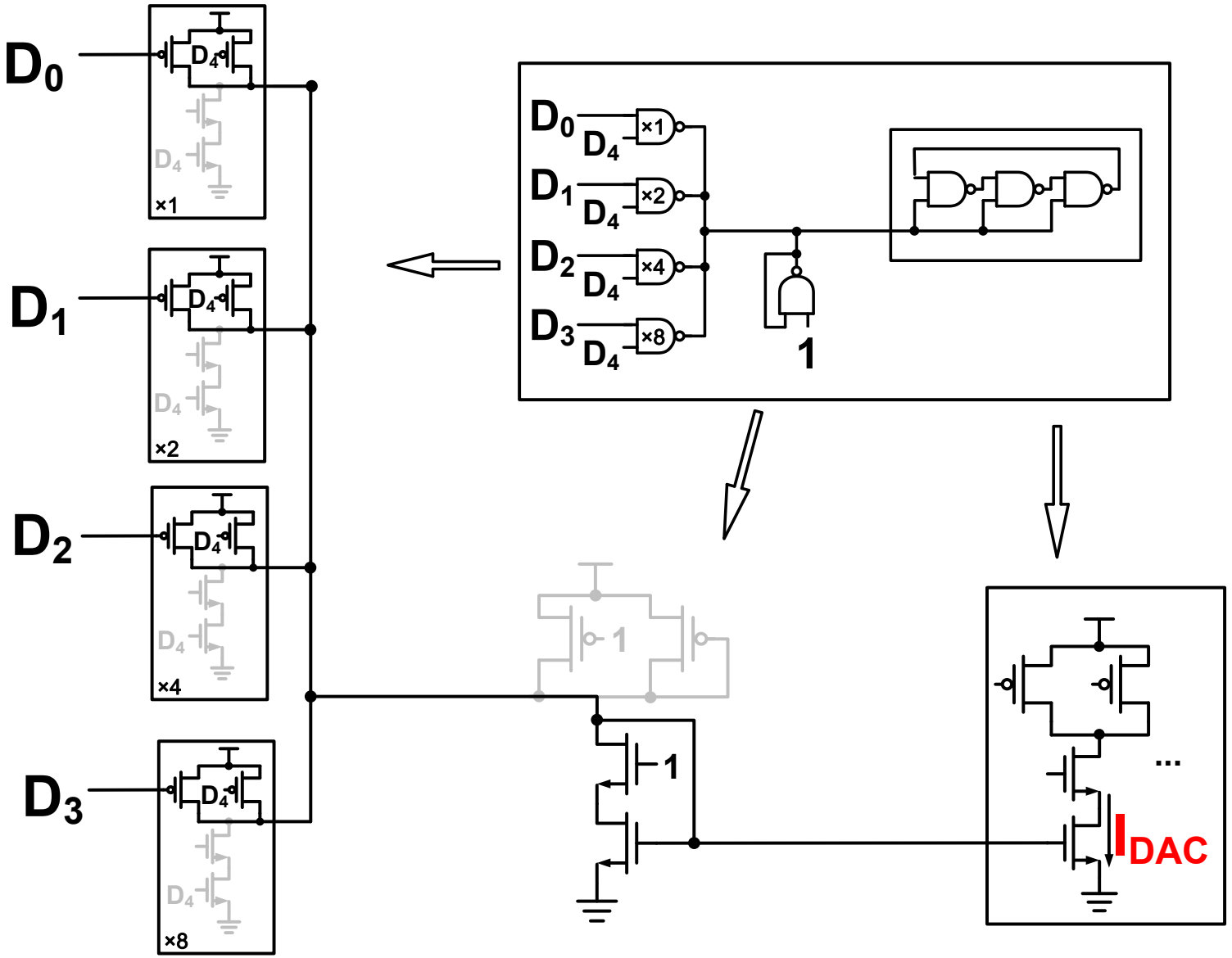
- Loading is equalized.

I-Linear DAC



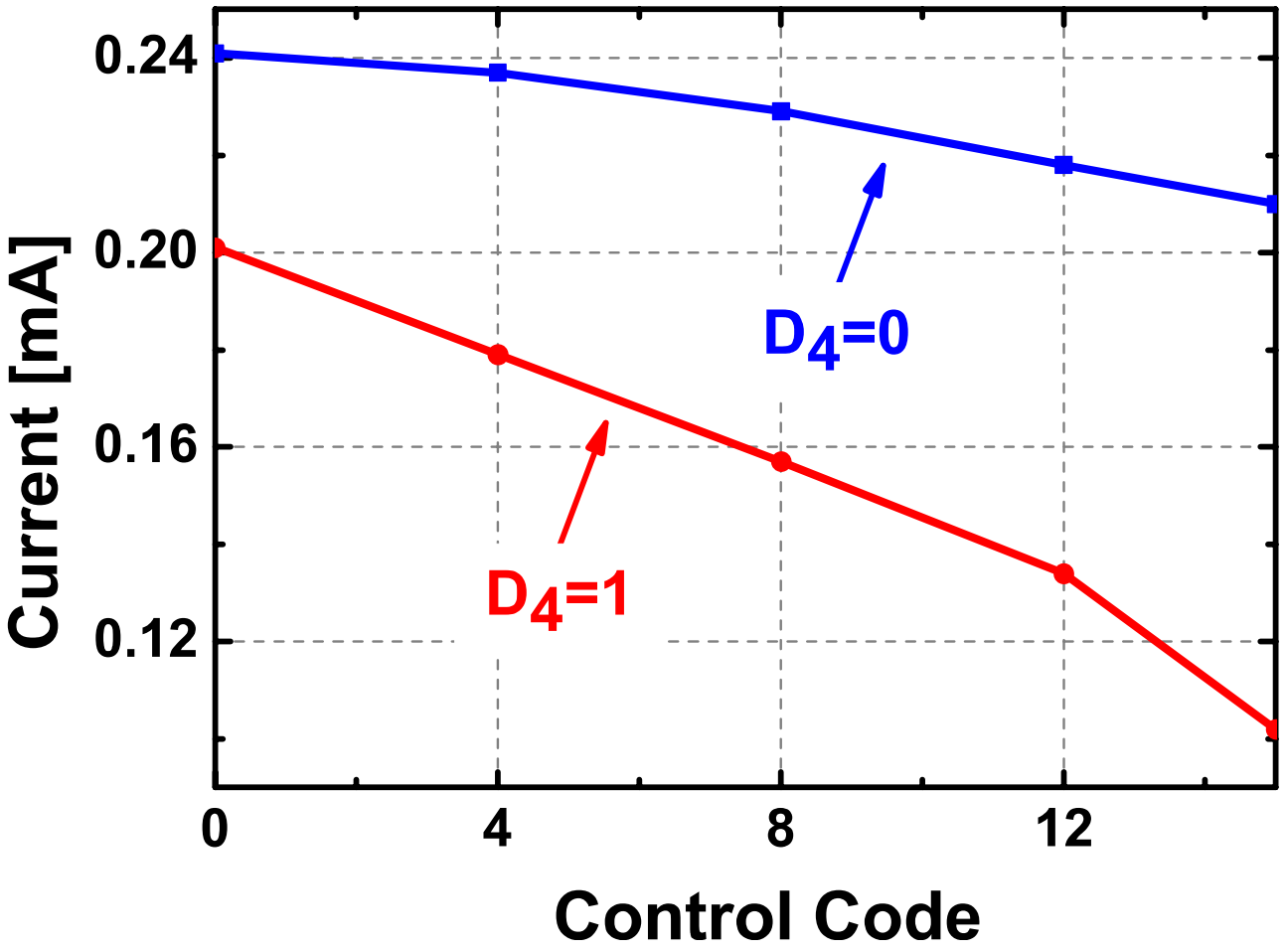
[W. Deng, *et. al.*, JSSC 2014]

I-Linear DAC *Cont.*



[W. Deng, *et. al.*, JSSC 2014]

Simulation Results



- Approximately 2GHz tuning range is achieved in simulation using the I-linear DAC

Outline

- Motivation
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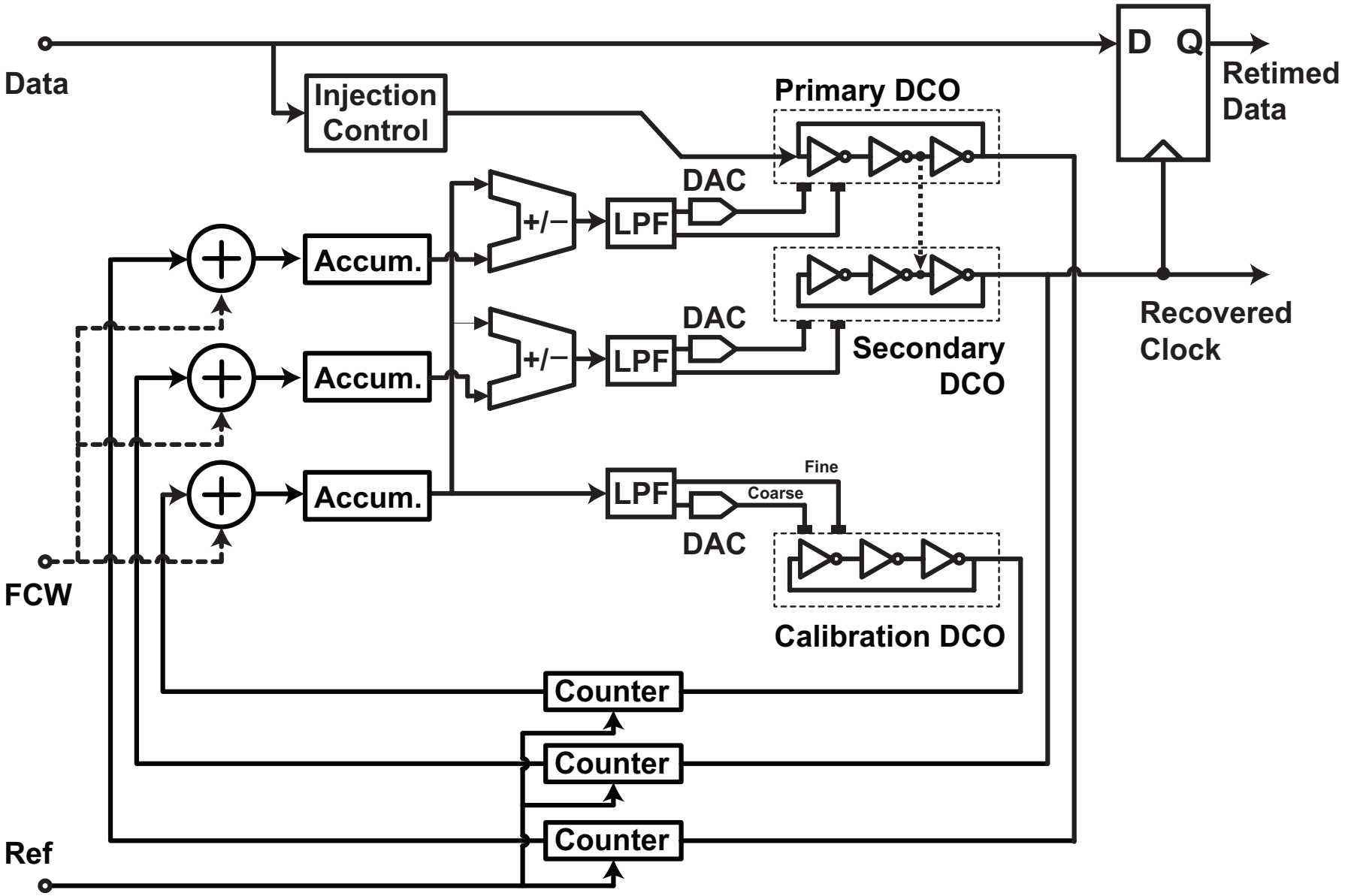
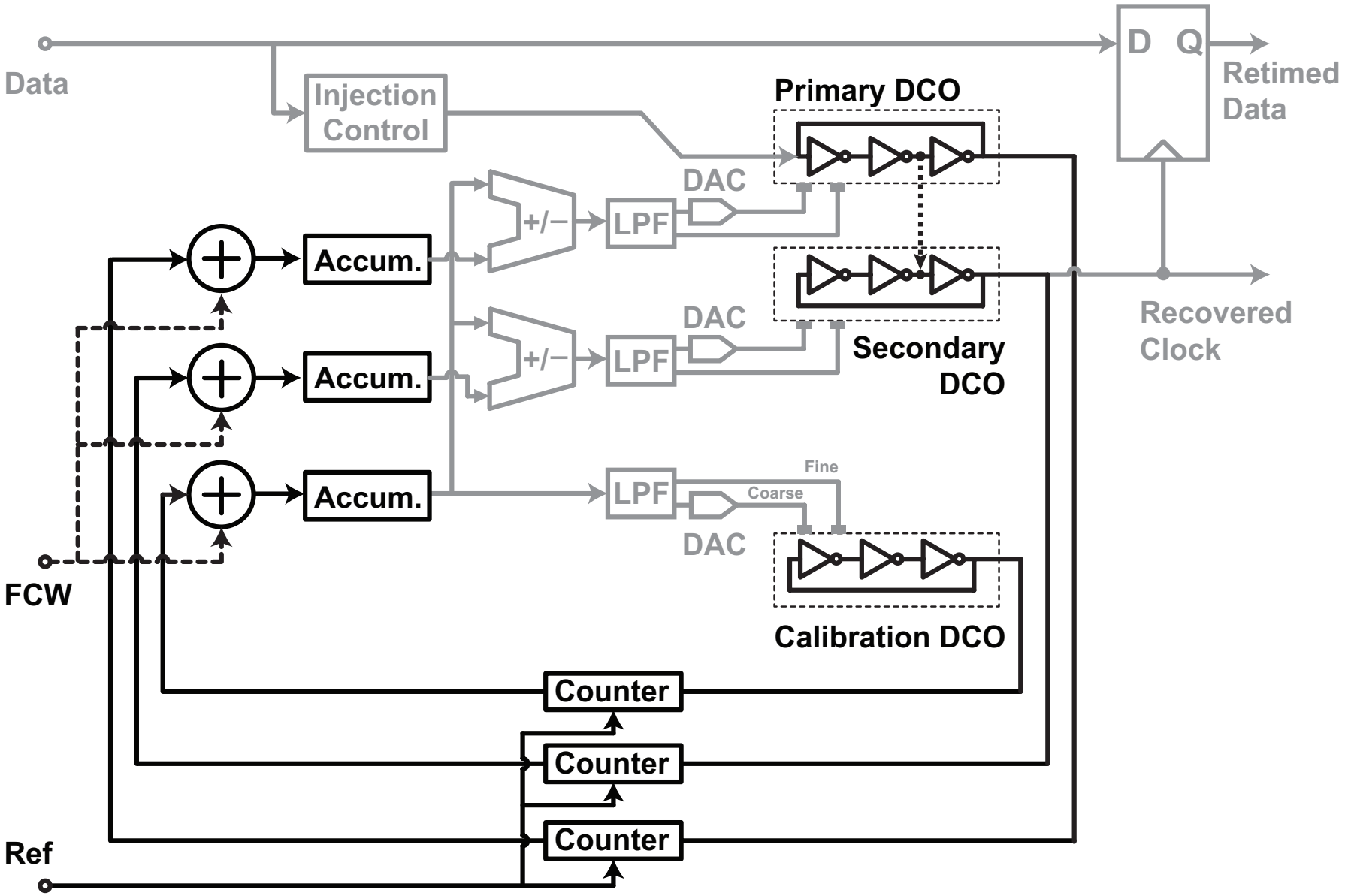
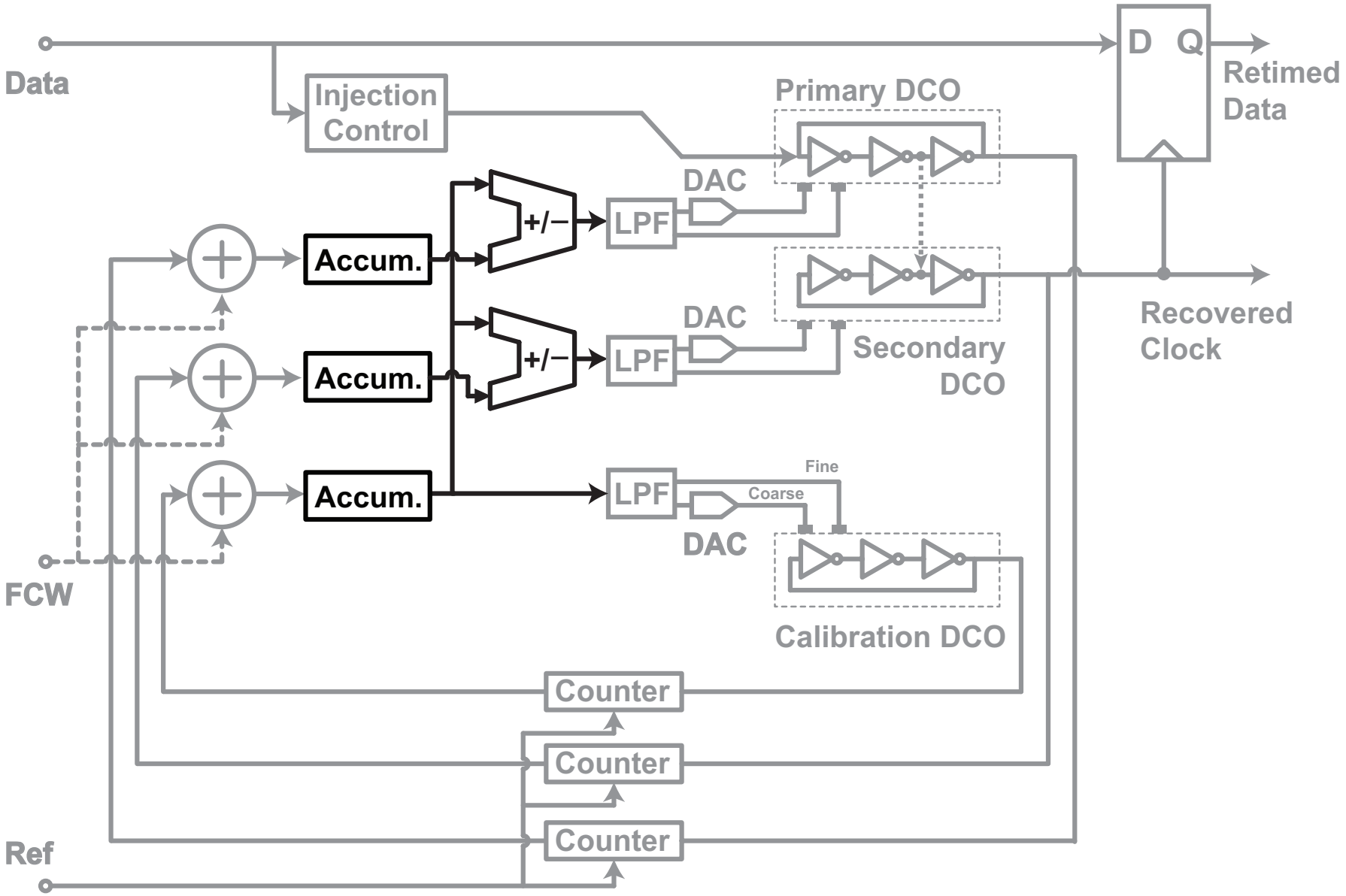
Complete Block Diagram



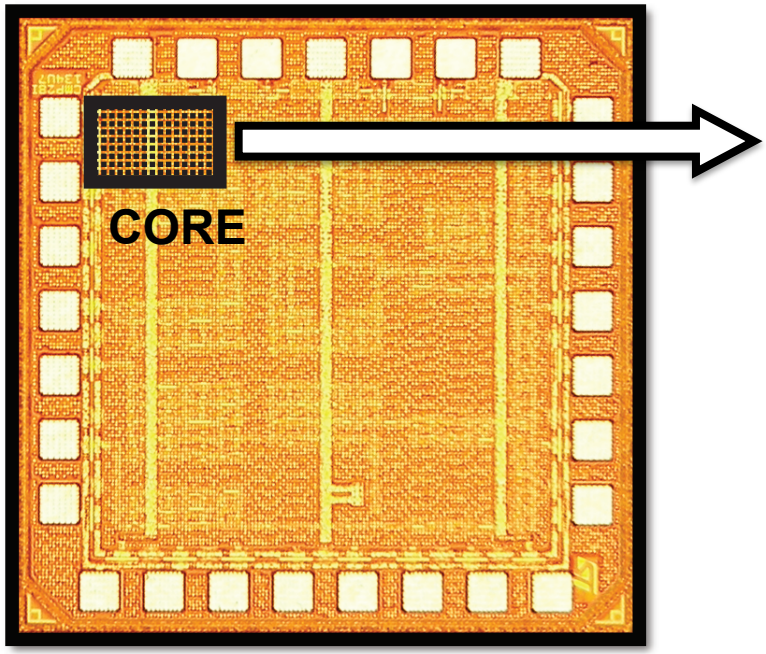
Calibration: Acquisition

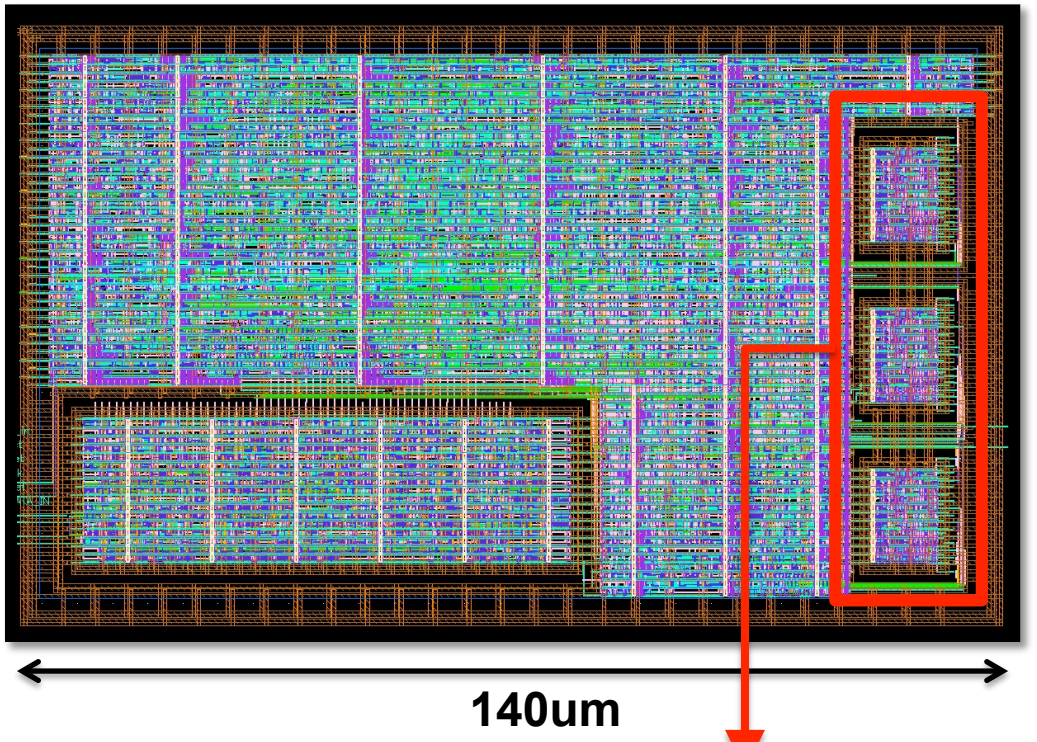


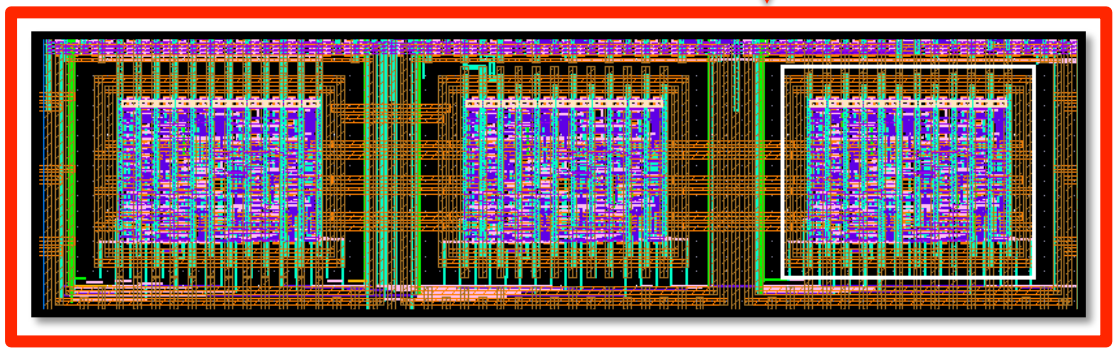
Calibration: Tracking



Chip micrograph and Layout

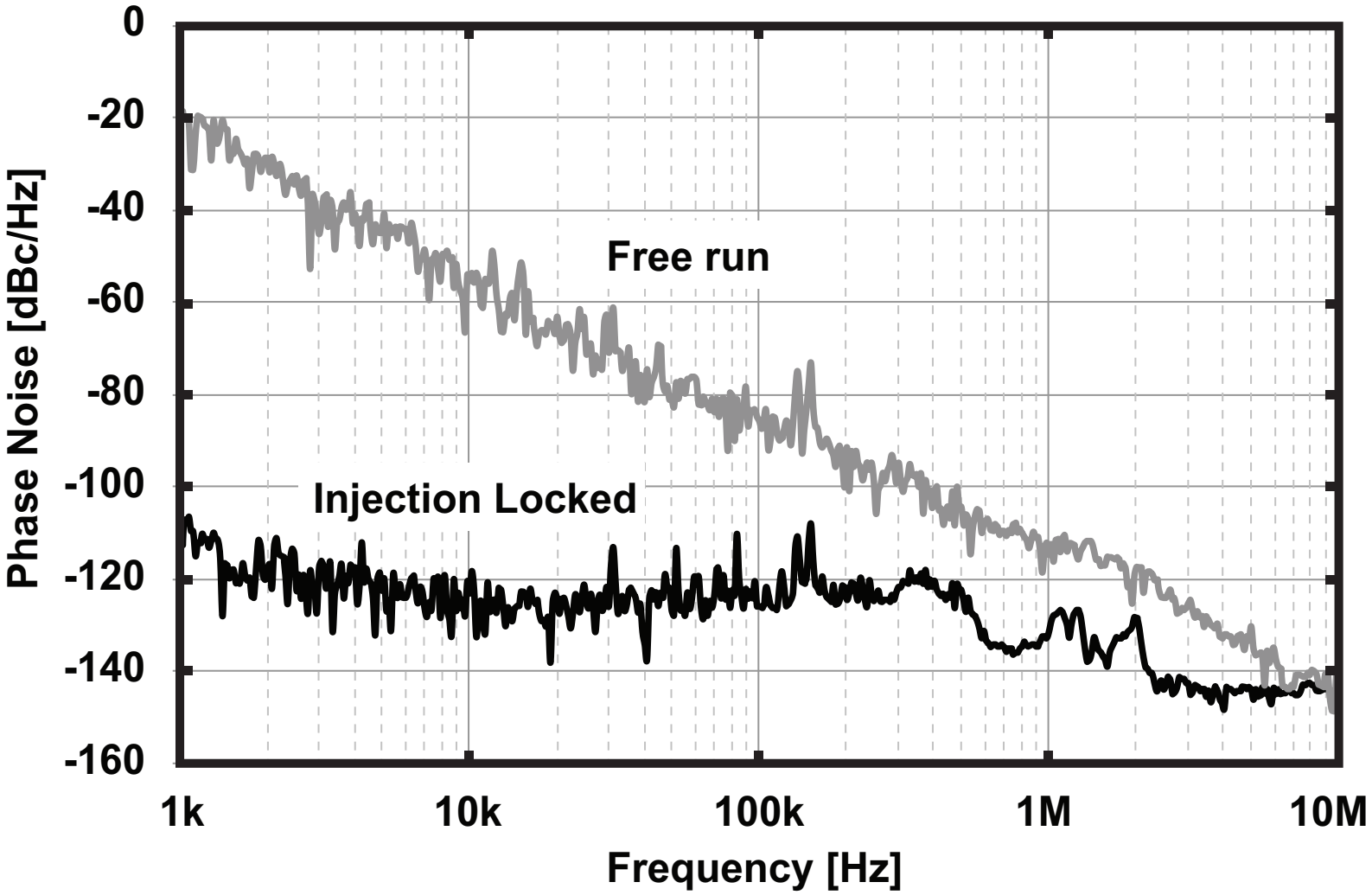






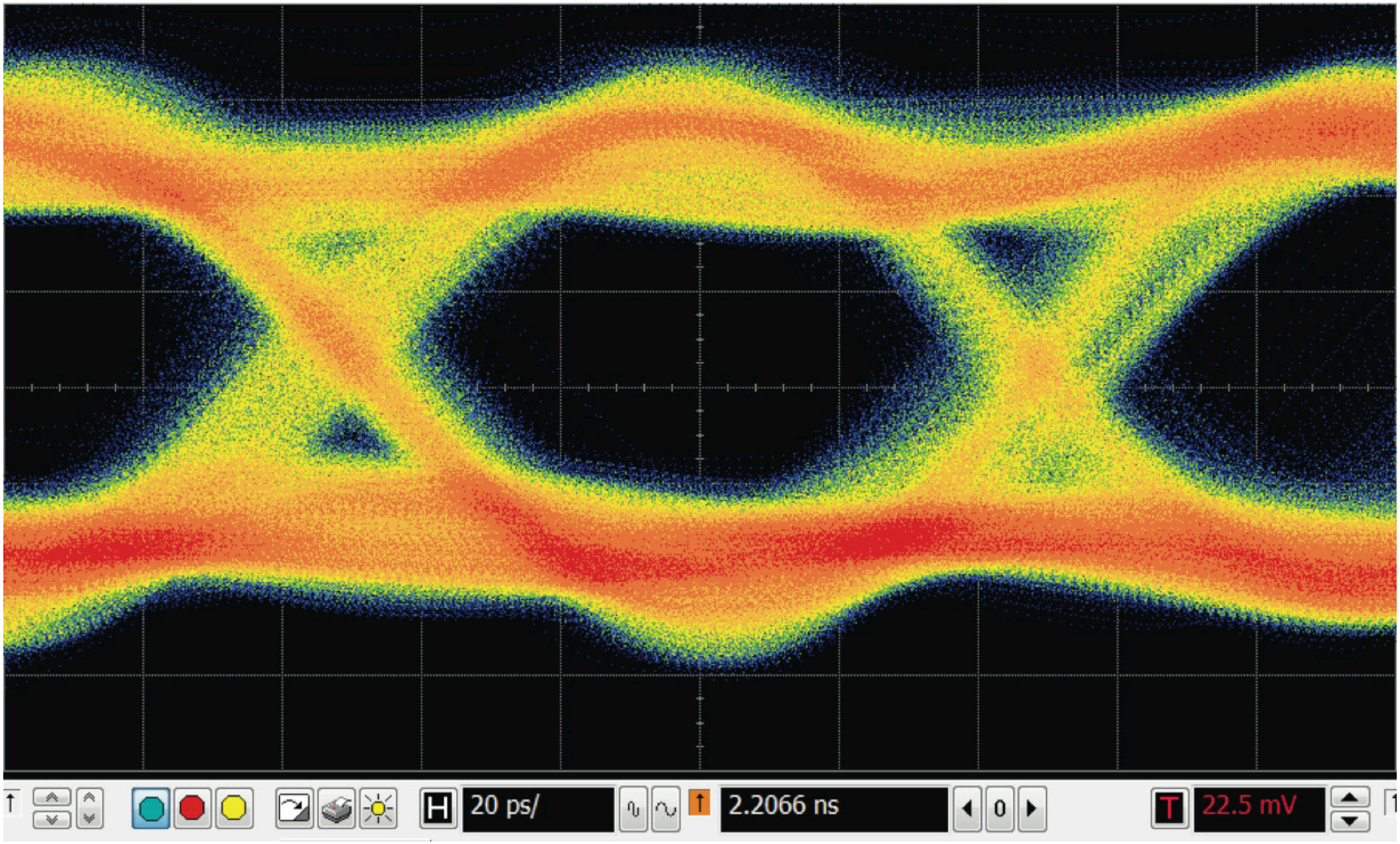
Identical DCOs

Measurement Results



- Phase noise measured with SG as input.

Eye Diagram



- Eye pattern measured at 10.05Gbps

Performance Comparison

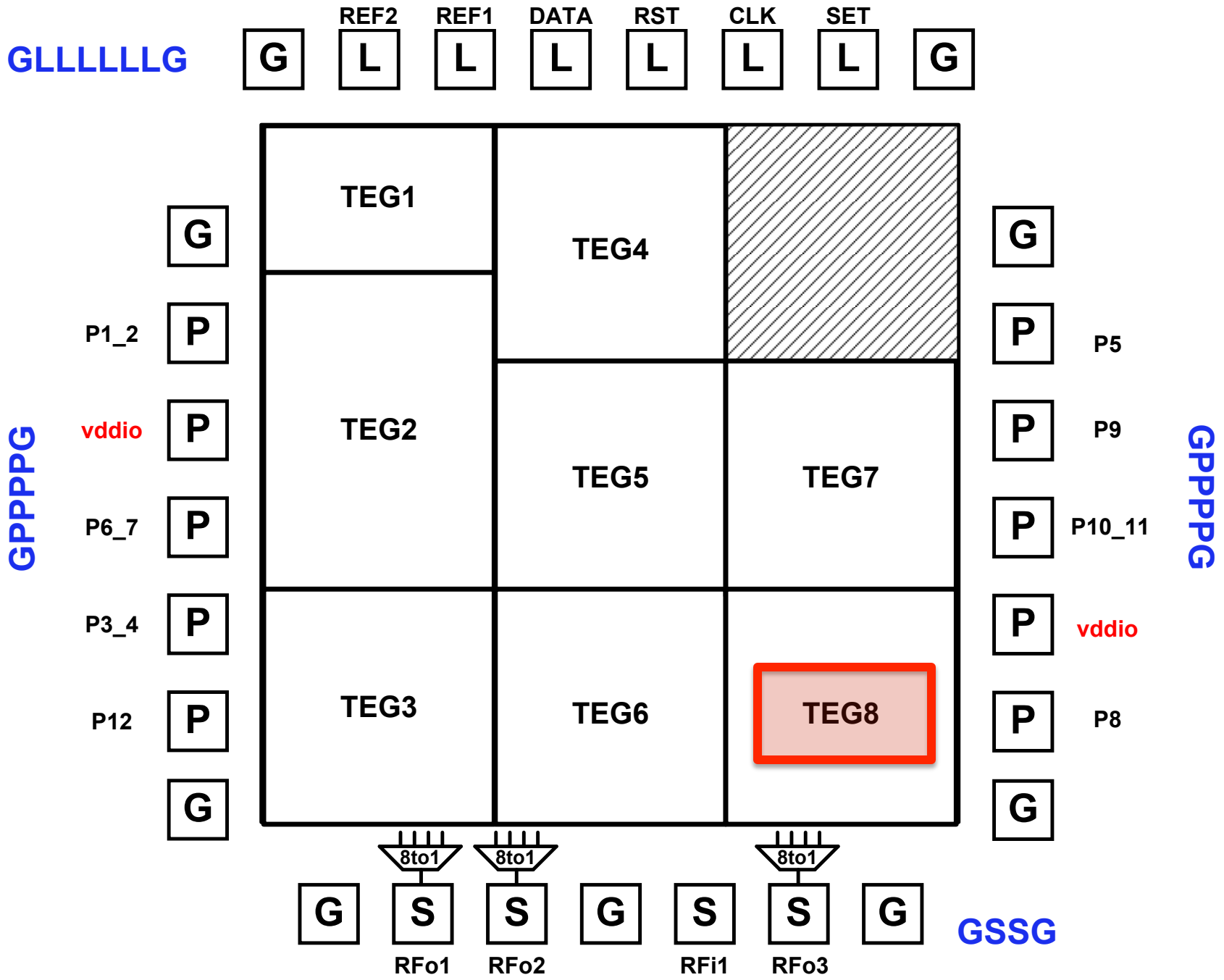
	[1]	[2]	[3]	[4]	**This**
Technology	90nm	180nm	90nm	40nm	**28nm**
Data Rate (Gb/s)	20	10	6	8	**10**
Feature	Analog	Analog	Digital	Digital	**Digital**
Locking Time (bits)	N.A	32	N.A.	N.A.	**1**
Power (mW)	102 (core)	200	16.6	12	**16**
Area (mm^2)	0.96	3.4	0.234	0.0052	**0.011**

[1] J. Lee, *et. al.,* JSSC 2008.
[2] C.F Liang, *et. al.,* CICC 2006.
[3] M. Loh, *et. al.,* VLSI 2010.
[4] H. Pan, *et. al., ISSCC 2011.*

Conclusion

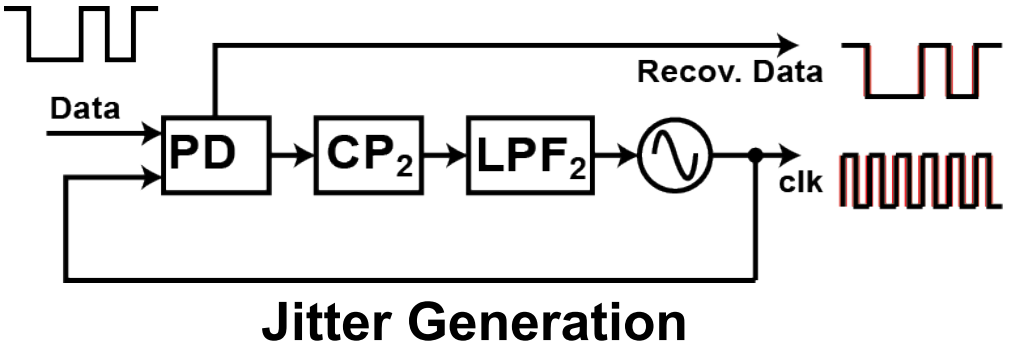
- **Fully-synthesizable CDR is presented.**
  - **Co-synthesis with digital core is possible.**
  - **Saves design time and cost.**
- **Challenges arising from limited control over the layout is solved at architecture level.**
  - **Edge Injection.**
  - **Interpolative phase-coupled DCO.**
  - **I-DAC.**
  - **PVT calibration.**

APPENDIX

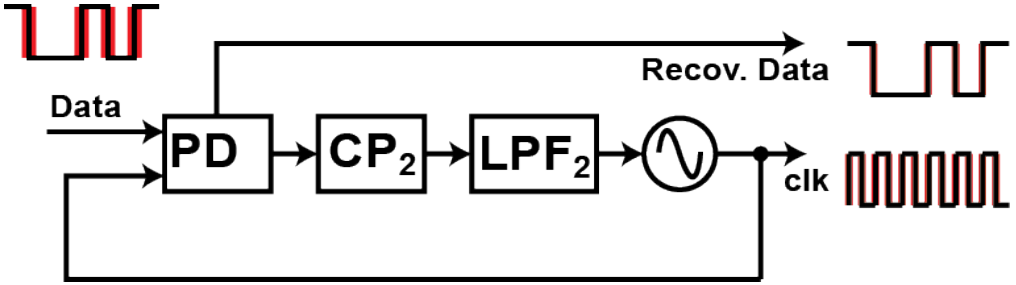

vddio: supply pin for I/O frame
(should be connected for all meas.)
GLLLLLLG
G
REF2
L
REF1
L
DATA
L
RST
L
CLK
L
SET
L
G
TEG1
TEG4
TEG2
TEG5
TEG7
TEG3
TEG6
TEG8
GPPPPG
G
P1_2
P
vddio
P
P6_7
P
P3_4
P
P12
P
G
GPPPPG
G
P
P5
P
P9
P
P10_11
P
vddio
P
P8
G
8to1
8to1
8to1
G
S
RFo1
S
RFo2
G
S
RFi1
S
RFo3
G
GSSG

Performance Metrics

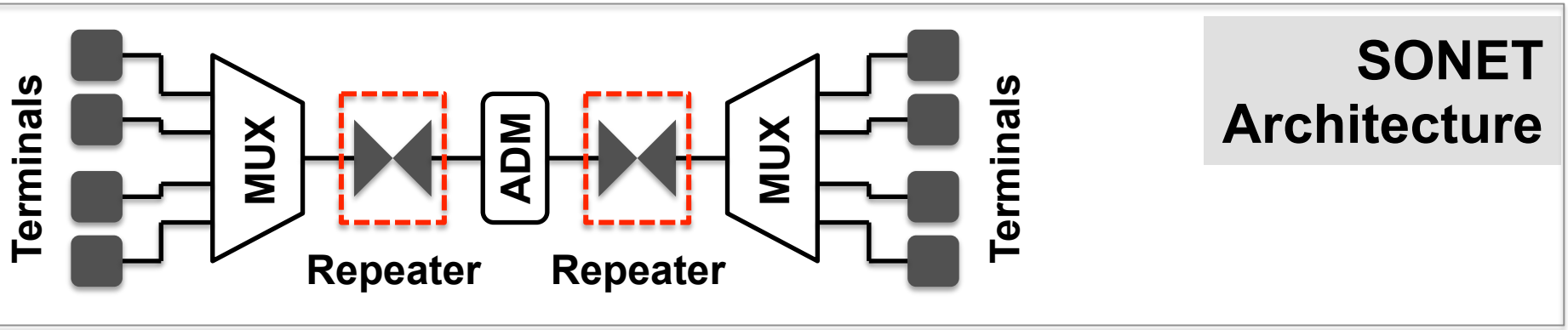
- **Jitter Generation.**
- **Jitter Tolerance.**
- **Jitter Transfer.**
- **Acquisition Time.**
- **Capture Range.**



Jitter Generation



Jitter Tolerance

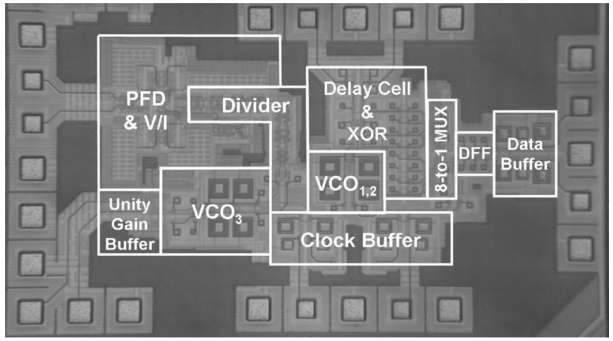


SONET Architecture

Why Fully-Synthesizable.

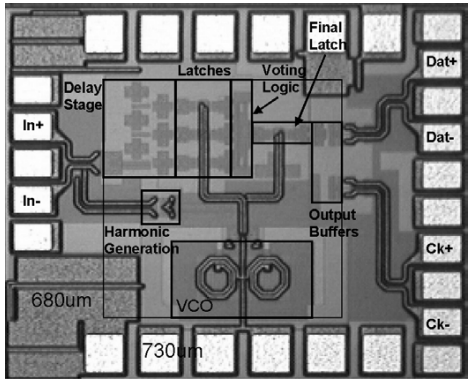
Analog Implementations

[1]



800umx1200um [90nm]
20Gbps

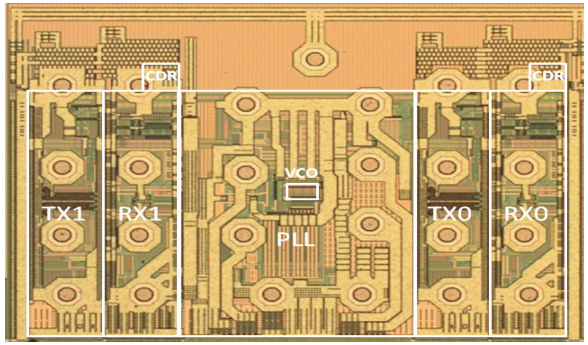
[2]



730umx680um [SiGe]
10.3Gbps

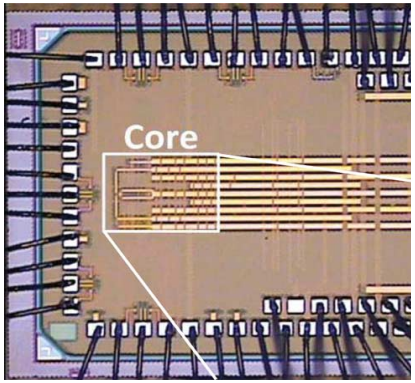
Digital Implementations

[3]



72umx72um [40nm]
8Gbps

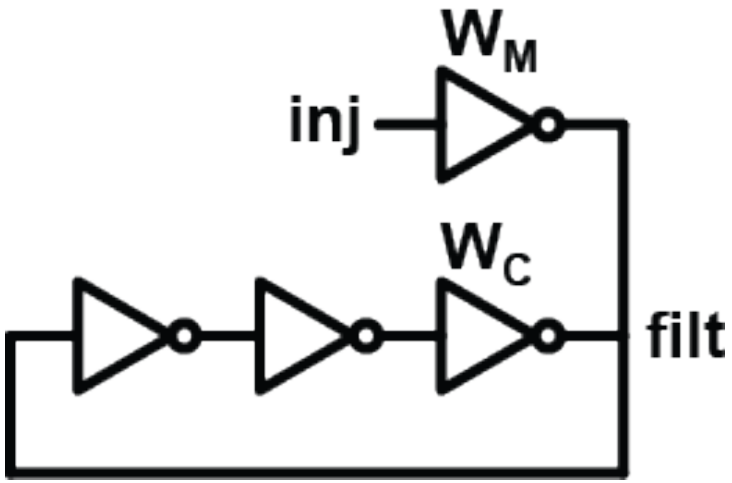
[4]



460umx330um [90nm]
3x9Gbps

[1] Jri Lee, *et. al.,* JSSC 2008
[2] Jing-Hong, *et. al.,* CICC 2005
[3] Matthew Loh, *et. al.,* JSSC 2012
[4] Hui Pan, *et. al.,* ISSCC 2011

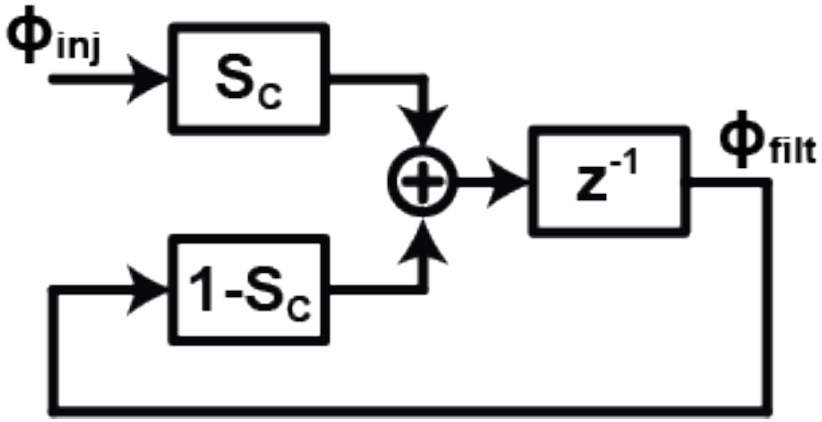
Phase Filtering

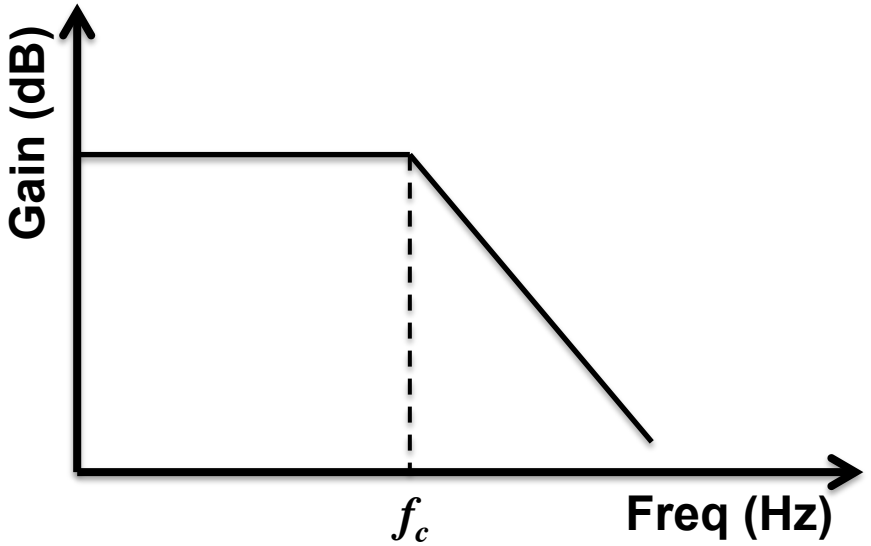


$$S_C = \frac{W_M}{W_M + W_C}$$

$$\frac{\phi_{filt}}{\phi_{inj}} = \frac{S_C}{z - (1 - S_C)}$$

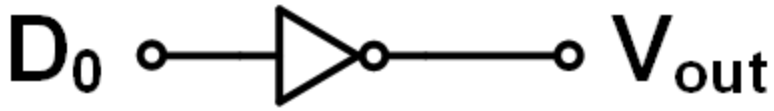
$$P_0 = \frac{ln(1 - S_C)}{T_i} \ (rad/s)$$





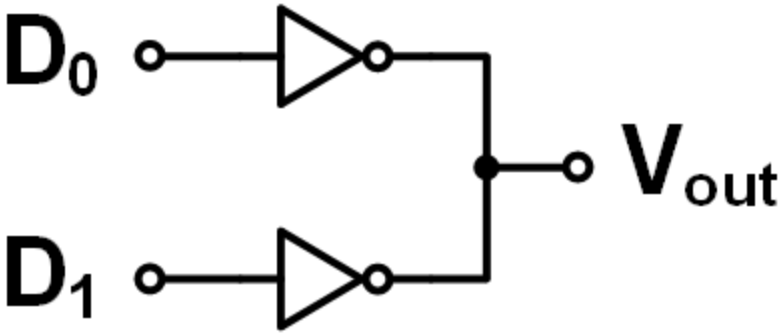
Hiok et. al, 2003 JSSC

Simple Voltage-output DAC



$D_0 = 0$ $V_{out} = 1V$

$D_0 = 1$ $V_{out} = 0V$



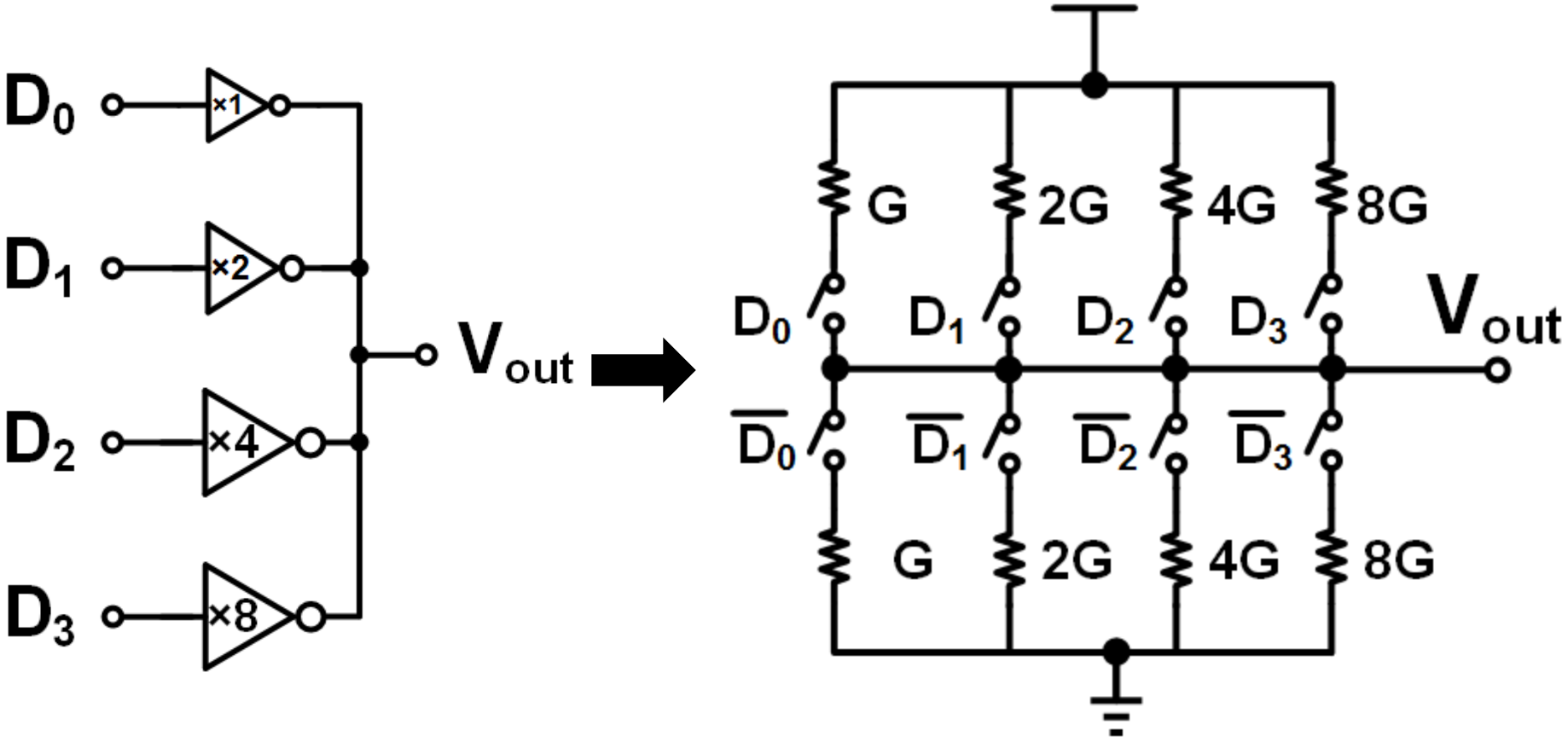
$D_0D_1 = 11$ $V_{out} = 0V$

$D_0D_1 = 10$ $V_{out} = 0.5V$

$D_0D_1 = 01$ $V_{out} = 0.5V$

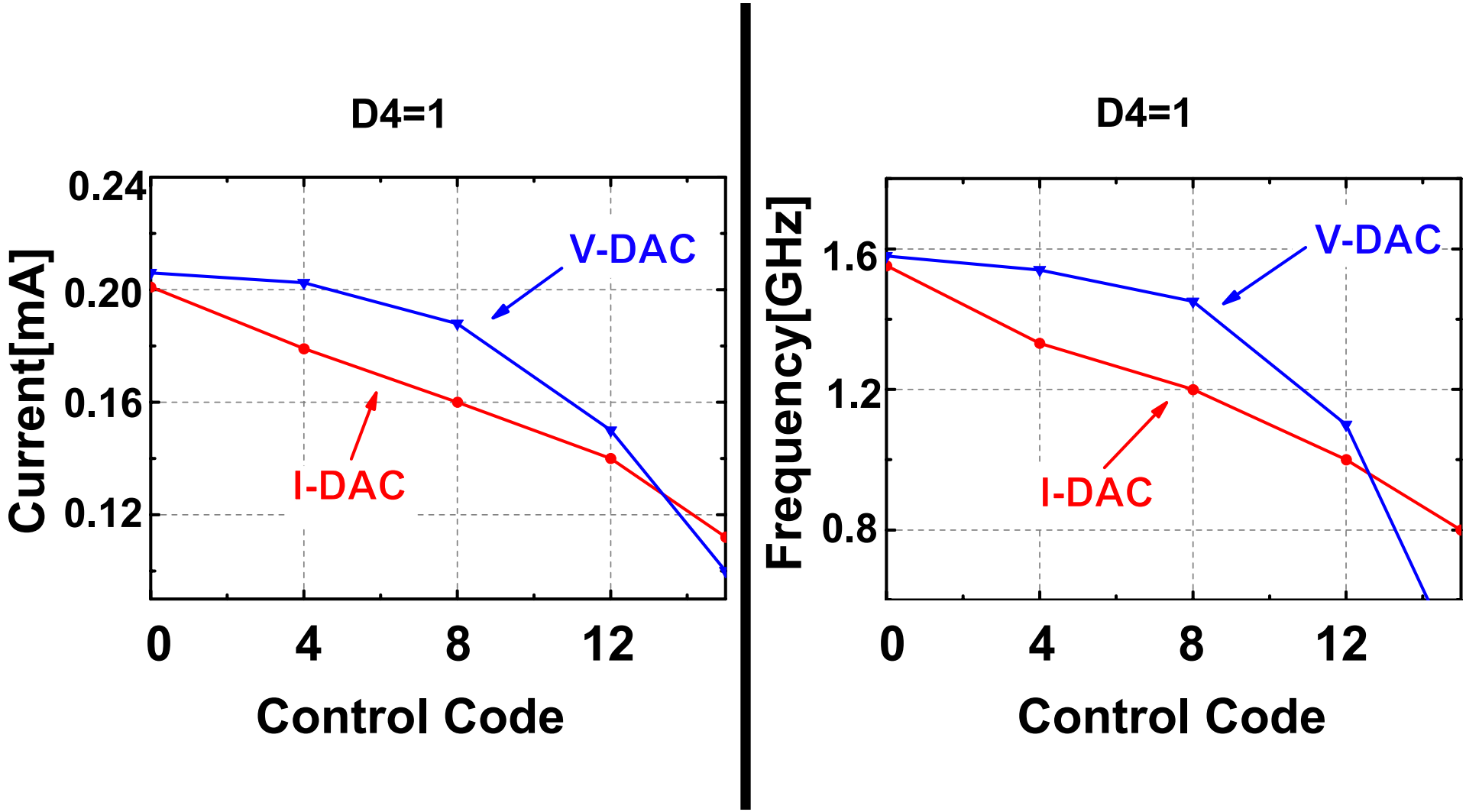
$D_0D_1 = 00$ $V_{out} = 1V$

Model of V-linear DAC

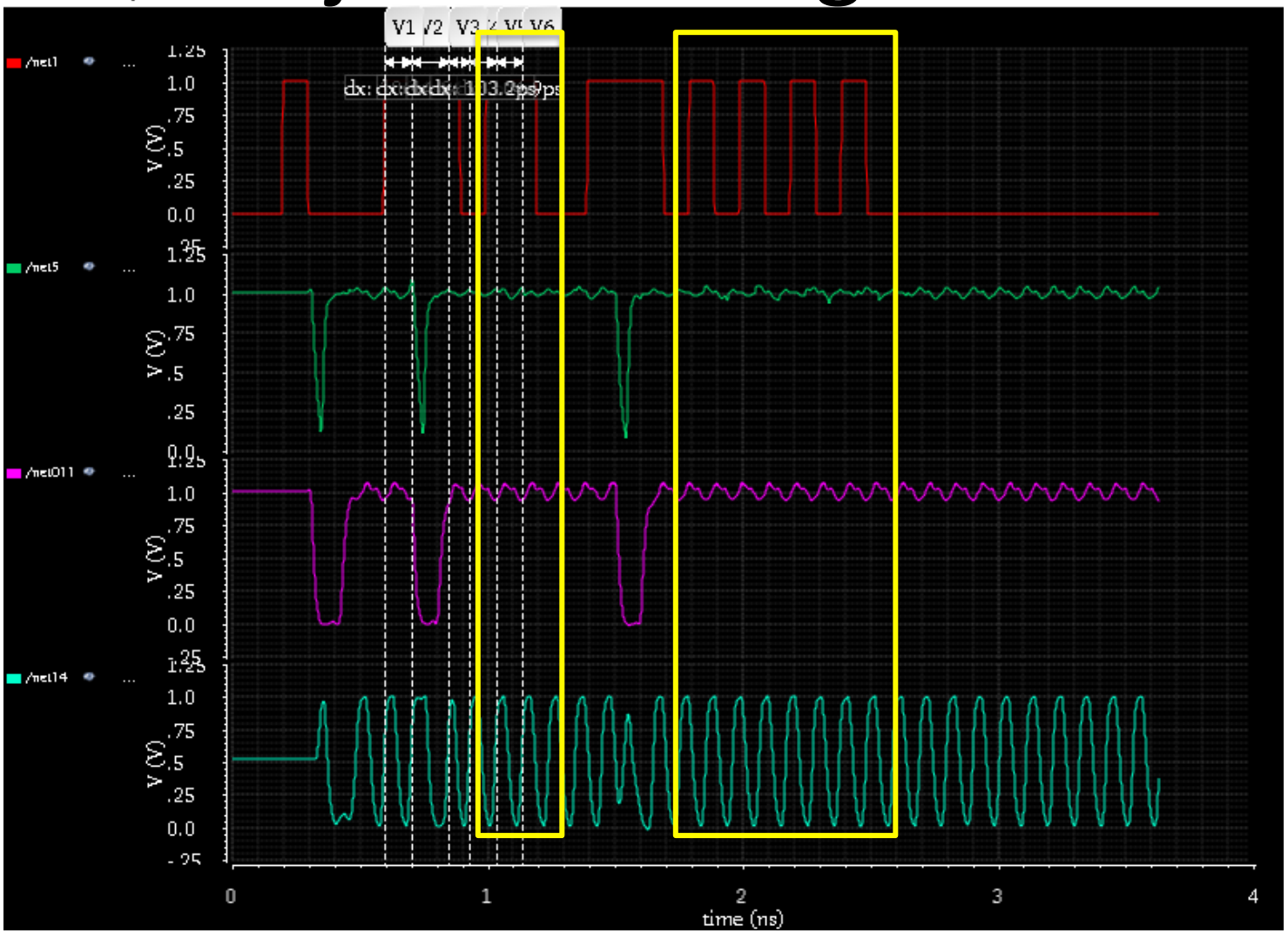


- How to obtain a **I-linear** DAC?

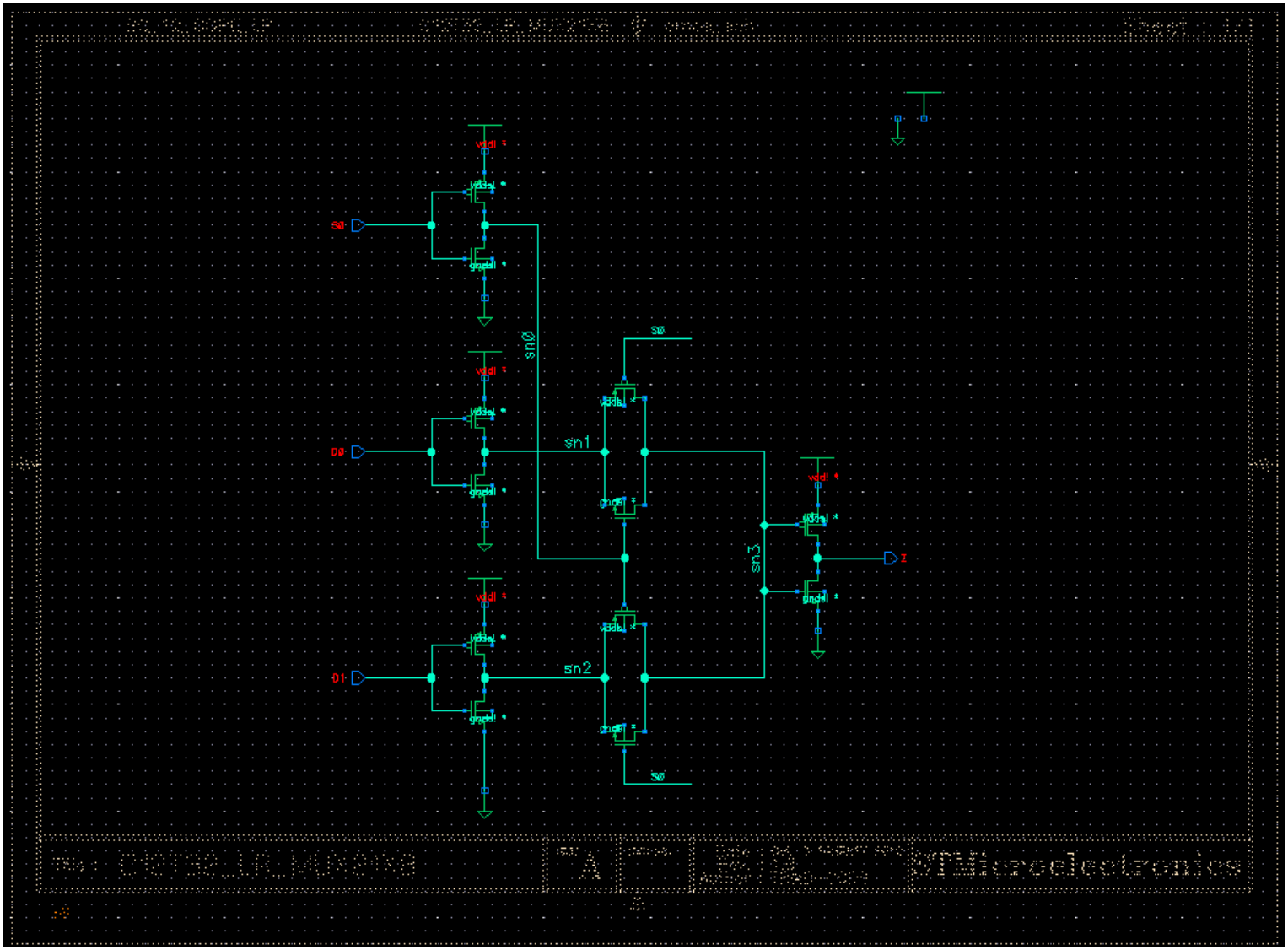
V-DAC VS I-DAC


D4=1
Current[mA]
0.24
0.20
0.16
0.12
V-DAC
I-DAC
0
4
8
12
Control Code
D4=1
Frequency[GHz]
1.6
1.2
0.8
V-DAC
I-DAC
0
4
8
12
Control Code

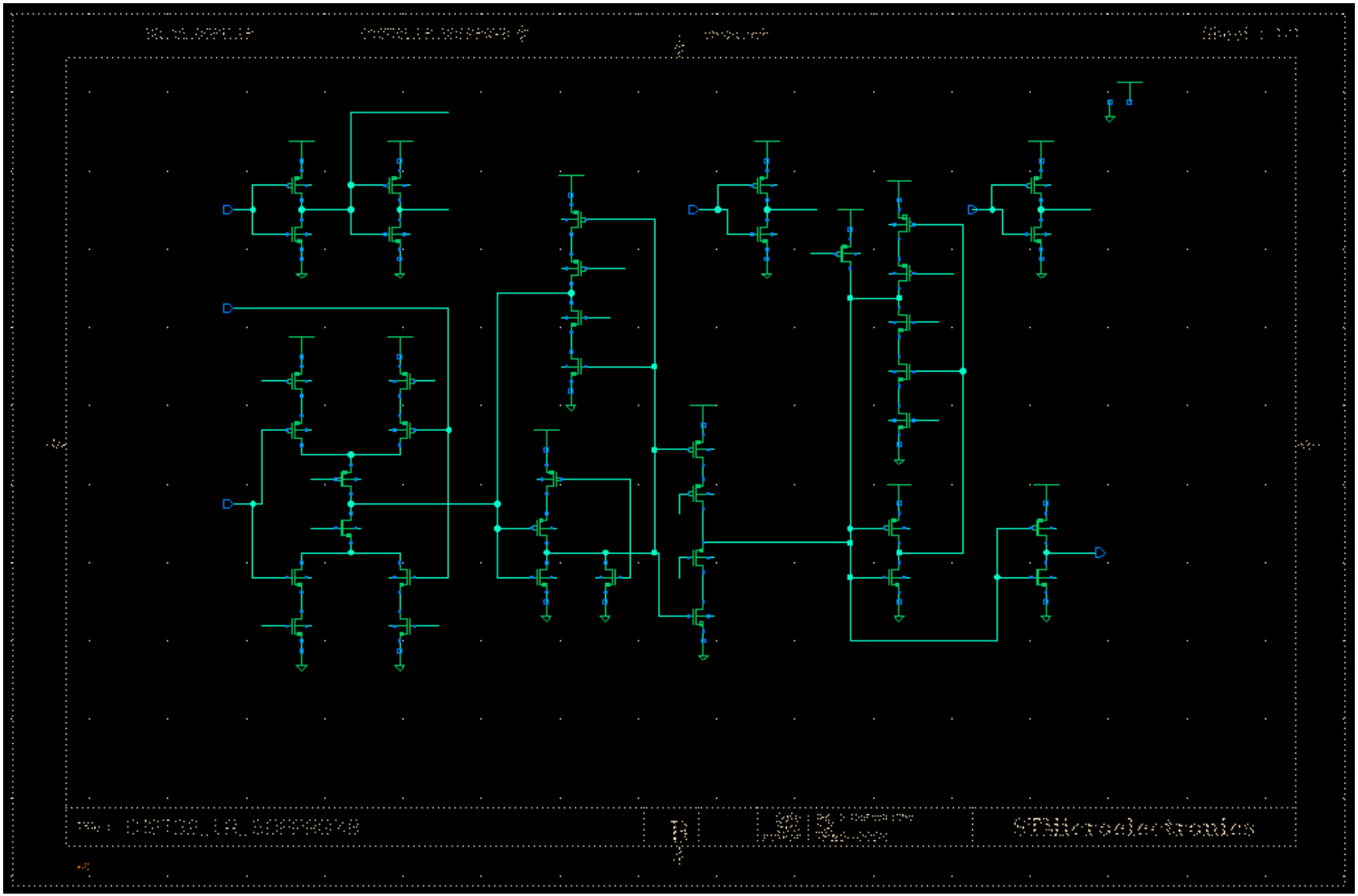
Injection Using DFF



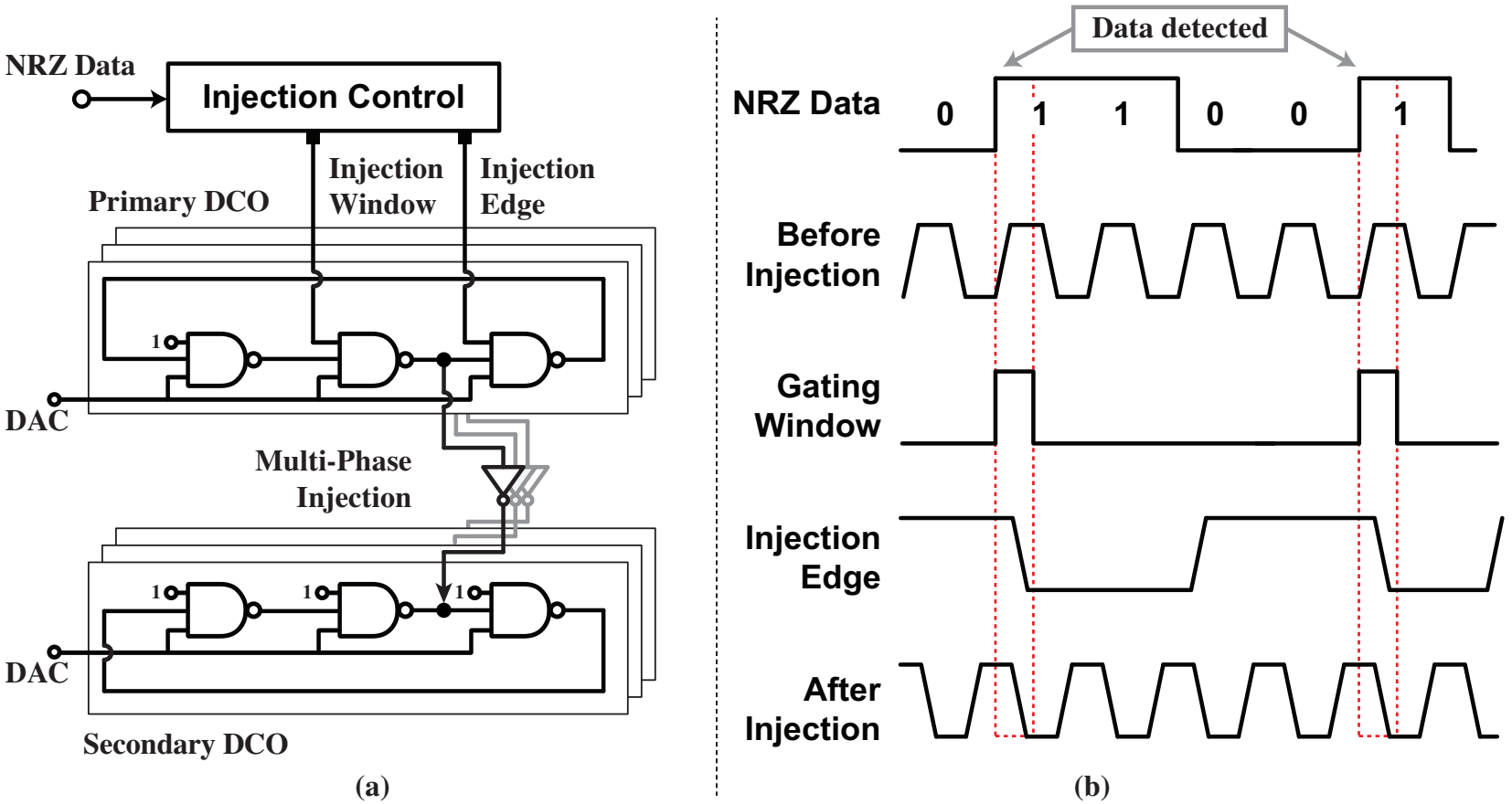
2:1 MUX [ST 28nm]



DFF [ST 28nm]



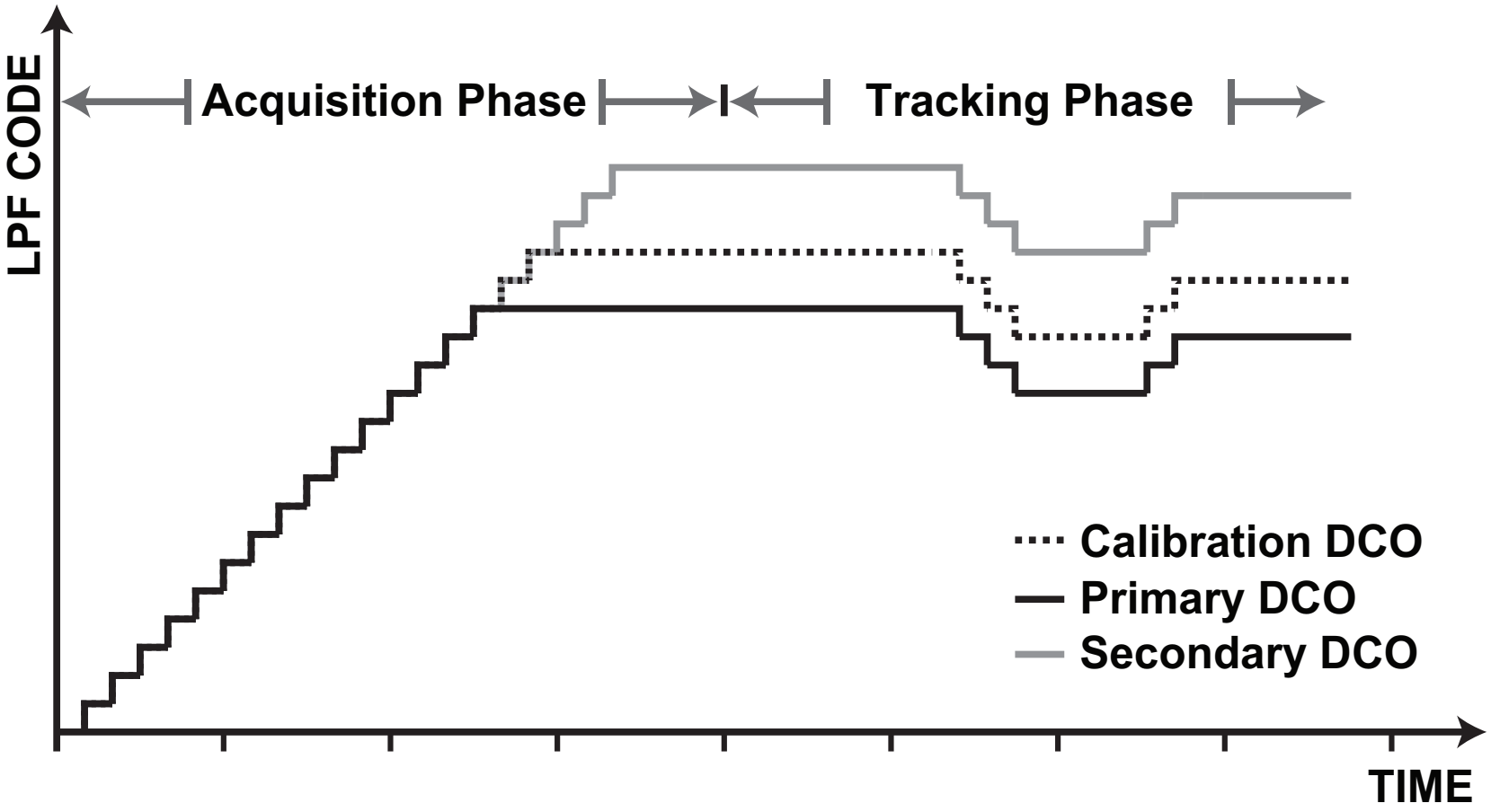
Phase Filtering



- **More jitter suppression by changing injection strength**
- **Multi-phase injection for balanced phase and amplitude**

Deng *et. al.*, 2003 JSSC.
Hiok *et. al.*, 2003 JSSC.

Calibration



- **<u>Faster settling time</u> compered to conventional calibration scheme.**